

74FST3244

8-Bit Bus Switch

The ON Semiconductor 74FST3244 is an 8-bit, high performance switch. The device is CMOS TTL compatible when operating between 4 and 5.5 Volts. The device exhibits extremely low R_{ON} and adds nearly zero propagation delay. The device adds no noise or ground bounce to the system.

The device consists of two 4-bit switches with separate Output/Enable (\overline{OE}) pins. Port A is connected to Port B when \overline{OE} is low. If \overline{OE} is high, the switch is high Z.

Features

- $R_{ON} < 4 \Omega$ Typical
- Less Than 0.25 ns–Max Delay Through Switch
- Nearly Zero Standby Current
- No Circuit Bounce
- Control Inputs are TTL/CMOS Compatible
- Pin-For-Pin Compatible with QS3244, FST3244, CBT3244
- All Popular Packages: QSOP–20, TSSOP–20, SOIC–20
- All Devices in Package TSSOP are Inherently Pb-Free*

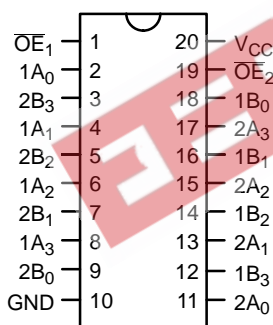


Figure 1. 20-Lead Pinout

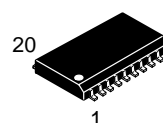
TRUTH TABLE

| Inputs | | Inputs/Outputs | |
|-------------------|-------------------|----------------|---------|
| \overline{OE}_1 | \overline{OE}_2 | 1A, 1B | 2A, 2B |
| L | L | 1A = 1B | 2A = 2B |
| L | H | 1A = 1B | Z |
| H | L | Z | 2A = 2B |
| H | H | Z | Z |

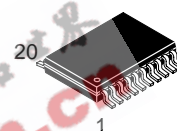
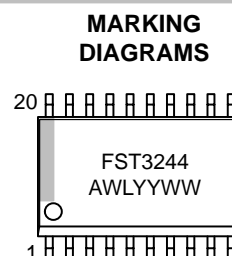


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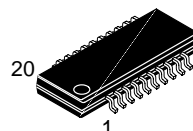
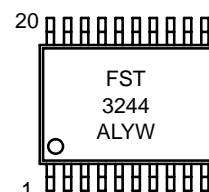
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SOIC–20
DW SUFFIX
CASE 751D



TSSOP–20
DT SUFFIX
CASE 948E



QSOP–20
QS SUFFIX
CASE 492A



A = Assembly Location
L, WL = Wafer Lot
Y = Year
W, WW = Work Week

PIN NAMES

| Pin | Description |
|------------------------------------|--------------------|
| $\overline{OE}_1, \overline{OE}_2$ | Bus Switch Enables |
| 1A, 2A | Bus A |
| 1B, 2B | Bus B |

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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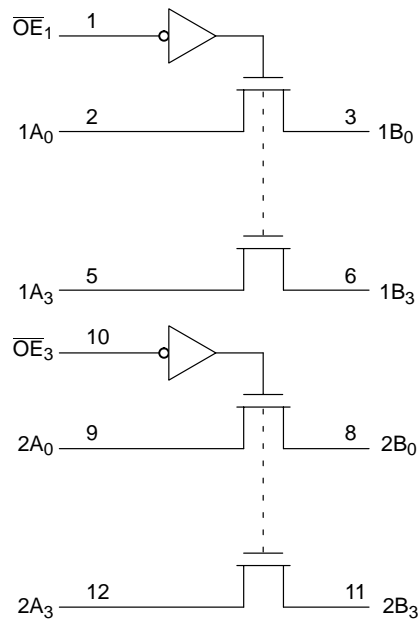


Figure 2. Logic Diagram

ORDERING INFORMATION

| Device Order Number | Package | Shipping [†] |
|---------------------|------------------------|--------------------------|
| 74FST3244DW | SOIC-20 | 55 Units / Rail |
| 74FST3244DWR2 | SOIC-20 | 1000 Units / Tape & Reel |
| 74FST3244DT | TSSOP-20* (Pb-Free) | 75 Units / Rail |
| 74FST3244DTR2 | TSSOP-20* (Pb-Free) | 2500 Units / Tape & Reel |
| 74FST3244QS | QSOP-20 | 55 Units / Rail |
| 74FST3244QSR | QSOP-20 | 2500 Units / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

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MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|----------------------|--|----------------------|------|
| V _{CC} | DC Supply Voltage | − 0.5 to +7.0 | V |
| V _I | DC Input Voltage | − 0.5 to +7.0 | V |
| V _O | DC Output Voltage | − 0.5 to +7.0 | V |
| I _{IK} | DC Input Diode Current V _I < GND | − 50 | mA |
| I _{OK} | DC Output Diode Current V _O < GND | − 50 | mA |
| I _O | DC Output Sink Current | 128 | mA |
| I _{CC} | DC Supply Current per Supply Pin | ± 100 | mA |
| I _{GND} | DC Ground Current per Ground Pin | ± 100 | mA |
| T _{STG} | Storage Temperature Range | − 65 to +150 | °C |
| T _L | Lead Temperature, 1 mm from Case for 10 Seconds | 260 | °C |
| T _J | Junction Temperature Under Bias | + 150 | °C |
| θ _{JA} | Thermal Resistance (Note 1) SOIC TSSOP QSOP | 96 128 200 | °C/W |
| MSL | Moisture Sensitivity | Level 1 | |
| F _R | Flammability Rating Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in | |
| V _{ESD} | ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) | > 2000 > 200 | V |
| I _{Latchup} | Latchup Performance Above V _{CC} and Below GND at 85°C (Note 4) | ± 500 | mA |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|-----------------|--|--------|-----------------|------|
| V _{CC} | Supply Voltage Operating, Data Retention Only | 4.0 | 5.5 | V |
| V _I | Input Voltage (Note) | 0 | 5.5 | V |
| V _O | Output Voltage (HIGH or LOW State) | 0 | V _{CC} | V |
| T _A | Operating Free-Air Temperature | − 40 | + 85 | °C |
| Δt/ΔV | Input Transition Rise or Fall Rate Switch Control Input Switch I/O | 0 0 | 5 DC | ns/V |

5. Unused control inputs may not be left open. All control inputs must be tied to a high or low logic input voltage level.

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DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | V _{CC} (V) | T _A = -40°C to +85°C | | | Unit |
|------------------|---------------------------------------|--|------------------------|---------------------------------|------|------|------|
| | | | | Min | Typ* | Max | |
| V _{IK} | Clamp Diode Resistance | I _{IN} = -18mA | 4.5 | | | -1.2 | V |
| V _{IH} | High-Level Input Voltage | | 4.0 to 5.5 | 2.0 | | | V |
| V _{IL} | Low-Level Input Voltage | | 4.0 to 5.5 | | | 0.8 | V |
| I _I | Input Leakage Current | 0 ≤ V _{IN} ≤ 5.5 V | 5.5 | | | ±1.0 | μA |
| I _{OZ} | OFF-STATE Leakage Current | 0 ≤ A, B ≤ V _{CC} | 5.5 | | | ±1.0 | μA |
| R _{ON} | Switch On Resistance (Note 6) | V _{IN} = 0 V, I _{IN} = 64 mA | 4.5 | | 4 | 7 | Ω |
| | | V _{IN} = 0 V, I _{IN} = 30 mA | 4.5 | | 4 | 7 | |
| | | V _{IN} = 2.4 V, I _{IN} = 15 mA | 4.5 | | 8 | 15 | |
| | | V _{IN} = 2.4 V, I _{IN} = 15 mA | 4.0 | | 11 | 20 | |
| I _{CC} | Quiescent Supply Current | V _{IN} = V _{CC} or GND, I _{OUT} = 0 | 5.5 | | | 3 | μA |
| ΔI _{CC} | Increase In I _{CC} per Input | One input at 3.4 V, Other inputs at V _{CC} or GND | 5.5 | | | 2.5 | mA |

*Typical values are at V_{CC} = 5.0 V and T_A = 25°C.

6. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Figures | Limits | | | | Unit |
|--|-----------------------------------|---|---------|---------------------------------|------|-------------------------|------|------|
| | | | | T _A = -40°C to +85°C | | | | |
| | | | | V _{CC} = 4.5 to 5.5 V | | V _{CC} = 4.0 V | | |
| Min | Max | Min | Max | | | | | |
| t _{PHL} , t _{PLH} | Prop Delay Bus to Bus (Note 7) | V _I = OPEN | 3 and 4 | | 0.25 | | 0.25 | ns |
| t _{PZH} , t _{PZL} | Output Enable Time | V _I = 7 V for t _{PZL} V _I = OPEN for t _{PZH} | 3 and 4 | 1.0 | 5.6 | | 6.1 | ns |
| t _{PHZ} , t _{PLZ} | Output Disable Time | V _I = 7 V for t _{PLZ} V _I = OPEN for t _{PHZ} | 3 and 4 | 1.5 | 6.2 | | 5.6 | ns |

7. This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

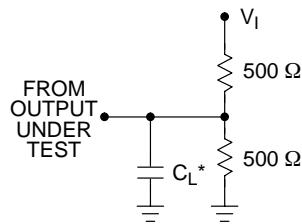
CAPACITANCE (Note 8)

| Symbol | Parameter | Conditions | Typ | Max | Unit |
|------------------|-------------------------------|---|-----|-----|------|
| C _{IN} | Control Pin Input Capacitance | V _{CC} = 5.0 V | 3 | | pF |
| C _{I/O} | Input/Output Capacitance | V _{CC} , \overline{OE} = 5.0 V | 5 | | pF |

8. T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

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AC Loading and Waveforms



NOTES:

1. Input driven by 50 Ω source terminated in 50 Ω.
 2. C_L includes load and stray capacitance.
- *C_L = 50 pF

Figure 3. AC Test Circuit

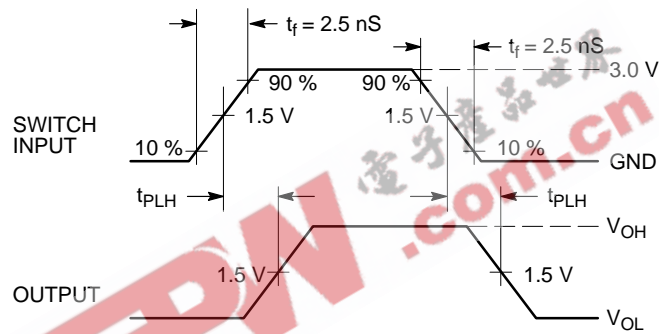


Figure 4. Propagation Delays

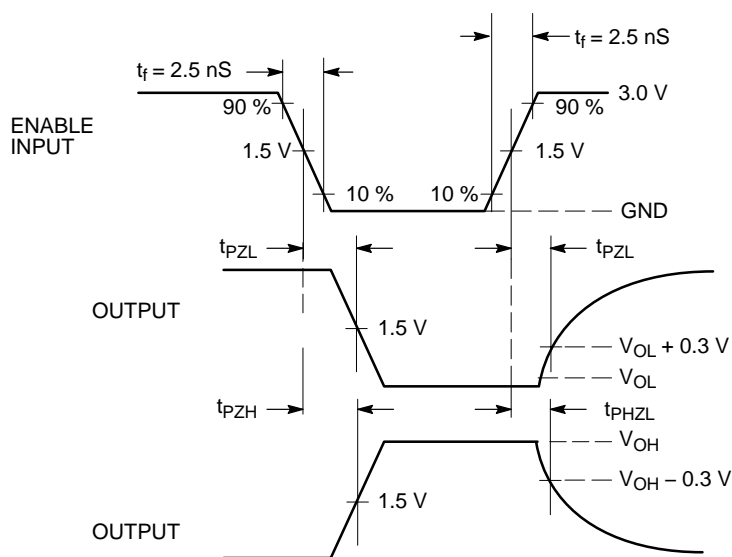
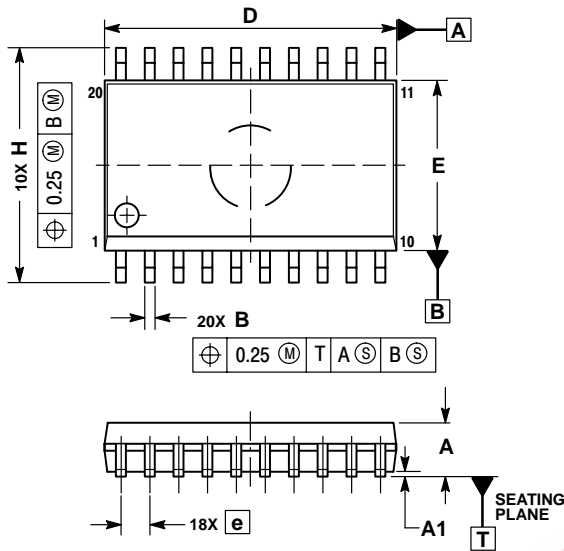


Figure 5. Enable/Disable Delays

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PACKAGE DIMENSIONS

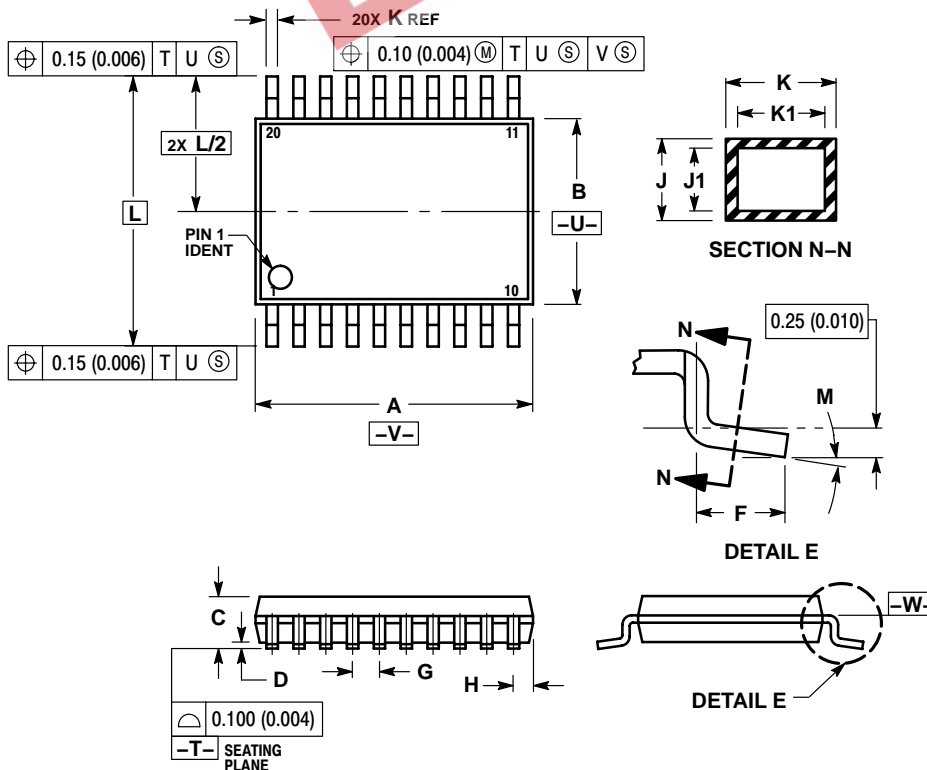
SOIC-20
DW SUFFIX
CASE 751D-05
ISSUE G



- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| MILLIMETERS | | |
|-------------|----------|-------|
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

TSSOP-20
DT SUFFIX
CASE 948E-02
ISSUE B



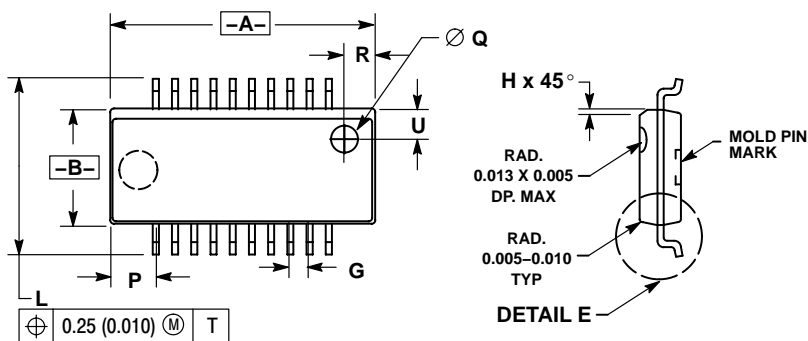
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

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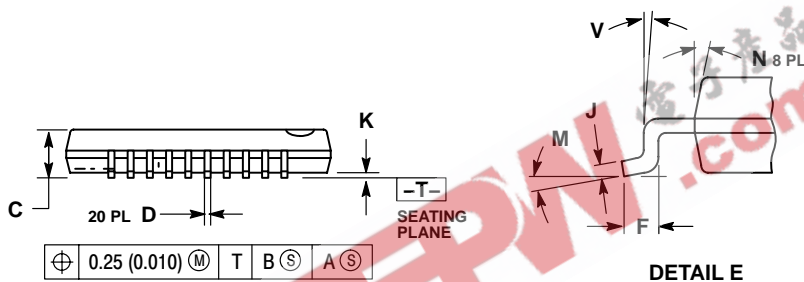
PACKAGE DIMENSIONS

QSOP-20
 QS SUFFIX
 CASE 492A-01
 ISSUE O




- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. THE BOTTOM PACKAGE SHALL BE BIGGER THAN THE TOP PACKAGE BY 4 MILS (NOTE: LEAD SIDE ONLY). BOTTOM PACKAGE DIMENSION SHALL FOLLOW THE DIMENSION STATED IN THIS DRAWING.
 4. PLASTIC DIMENSIONS DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 6 MILS PER SIDE.
 5. BOTTOM EJECTOR PIN WILL INCLUDE THE COUNTRY OF ORIGIN (COO) AND MOLD CAVITY I.D.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|--------|-------------|-------|
| | MAX | MIN | MAX | MIN |
| A | 0.337 | 0.344 | 8.56 | 8.74 |
| B | 0.150 | 0.157 | 3.81 | 3.99 |
| C | 0.061 | 0.068 | 1.55 | 1.73 |
| D | 0.008 | 0.012 | 0.20 | 0.31 |
| F | 0.016 | 0.035 | 0.41 | 0.89 |
| G | 0.025 BSC | | 0.64 BSC | |
| H | 0.008 | 0.018 | 0.20 | 0.46 |
| J | 0.0098 | 0.0075 | 0.249 | 0.191 |
| K | 0.004 | 0.010 | 0.10 | 0.25 |
| L | 0.230 | 0.244 | 5.84 | 6.20 |
| M | 0° | 8° | 0° | 8° |
| N | 0° | 7° | 0° | 7° |
| P | 0.052 | 0.062 | 1.32 | 1.58 |
| Q | 0.035 DIA | | 0.89 DIA | |
| R | 0.035 | 0.045 | 0.89 | 1.14 |
| U | 0.035 | 0.045 | 0.89 | 1.14 |
| V | 0° | 8° | 0° | 8° |



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