

September 1983 Revised February 1999

MM74HC273 Octal D-Type Flip-Flops with Clear

General Description

The MM74HC273 edge triggered flip-flops utilize advanced silicon-gate CMOS technology to implement D-type flip-flops. They possess high noise immunity, low power, and speeds comparable to low power Schottky TTL circuits. This device contains 8 master-slave flip-flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the LOW-to-HIGH transition of the CLOCK input. The CLEAR input when LOW, sets all outputs to a low state

Each output can drive 10 low power Schottky TTL equivalent loads. The MM74HC273 is functionally as well as pin compatible to the 74LS273. All inputs are protected from damage due to static discharge by diodes to $\rm V_{\rm CC}$ and ground.

Features

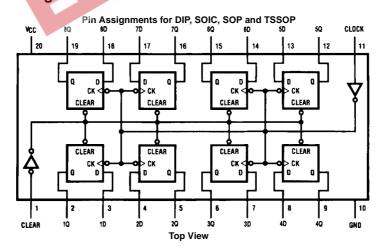
- Typical propagation delay: 18 ns
- Wide operating voltage range
- Low input current: 1 µA maximum
- Low quiescent current: 80 µA (74 Series)
- Output drive: 10 LS-TTL loads

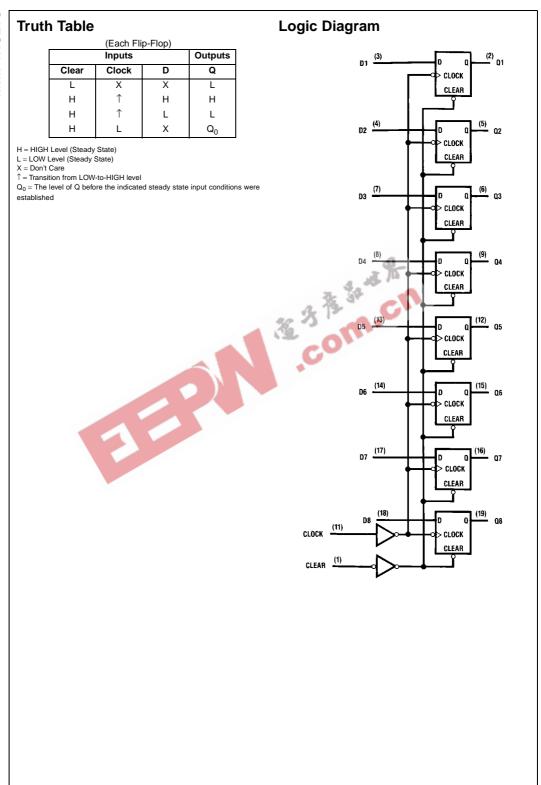
Ordering Code:

Order Number	Package Number	Package Description
MM74HC273M	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-153, 0.300" Wide
MM74HC273SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC273MTC	MTC20	20-Lead thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC273N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram





Absolute Maximum Ratings(Note 1)

(Note 2)

Supply Voltage (V _{CC})	-0.5 to $+7.0$ V
DC Input Voltage (V _{IN})	-1.5 to V_{CC} +1.5 V
DC Output Voltage (V _{OUT})	-0.5 to V_{CC} +0.5 V
Clamp Diode Current (I _{IK} , I _{OK})	±20 mA
DC Output Current, per pin (I _{OUT})	±25 mA
DC V _{CC} or GND Current, per pin (I _{CC})	±50 mA
Storage Temperature Range (T _{STG})	-65°C to +150°C
Power Dissipation (P _D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T _L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V _{CC})	2	6	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T _A)	-40	+85	°C
Input Rise or Fall Times			
$(t_{r}, t_{f}) V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: –
12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	v _{cc}	T _A = 25°C		$T_A = -40 \text{ to } 85^{\circ}\text{C}$	$T_A = -55 \text{ to } 125^{\circ}\text{C}$	Units
Symbol				Тур	36	Guaranteed L	imits	Ullits
V _{IH}	Minimum HIGH Level		2.0V	4	1.5	1.5	1.5	V
	Input Voltage		4.5V	26	3.15	3 .15	3.15	V
			6.0V	136	4.2	4.2	4.2	V
V _{IL}	Maximum LOW Level		2.0V	4	0.5	0.5	0.5	V
	Input Voltage		4.5V	1	1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V _{OH}	Minimum HIGH Level	$V_{IN} = V_{IH} \text{ or } V_{IL}$						
	Output Voltage	I _{OUT} ≤ 20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V _{IN} = V _{IH} or V _{IL}						
		$ I_{OUT} \le 4.0 \text{ mA}$	4.5V	4.2	3.98	3.84	3.7	V
		I _{OUT} ≤ 5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V _{OL}	Maximum LOW Level	$V_{IN} = V_{IH}$ or V_{IL}						
	Output Voltage	$ I_{OUT} \le 20 \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or V_{IL}						
		$ I_{OUT} \le 4 \text{ mA}$	4.5V	0.2	0.26	0.33	0.4	V
		$ I_{OUT} \le 5.2 \text{ mA}$	6.0V	0.2	0.26	0.33	0.4	V
I _{IN}	Maximum Input	V _{IN} = V _{CC} or GND	6.0V		±0.1	±1.0	±1.0	μΑ
	Current							
I _{CC}	Maximum Quiescent	V _{IN} = V _{CC} or GND	6.0V		8	80	160	μΑ
	Supply Current	$I_{OUT} = 0 \mu A$						

Note 4: For a power supply of 5V \pm 10% the worst case output voltages (V_{OH} , and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

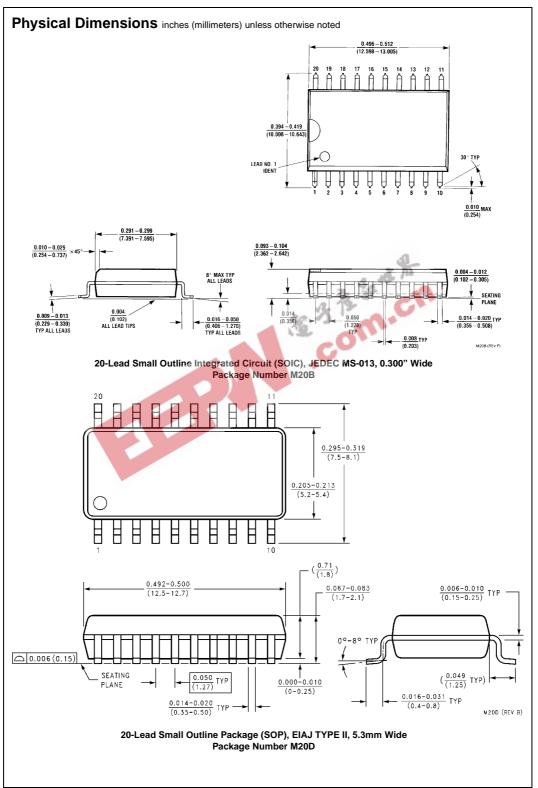
$v_{CC} = 5v, I_A =$	$= 25^{\circ}$ C, C _L $= 15$ pF, $t_r = t_f = 6$ ns				
Symbol	Parameter	Conditions	Тур	Guaranteed Limit	Unit
f _{MAX}	Maximum Operating		50	30	MH:
	Frequency				Unit MH2 ns ns ns ns ns ns ns ns
t _{PHL} , t _{PLH}	Maximum Propagation		18	27	ns
	Delay, Clock to Output				
t _{PHL}	Maximum Propagation		18	27	ns
	Delay, Clear to Output				
t _{REM}	Minimum Removal Time,		10	20	ns
	Clear to Clock				
t _s	Minimum Setup Time		10	20	ns
	Data to Clock				
t _H	Minimum Hold Time		-2	0	ns
	Clock to Data				
t _W	Minimum Pulse Width		10	16	ns
	Clock or Clear				

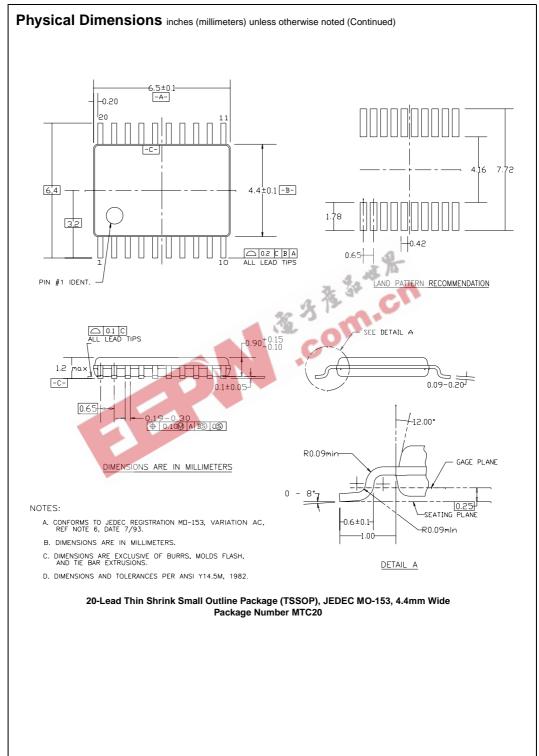
AC Electrical Characteristics

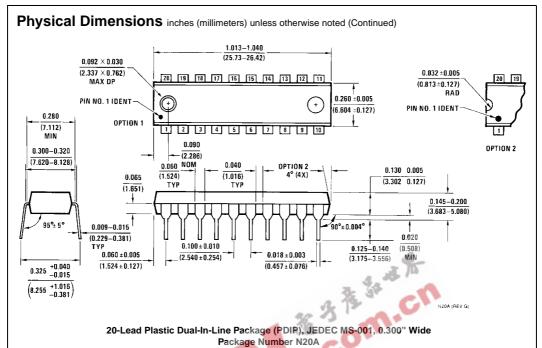
 $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	v _{cc}	T _A = 25°C		T _A = -40 to 85°C T _A = -55 to 125°C		Units
Cymbol				Тур	-40	Guaranteed L	imits	Oilles
f _{MAX}	Maximum Operating		2.0V	16	5	4	3	MHz
	Frequency		4.5V	74	27	21	18	MHz
			6.0V	78	31	24	20	MHz
t _{PHL} , t _{PLH}	Maximum Propagation		2.0V	38	135	170	205	ns
	Delay, Clock to Output		4.5V	14	27	34	41	ns
			6.0V	12	23	29	35	ns
t _{PHL}	Maximum Propagation		2.0V	42	135	170	205	ns
	Delay, Clear to Output		4.5V	19	27	34	41	ns
			6.0V	18	23	29	35	ns
t _{REM}	Minimum Removal Time		2.0V	0	25	32	37	ns
	Clear to Clock		4.5V	0	5	6	7	ns
			6.0V	0	4	5	6	ns
t _s	Minimum Setup Time		2.0V	26	100	125	150	ns
	Data to Clock		4.5V	7	20	25	30	ns
			6.0V	5	17	21	25	ns
t _H	Minimum Hold Time		2.0V	-15	0	0	0	ns
	Clock to Data		4.5V	-6	0	0	0	ns
			6.0V	-4	0	0	0	ns
t _W	Minimum Pulse Width		2.0V	34	80	100	120	ns
	Clock or Clear		4.5V	11	16	20	24	ns
			6.0V	10	14	18	20	ns
t _r , t _f	Maximum Input Rise and		2.0V		1000	1000	1000	ns
	Fall Time, Clock		4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t _{THL} , t _{TLH}	Maximum Output Rise		2.0V	28	75	95	110	ns
	and Fall Time		4.5V	11	15	19	22	ns
			6.0V	9	13	16	19	ns
C _{PD}	Power Dissipation	(per flip-flop)		45				pF
	Capacitance (Note 5)							
C _{IN}	Maximum Input			7	10	10	10	pF
	Capacitance							

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} \ V_{CC}^2 f + I_{CC} \ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$







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