DATA SHEET

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74F647
Octal transceiver/register, non-inverting (open-collector)

74F649
Octal transceiver/register, inverting (open-collector)

Product specification

1992 Feb 28

IC15 Data Handbook

Philips Semiconductors

PHILIPS

Octal transceivers/registers (open-collector) 74F647/74F649

74F647 Octal Transceiver/Register, Non-inverting (Open Collector)
74F649 Octal Transceiver/Register, Inverting (Open Collector)

FEATURES

- High impedance NPN base inputs for reduced loading (20µA in High and Low states)
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Choice of non-inverting and inverting data paths
- Open Collector outputs
- 300 mil wide 24-pin Slim Dip package

DESCRIPTION

The 74F647 and 74F649 Transceivers/Registers consist of bus transceiver circuits with open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a High logic level. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The select (SAB, SBA) controls can multiplex stored and real-time (transparent mode) data. The DIR determines which bus will receive data when the Output Enable, $\overline{OE}$ is active Low. In the isolation mode (Output Enable, $\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register.

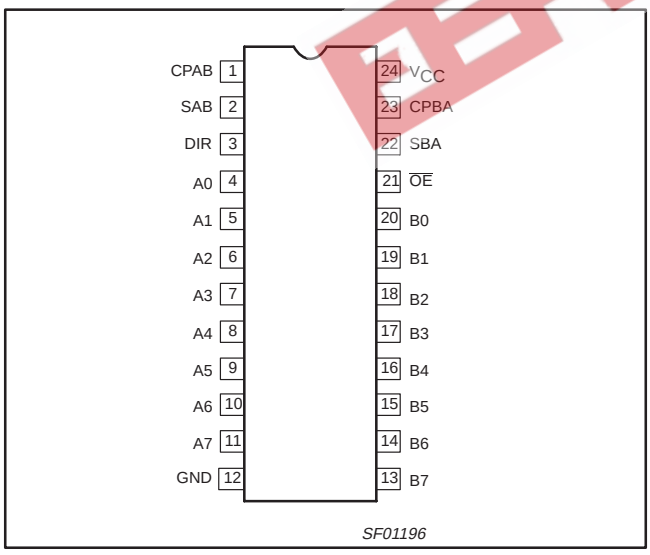
When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74F647 and 74F649.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F647	65MHz	125mA
74F649	65MHz	125mA

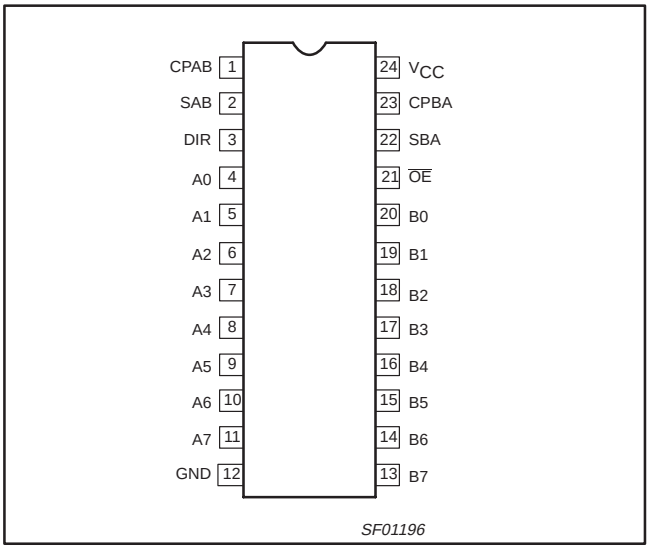
ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
24-pin plastic Slim DIP (300mil)	N74F647N, N74F649N	SOT222-1
24-pin plastic SOL	N74F647D, N74F649D	SOT137-1

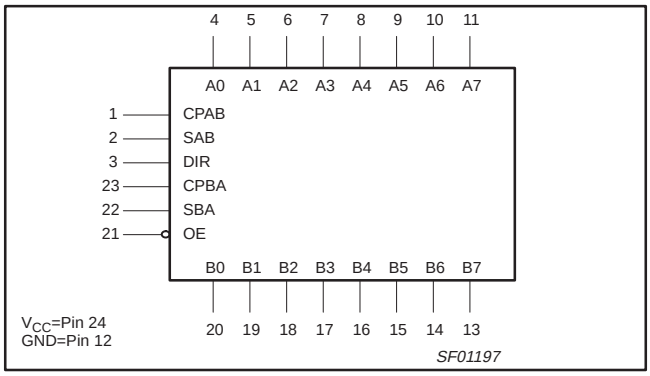
PIN CONFIGURATION – 74F647



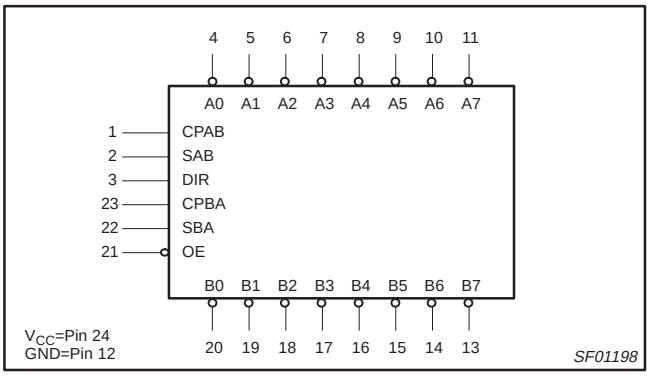
PIN CONFIGURATION – 74F649



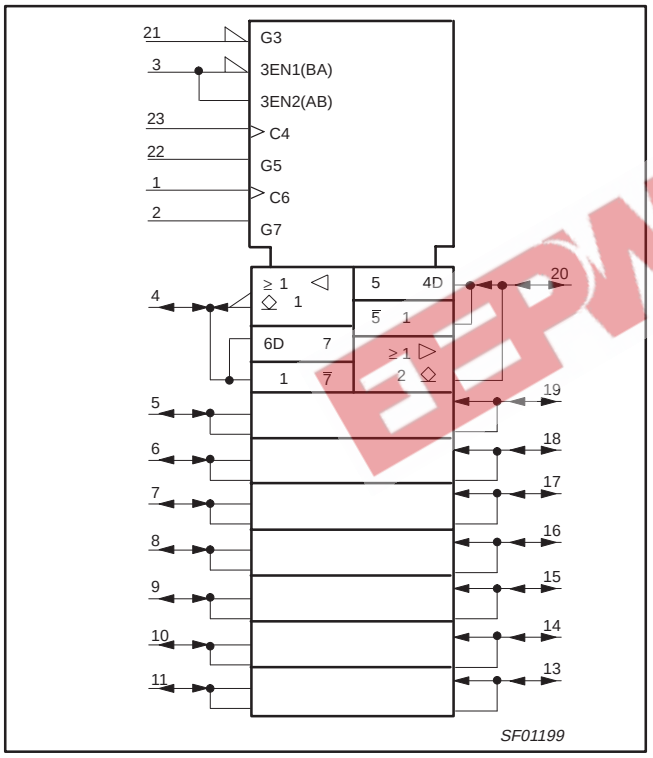
LOGIC SYMBOL – 74F647



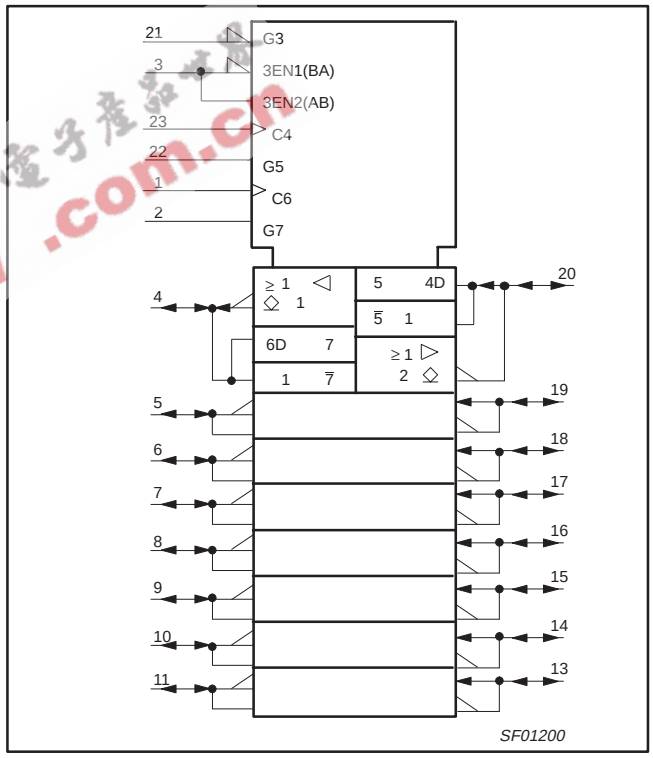
LOGIC SYMBOL – 74F649

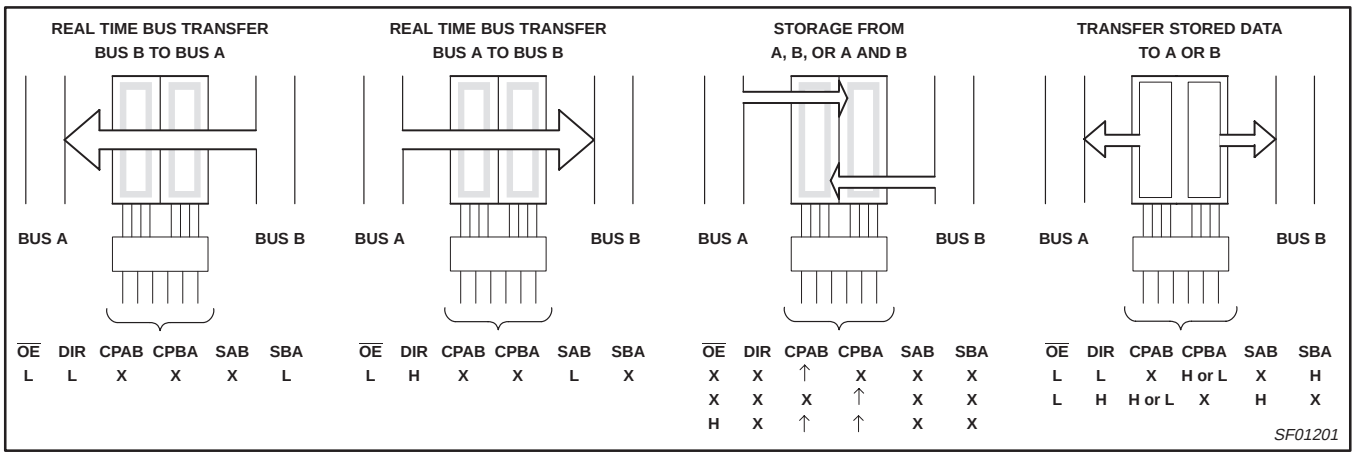


LOGIC SYMBOL – 74F647



LOGIC SYMBOL – 74F648





INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 - A7	A inputs	1.0/0.033	20µA/20µA
B0 - B7	B inputs	1.0/0.033	20µA/20µA
CPAB	A-to-B clock input	1.0/0.033	20µA/20µA
CPBA	B-to-A clock input	1.0/0.033	20µA/20µA
SAB	A-to-B select input	1.0/0.033	20µA/20µA
SBA	B-to-A select input	1.0/0.033	20µA/20µA
DIR	Data flow Directional control enable input	1.0/0.066	20µA/20µA
$\overline{OE}$	Output Enable input	1.0/0.066	20µA/20µA
A0 - A7	A outputs	OC/106.7	OC/64mA
B0 - B7	B outputs	OC/106.7	OC/64mA

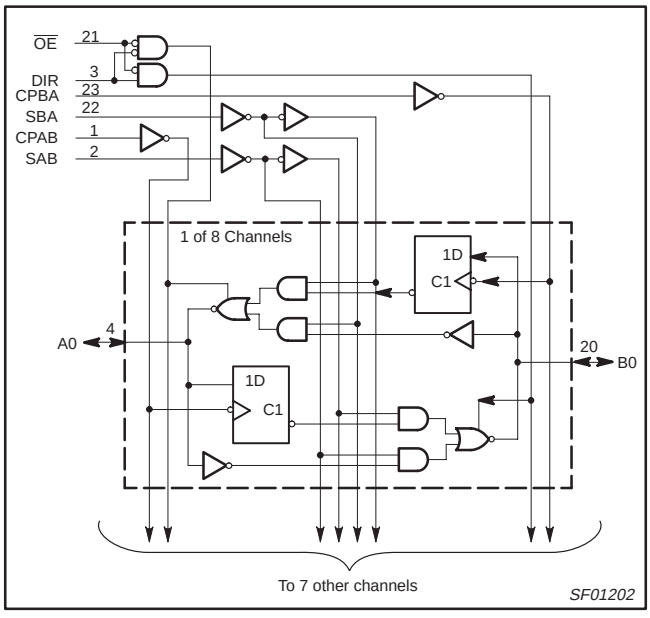
NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state. OC = Open Collector

FUNCTION TABLE

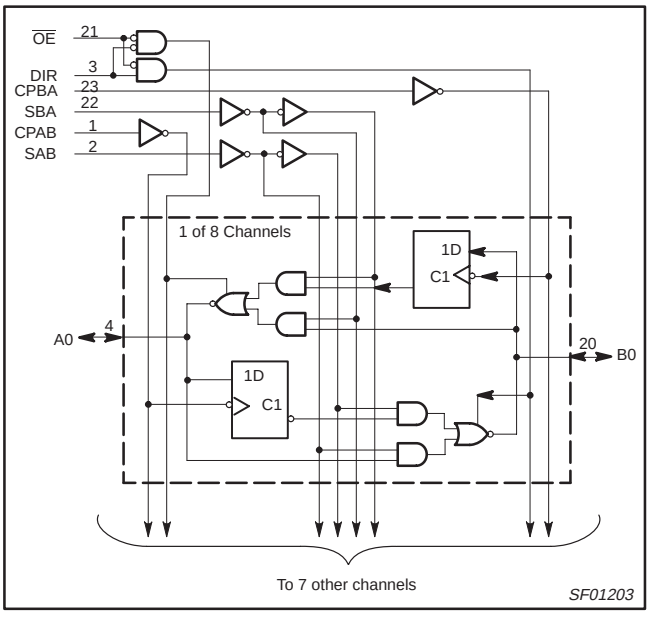
INPUTS						DATA I/O		OPERATING MODE	
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	A0-A7	B0-B7		
X	X	↑	X	X	X	Input	Unspecified*	Store A, B unspecified*	Store A, B unspecified*
X	X	X	↑	X	X	Unspecified*	Input	Store B, A unspecified*	Store B, A unspecified*
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus	Real time B data to A bus Stored B data to A bus
L L	H H	H or L X	X X	L H	X X	Input	Output	Real time A data to B bus Stored A data to B bus	Real time A data to B bus Stored A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* = The data output function may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

LOGIC DIAGRAM – 74F647



LOGIC DIAGRAM – 74F649



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			64	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX					250	µA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL} = 48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL} = 64mA	±5%V_{CC}		0.42	0.55	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage	Others	V_{CC} = 0.0, V_I = 7.0V					100	µA
		An, Bn	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				105	145	mA
		I_{CCL}					145	200	mA

NOTES:
1. For conditions shown as MIN or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	50	65		40		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB to Bn or CPBA or An	Waveform 1	7.0 5.5	12.0 8.5	15.0 11.0	7.0 5.5	16.5 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 2 Waveform 3	7.5 4.0	10.5 7.0	13.5 9.5	7.5 4.0	16.0 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay SBA to An or SAB to Bn	Waveform 2 Waveform 3	7.5 4.0	11.5 7.0	14.5 9.5	7.5 4.0	17.0 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to An or Bn	Waveform 2 Waveform 3	9.0 6.5	13.0 10.0	16.0 12.5	9.0 6.5	18.5 13.5	ns ns
t_{PLH} t_{PHL}	Propagation delay DIR to An or Bn	Waveform 2 Waveform 3	9.0 7.0	13.0 15.0	16.0 18.0	9.0 7.0	18.5 20.0	ns ns

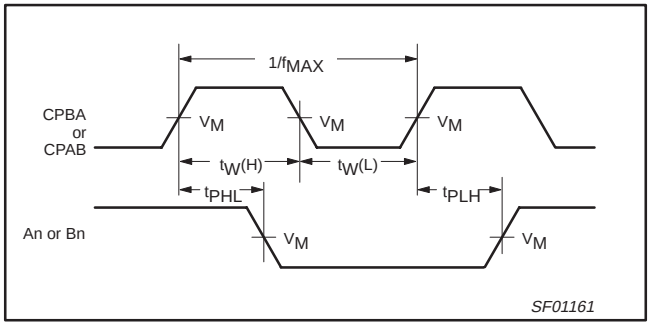
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low An to CPBA or Bn to CPAB	Waveform 4	4.0 4.0			5.0 5.0		ns ns
t_s(H) t_s(L)	Hold time, High or Low An to CPBA or Bn to CPAB	Waveform 4	0 0			0 0		ns ns
t_w(H) t_w(L)	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.5 6.0			4.5 6.5		ns ns

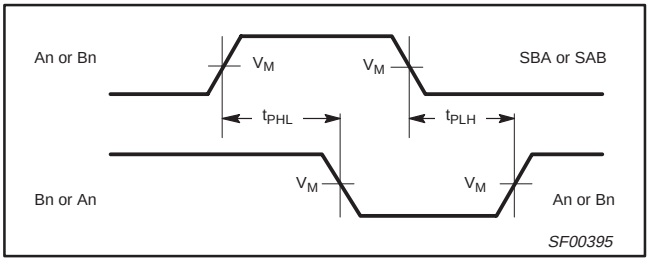
AC WAVEFORMS

For all waveforms, V_M = 1.5V

The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

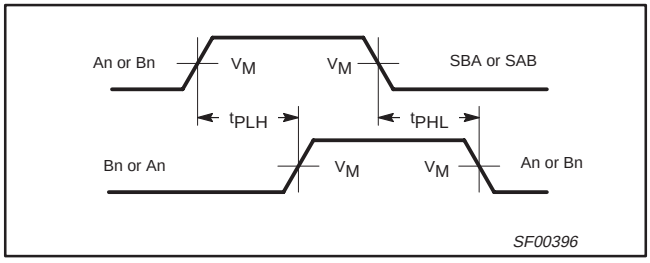


Waveform 2. Propagation Delay, An to Bn or Bn to An and SBA to An or SAB to Bn

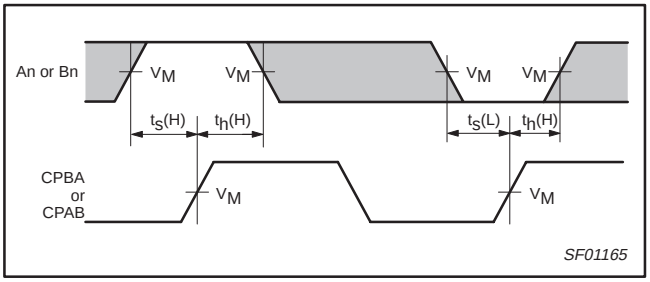
AC WAVEFORMS (Continued)

For all waveforms, V_M = 1.5V

The shaded areas indicate when the input is permitted to change for predictable output performance.

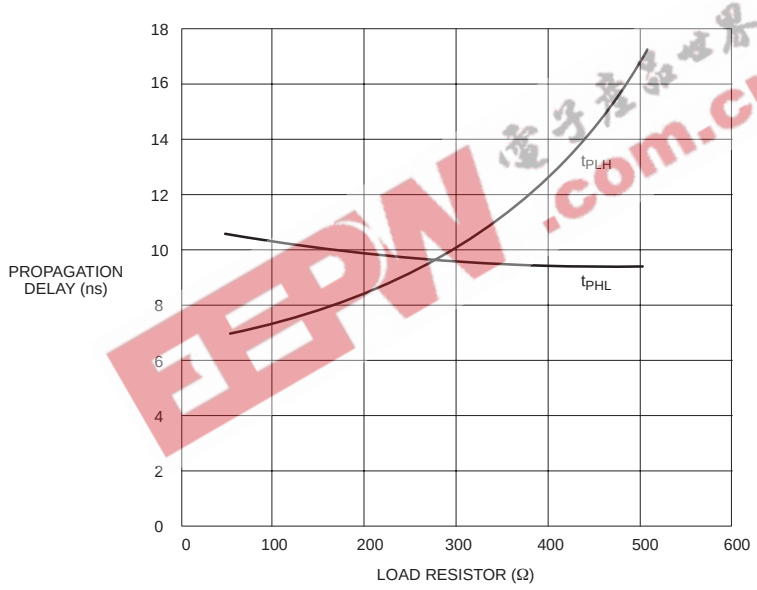


Waveform 3. Propagation Delay, An to Bn or Bn to An and SBA to An or SAB to Bn



Waveform 4. Data Setup and Hold Times

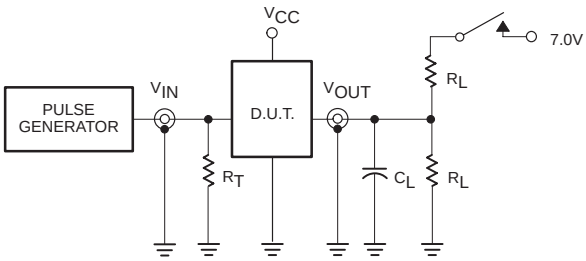
TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



NOTE:

When using open-collector part, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only slight increase in the t_{PHL}. However, if the pull-up resistor is changed, the user must take certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers do not exceed the I_{OL} maximum specification.

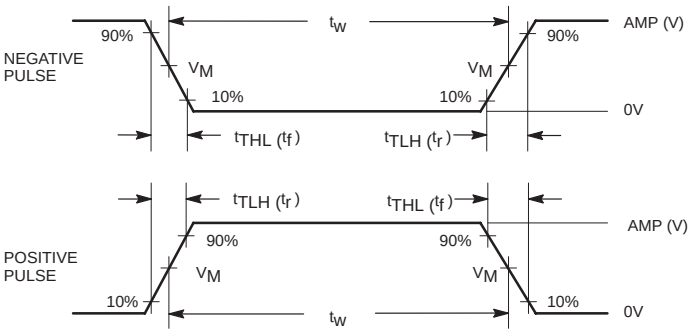
TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Outputs

SWITCH POSITION

TEST	SWITCH
Open Collector	closed
All other	open



Input Pulse Definition

DEFINITIONS:

R_L = Load resistor;
see AC electrical characteristics for value.

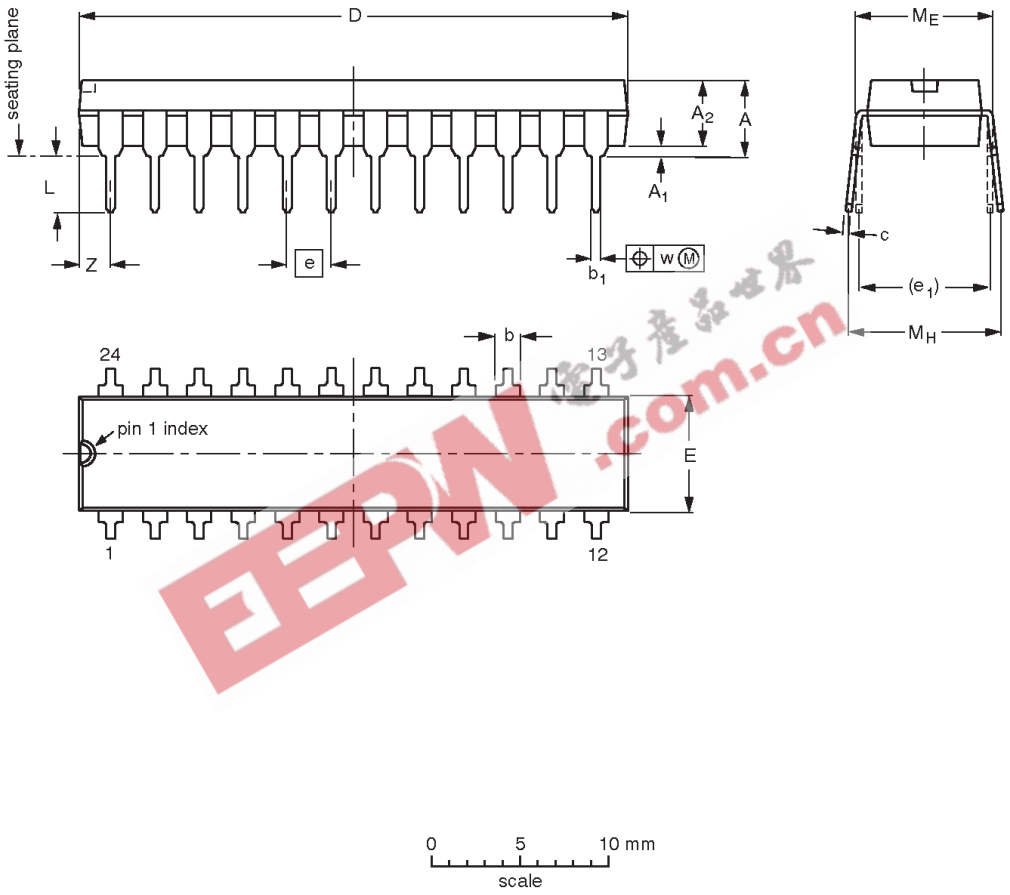
C_L = Load capacitance includes jig and probe capacitance;
see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00195

DIP24: plastic dual in-line package; 24 leads (300 mil) SOT222-1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

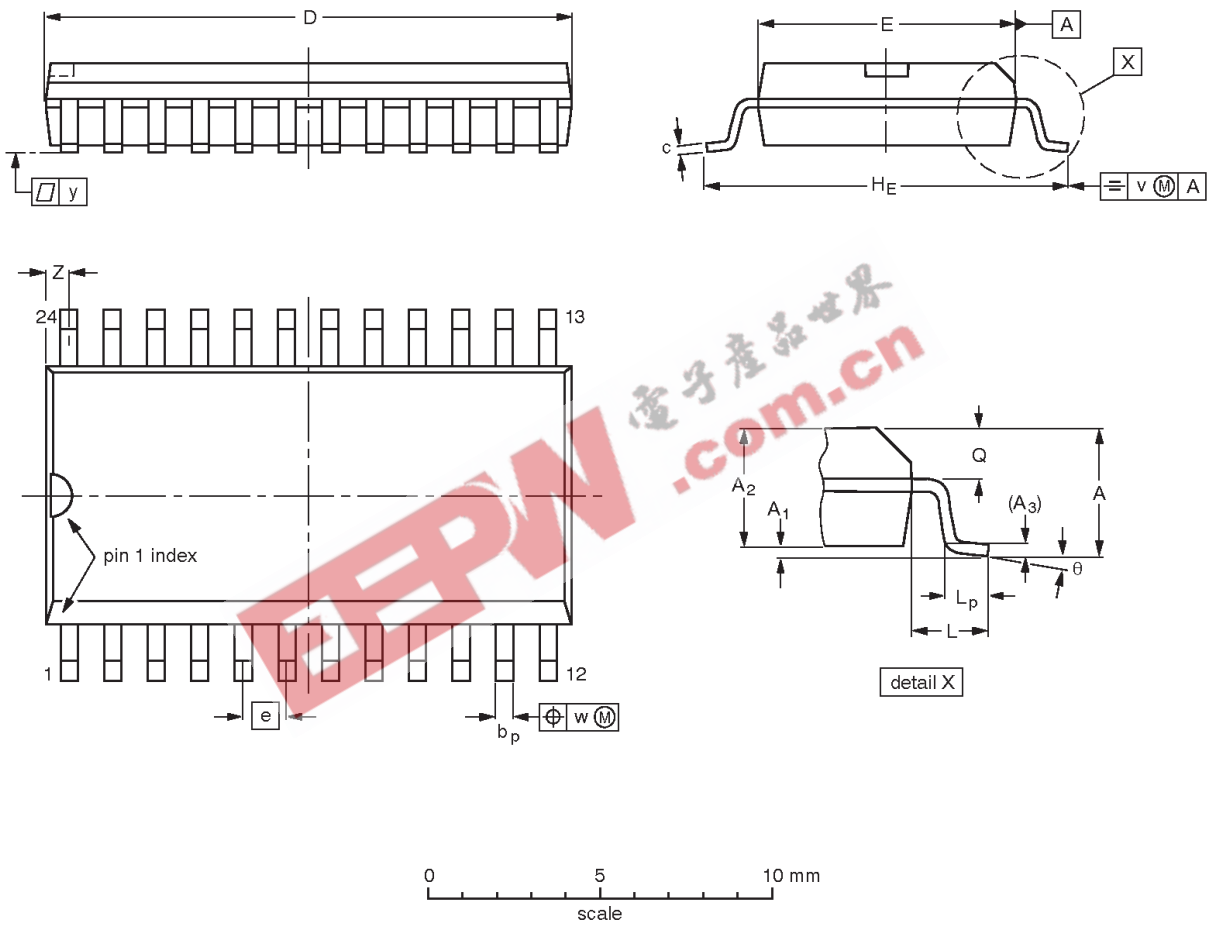
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

NOTES

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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