FAIRCHILD SEMICONDUCTOR®

June 1993
Revised February 2005

74VHC14
Hex Schmitt Inverter

General Description

The VHC14 is an advanced high speed CMOS Hex Schmitt Inverter fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. Pin configuration and function are the same as the VHC04 but the inputs have hysteresis between the positive-going and negative-going input thresholds, which are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals, thus providing greater noise margin than conventional inverters.

An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High Speed: t_{PD} = 5.5 ns (typ) at V_{CC} = 5V
- Low power dissipation: I_{CC} = 2 μA (Max) at T_A = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min)
- Power down protection is provided on all inputs
- Low noise: V_{OLP} = 0.8V (Max)
- Pin and function compatible with 74HC14

Ordering Code:

Order Number	Package Number	Package Description
74VHC14M (Note 1)	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC14MX_NL (Note 2)	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC14SJ (Note 1)	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC14MTC (Note 1)	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC14MTC_NL (Note 3)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC14MTCX_NL (Note 2)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC14N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Pb-Free package per JEDEC J-STD-020B.

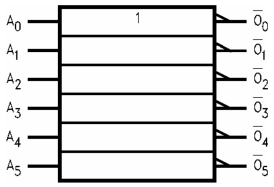
Note 1: Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Note 2: "_NL" indicates Pb-Free product (per JEDEC J-STD-020B). Device is available in Tape and Reel only.

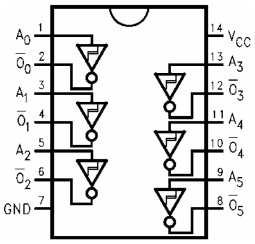
Note 3: "_NL" indicates Pb-Free product (per JEDEC J-STD-020B).

Logic Symbol

IEEE/IEC



Connection Diagram



Pin Descriptions

Pin Names	Description
A_n	Inputs
$\overline{O}_n$	Outputs

Truth Table

A	O
L	H
H	L

Absolute Maximum Ratings (Note 4)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L)	
Soldering (10 seconds)	260°C

Recommended Operating Conditions (Note 5)

Supply Voltage (V_{CC})	+2.0V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	−40°C to +85°C

Note 4: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. The data book specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 5: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	T_A = 25°C			T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_P	Positive Threshold Voltage	3.0			2.20		2.20	V		
		4.5			3.15		3.15			
		5.5			3.85		3.85			
V_N	Negative Threshold Voltage	3.0	0.90			0.90		V		
		4.5	1.35			1.35				
		5.5	1.65			1.65				
V_H	Hysteresis Voltage	3.0	0.30		1.20	0.30	1.20	V		
		4.5	0.40		1.40	0.40	1.40			
		5.5	0.50		1.60	0.50	1.60			
V_{OH}	HIGH Level Output Voltage	2.0	1.9	2.0		1.9		V	V_{IN} = V_{IL}	I_{OH} = −50 μA
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		3.0	2.58			2.48		V		I_{OH} = −4 mA
		4.5	3.94			3.80				I_{OH} = −8 mA
V_{OL}	LOW Level Output Voltage	2.0		0.0	0.1		0.1	V	V_{IN} = V_{IH}	I_{OL} = 50 μA
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44	V		I_{OL} = 4 mA
		4.5			0.36		0.44			I_{OL} = 8 mA
I_{IN}	Input Leakage Current	0–5.5			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			2.0		20.0	μA	V_{IN} = V_{CC} or GND	

Noise Characteristics

Symbol	Parameter	V_{CC}	T_A = 25°C		Units	Conditions
			Typ	Limits		
V_{OLP} (Note 6)	Quiet Output Maximum Dynamic V_{OL}	5.0	0.4	0.8	V	C_L = 50 pF
V_{OLV} (Note 6)	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.4	−0.8	V	C_L = 50 pF
V_{IHD} (Note 6)	Minimum HIGH Level Dynamic Input Voltage	5.0		3.5	V	C_L = 50 pF
V_{ILD} (Note 6)	Maximum LOW Level Dynamic Input Voltage	5.0		1.5	V	C_L = 50 pF

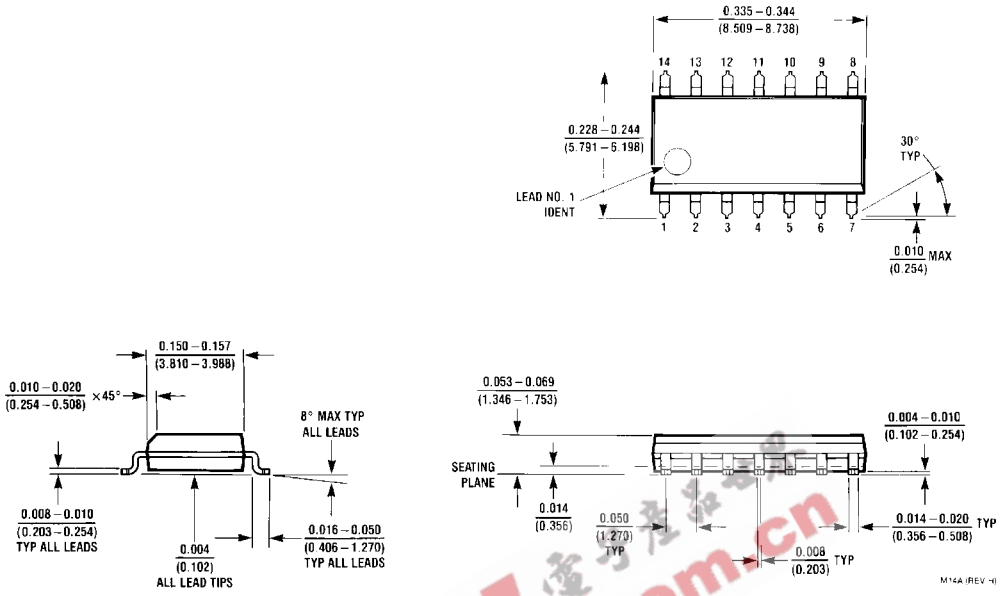
Note 6: Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}	$T_A = 25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3 ± 0.3		8.3	12.8	1.0	15.0	ns	$C_L = 15$ pF
t_{PHL}	Time			10.8	16.3	1.0	18.5		$C_L = 50$ pF
		5.0 ± 0.5		5.5	8.6	1.0	10.0	ns	$C_L = 15$ pF
				7.0	10.6	1.0	12.0		$C_L = 50$ pF
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open
C_{PD}	Power Dissipation Capacitance			21				pF	(Note 7)

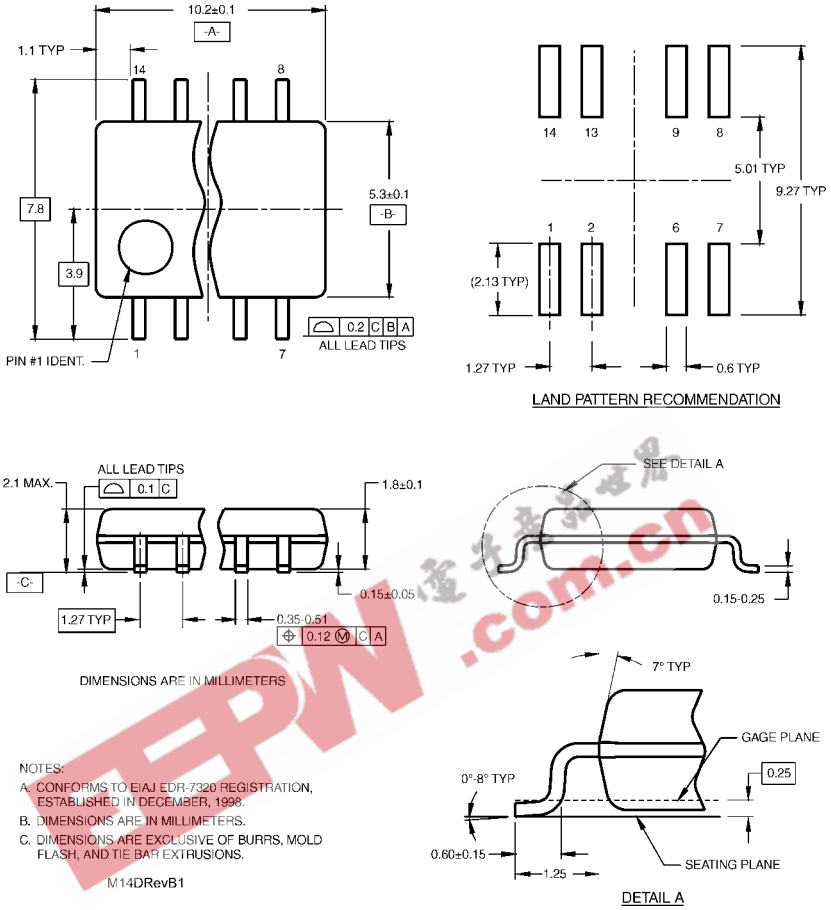
Note 7: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (Opr) = $C_{PD} * V_{CC} * f_{IN} + I_{CC}/6$ (per Gate)

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

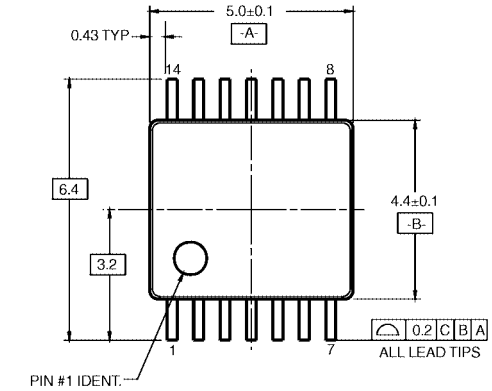
B. DIMENSIONS ARE IN MILLIMETERS.

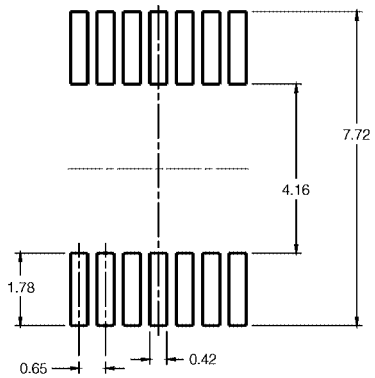
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

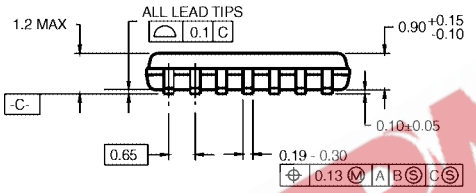
Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

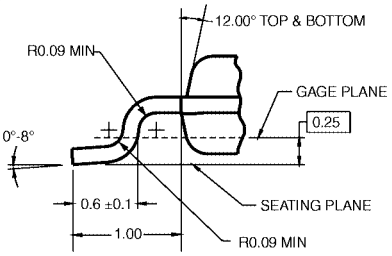
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)





LAND PATTERN RECOMMENDATION





DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

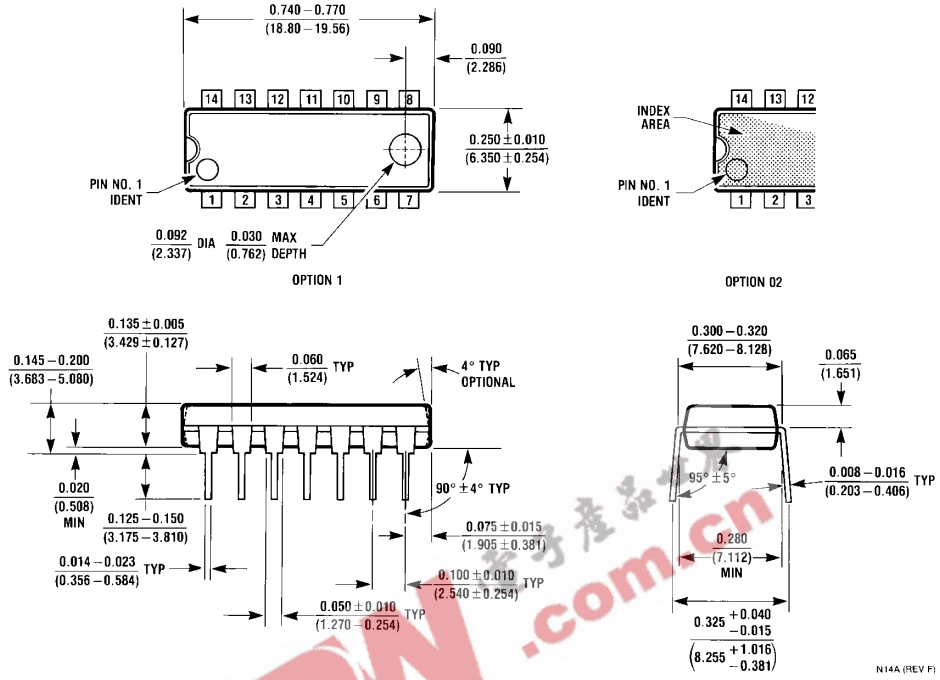
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC14RevC3

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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