# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## 74HC/HCT107
## Dual JK flip-flop with reset; negative-edge trigger

Product specification

File under Integrated Circuits, IC06

December 1990

**PHILIPS**

# Dual JK flip-flop with reset; negative-edge trigger

**74HC/HCT107**

## FEATURES

- Output capability: standard
- $I_{CC}$ category: flip-flops

## GENERAL DESCRIPTION

The 74HC/HCT107 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT107 are dual negative-edge triggered JK-type flip-flops featuring individual J, K, clock ($n\overline{CP}$) and reset ($n\overline{R}$) inputs; also complementary Q and $\overline{Q}$ outputs.

The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation.

The reset ($n\overline{R}$) is an asynchronous active LOW input. When LOW, it overrides the clock and data inputs, forcing the Q output LOW and the $\overline{Q}$ output HIGH.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

## QUICK REFERENCE DATA

GND = 0 V; $T_{amb}$ = 25 °C; $t_r$ = $t_f$ = 6 ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|---|---|---|---|---|---|
| | | | HC | HCT | |
| $t_{PHL}$/ $t_{PLH}$ | propagation delay<br>$\quad$ $n\overline{CP}$ to nQ<br>$\quad$ $n\overline{CP}$ to $n\overline{Q}$<br>$\quad$ $n\overline{R}$ to nQ, $n\overline{Q}$ | $C_L$ = 15 pF;<br>$V_{CC}$ = 5 V | 16<br>16<br>16 | 16<br>18<br>17 | ns<br>ns<br>ns |
| $f_{max}$ | maximum clock frequency | | 78 | 73 | MHz |
| $C_I$ | input capacitance | | 3.5 | 3.5 | pF |
| $C_{PD}$ | power dissipation<br>$\quad$ capacitance per flip-flop | notes 1 and 2 | 30 | 30 | pF |

### Notes

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW):

   $$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma \ (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

   $f_i$ = input frequency in MHz

   $f_o$ = output frequency in MHz

   $\Sigma \ (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   $C_L$ = output load capacitance in pF

   $V_{CC}$ = supply voltage in V

2. For HC $\quad$ the condition is $V_I$ = GND to $V_{CC}$
   For HCT the condition is $V_I$ = GND to $V_{CC}$ − 1.5 V.
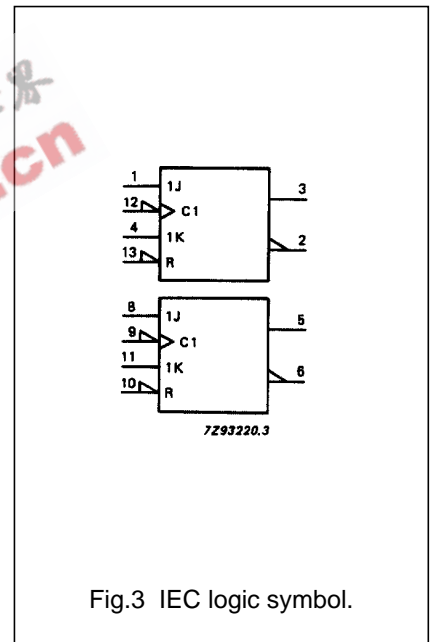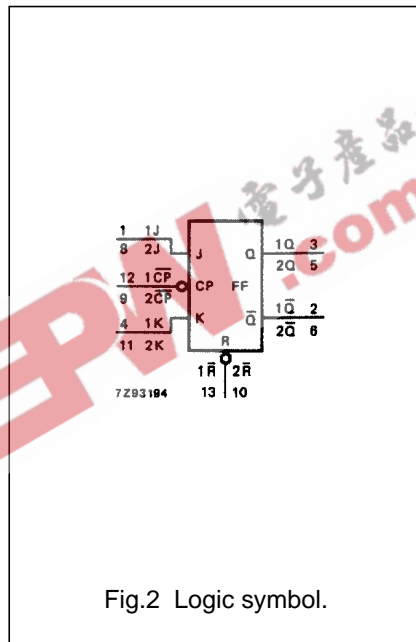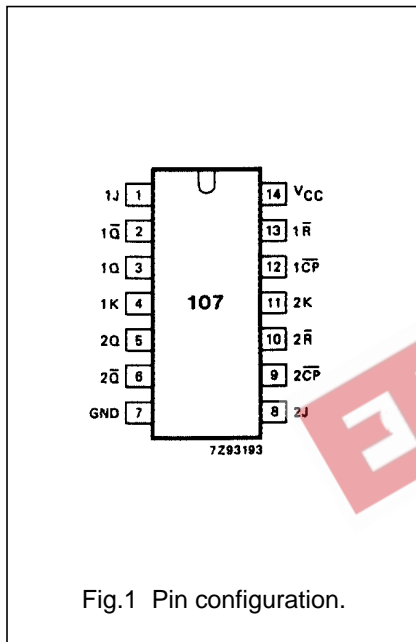
## ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

## Dual JK flip-flop with reset; negative-edge trigger 74HC/HCT107

**PIN DESCRIPTION**

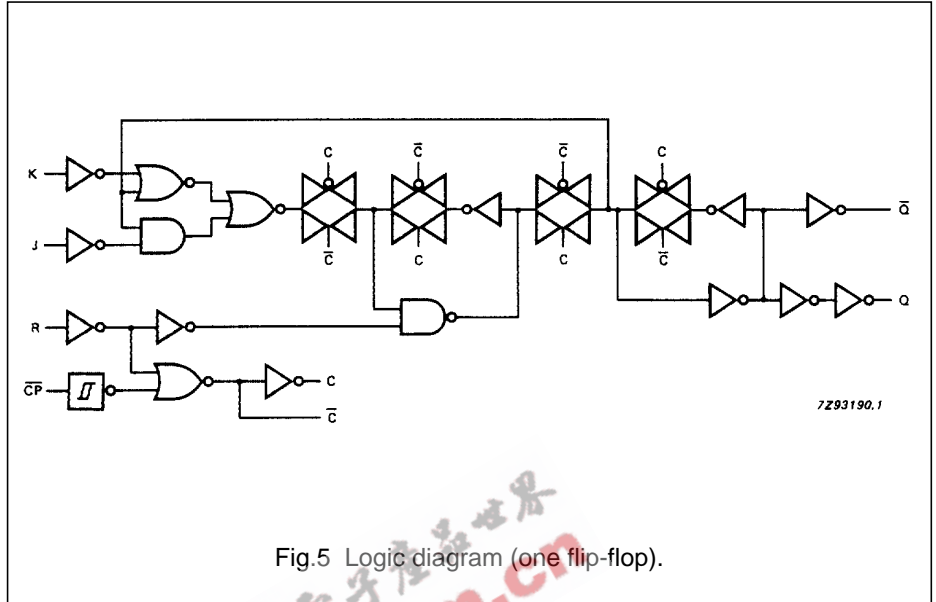| PIN NO. | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 1, 8, 4, 11 | 1J, 2J, 1K, 2K | synchronous inputs; flip-flops 1 and 2 |
| 2, 6 | 1$\overline{Q}$, 2$\overline{Q}$ | complement flip-flop outputs |
| 3, 5 | 1Q, 2Q | true flip-flop outputs |
| 7 | GND | ground (0 V) |
| 12, 9 | 1$\overline{CP}$, 2$\overline{CP}$ | clock input (HIGH-to-LOW, edge-triggered) |
| 13, 10 | 1$\overline{R}$, 2$\overline{R}$ | asynchronous reset inputs (active LOW) |
| 14 | $V_{CC}$ | positive supply voltage |



Fig.1 Pin configuration.



Fig.2 Logic symbol.



Fig.3 IEC logic symbol.

## Dual JK flip-flop with reset; negative-edge trigger

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Fig.4  Functional diagram.

Fig.5  Logic diagram (one flip-flop).
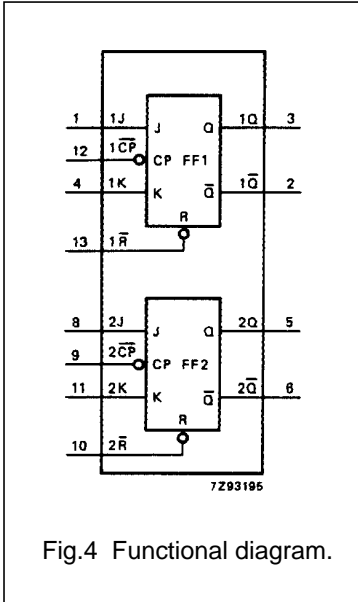
**FUNCTION TABLE**

| OPERATING MODE | INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| | $n\overline{R}$ | $n\overline{CP}$ | J | K | Q | $\overline{Q}$ |
| asynchronous reset | L | X | X | X | L | H |
| toggle | H | ↓ | h | h | $\overline{q}$ | q |
| load "0" (reset) | H | ↓ | l | h | L | H |
| load "1" (set) | H | ↓ | h | l | H | L |
| hold "no change" | H | ↓ | l | l | q | $\overline{q}$ |

**Note**

1.  H = HIGH voltage level

    h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition

    L = LOW voltage level

    l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition

    q = lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW CP transition

    X = don't care

    ↓ = HIGH-to-LOW CP transition

## Dual JK flip-flop with reset; negative-edge trigger

## 74HC/HCT107

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
$I_{CC}$ category: flip-flops

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | $V_{CC}$ (V) | WAVEFORMS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | **74HC** | | | | | | | | | |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $t_{PHL}/t_{PLH}$ | propagation delay n$\overline{CP}$ to nQ | | 52 19 15 | 160 32 27 | | 200 40 34 | | 240 48 41 | ns | 2.0 4.5 6.0 | Fig.6 |
| $t_{PHL}/t_{PLH}$ | propagation delay n$\overline{CP}$ to n$\overline{Q}$ | | 52 19 15 | 160 32 27 | | 200 40 34 | | 240 48 41 | ns | 2.0 4.5 6.0 | Fig.6 |
| $t_{PHL}/t_{PLH}$ | propagation delay n$\overline{R}$ to nQ, n$\overline{Q}$ | | 52 19 15 | 155 31 26 | | 195 39 33 | | 235 47 40 | ns | 2.0 4.5 6.0 | Fig.7 |
| $t_{THL}/t_{TLH}$ | output transition time | | 19 7 6 | 75 15 13 | | 95 19 16 | | 110 22 19 | ns | 2.0 4.5 6.0 | Fig.6 |
| $t_W$ | clock pulse width HIGH or LOW | 80 16 14 | 22 8 6 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.6 |
| $t_W$ | reset pulse width LOW | 80 16 14 | 22 8 6 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.7 |
| $t_{rem}$ | removal time n$\overline{R}$ to n$\overline{CP}$ | 60 12 10 | 19 7 6 | | 75 15 13 | | 90 18 15 | | ns | 2.0 4.5 6.0 | Fig.7 |
| $t_{su}$ | set-up time nJ, nK to n$\overline{CP}$ | 100 20 17 | 22 8 6 | | 125 25 21 | | 150 30 26 | | ns | 2.0 4.5 6.0 | Fig.6 |
| $t_h$ | hold time nJ, nK to n$\overline{CP}$ | 3 3 3 | −6 −2 −2 | | 3 3 3 | | 3 3 3 | | ns | 2.0 4.5 6.0 | Fig.6 |
| $f_{max}$ | maximum clock pulse frequency | 6.0 30 35 | 23 70 85 | | 4.8 24 28 | | 4.0 20 24 | | MHz | 2.0 4.5 6.0 | Fig.6 |

## Dual JK flip-flop with reset; negative-edge trigger

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### DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
$I_{CC}$ category: flip-flops

### Note to HCT types

The value of additional quiescent supply current ($\Delta I_{CC}$) for a unit load of 1 is given in the family specifications.
To determine $\Delta I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|---|---|
| nK | 0.60 |
| n$\overline{R}$ | 0.65 |
| n$\overline{CP}$, nJ | 1.00 |

### AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_f = t_f$ = 6 ns; $C_L$ = 50 pF

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HCT | | | | | | | | $V_{CC}$ (V) | WAVEFORMS |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $t_{PHL}$/ $t_{PLH}$ | propagation delay n$\overline{CP}$ to nQ | | 19 | 36 | | 45 | | 54 | ns | 4.5 | Fig.6 |
| $t_{PHL}$/ $t_{PLH}$ | propagation delay n$\overline{CP}$ to n$\overline{Q}$ | | 21 | 36 | | 45 | | 54 | ns | 4.5 | Fig.6 |
| $t_{PHL}$/ $t_{PLH}$ | propagation delay n$\overline{R}$ to nQ, n$\overline{Q}$ | | 20 | 38 | | 48 | | 57 | ns | 4.5 | Fig.7 |
| $t_{THL}$/ $t_{TLH}$ | output transition time | | 7 | 15 | | 19 | | 22 | ns | 4.5 | Fig.6 |
| $t_W$ | clock pulse width HIGH or LOW | 16 | 9 | | 20 | | 24 | | ns | 4.5 | Fig.6 |
| $t_W$ | reset pulse width LOW | 20 | 11 | | 25 | | 30 | | ns | 4.5 | Fig.7 |
| $t_{rem}$ | removal time n$\overline{R}$ to n$\overline{CP}$ | 14 | 8 | | 18 | | 21 | | ns | 4.5 | Fig.7 |
| $t_{su}$ | set-up time nJ, nK to n$\overline{CP}$ | 20 | 7 | | 25 | | 30 | | ns | 4.5 | Fig.6 |
| $t_h$ | hold time nJ, nK to n$\overline{CP}$ | 5 | −2 | | 5 | | 5 | | ns | 4.5 | Fig.6 |
| $f_{max}$ | maximum clock pulse frequency | 30 | 66 | | 24 | | 20 | | MHz | 4.5 | Fig.6 |

## Dual JK flip-flop with reset; negative-edge trigger

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### AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
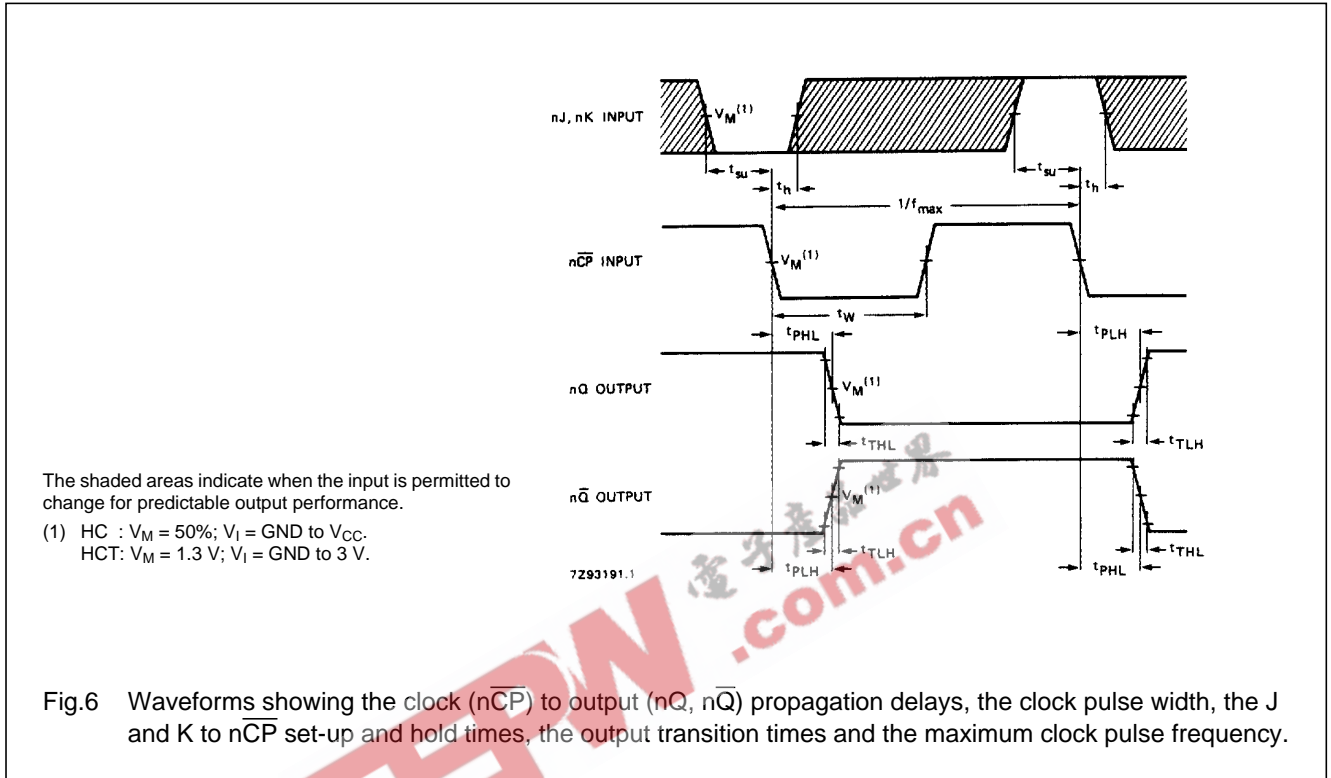    HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.6  Waveforms showing the clock (n$\overline{CP}$) to output (nQ, n$\overline{Q}$) propagation delays, the clock pulse width, the J and K to n$\overline{CP}$ set-up and hold times, the output transition times and the maximum clock pulse frequency.
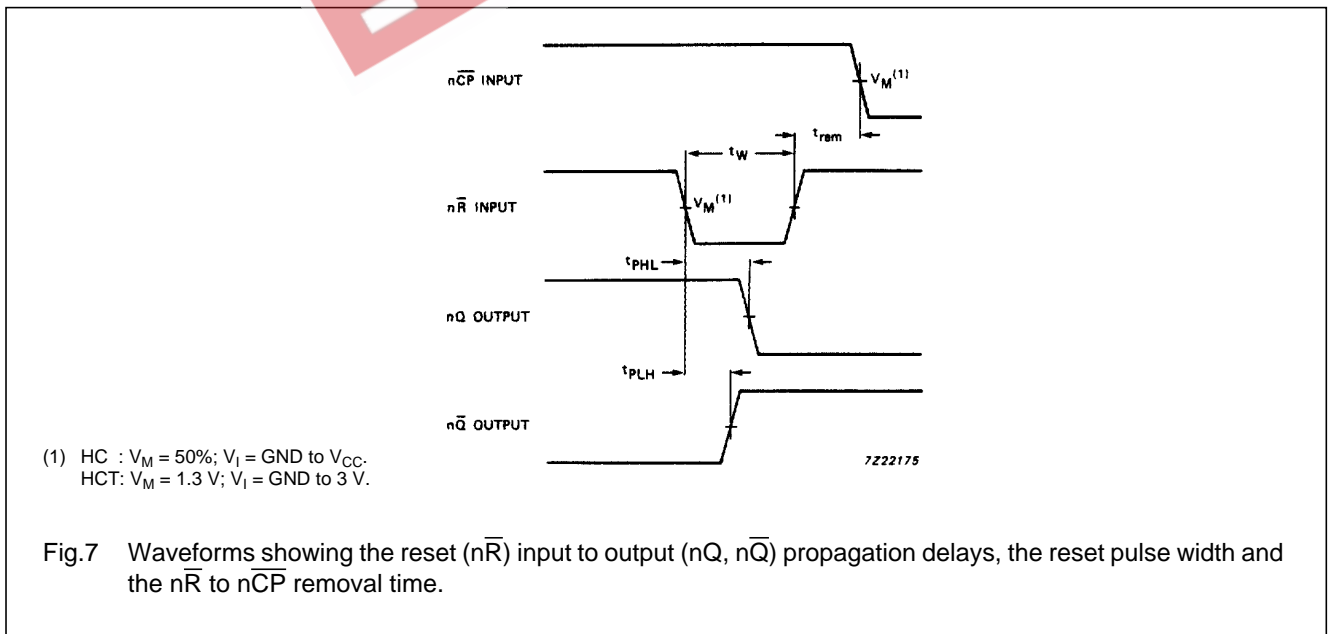
(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
    HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.7  Waveforms showing the reset (n$\overline{R}$) input to output (nQ, n$\overline{Q}$) propagation delays, the reset pulse width and the n$\overline{R}$ to n$\overline{CP}$ removal time.

### PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.