

54ACT/74ACT534 Octal D Flip-Flop with TRI-STATE® Outputs

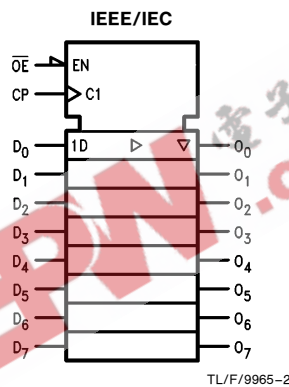
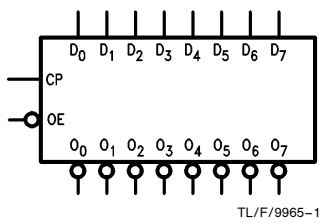
General Description

The 'ACT534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (\overline{OE}) are common to all flip-flops. The 'ACT534 is the same as the 'ACT374 except that the outputs are inverted.

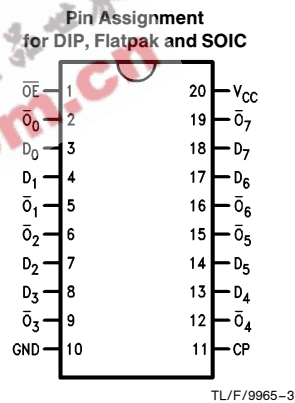
Features

- I_{CC} and I_{OZ} reduced by 50%
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT534 has TTL-compatible inputs
- Inverted output version of 'ACT374

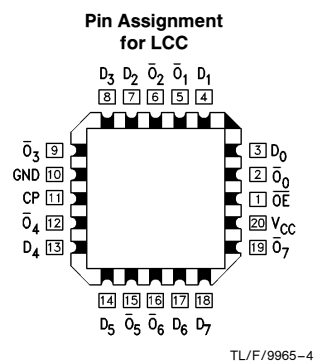
Logic Symbols



Connection Diagrams



| Pin Names | Description |
|-------------------------------------|---------------------------------|
| D ₀ -D ₇ | Data Inputs |
| CP | Clock Pulse Input |
| \overline{OE} | TRI-STATE Output Enable Input |
| \overline{O}_0 - \overline{O}_7 | Complementary TRI-STATE Outputs |



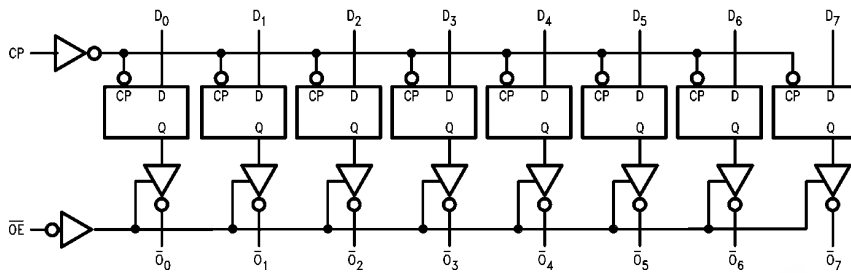
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Functional Description

The 'ACT534 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP)

transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

Logic Diagram



TL/F/9965-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

| Inputs | | | Output |
|--------|----|---|------------------|
| CP | OE | D | \overline{O} |
| — | L | H | L |
| — | L | L | H |
| L | L | X | \overline{O}_0 |
| X | H | X | Z |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

— = LOW-to-HIGH Clock Transition

Z = High Impedance

\overline{O}_0 = Value stored from previous clock cycle

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|--------------------------|
| Supply Voltage (V_{CC}) | -0.5V to +7.0V |
| DC Input Diode Current (I_{IK}) | |
| $V_I = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | +20 mA |
| DC Input Voltage (V_I) | -0.5V to $V_{CC} + 0.5V$ |
| DC Output Diode Current (I_{OK}) | |
| $V_O = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | +20 mA |
| DC Output Voltage (V_O) | -0.5V to $V_{CC} + 0.5V$ |
| DC Output Source or Sink Current (I_O) | ± 50 mA |
| DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) | ± 50 mA |
| Storage Temperature (T_{STG}) | -65°C to +150°C |
| Junction Temperature (T_J) | |
| CDIP | 175°C |
| PDIP | 140°C |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

| | |
|---|-----------------|
| Supply Voltage (V_{CC}) | 4.5V to 5.5V |
| 'ACT | |
| Input Voltage (V_I) | 0V to V_{CC} |
| Output Voltage (V_O) | 0V to V_{CC} |
| Operating Temperature (T_A) | |
| 74ACT | -40°C to +85°C |
| 54ACT | -55°C to +125°C |
| Minimum Input Edge Rate ($\Delta V/\Delta t$) | |
| 'ACT Devices | |
| V_{IN} from 0.8V to 2.0V | |
| V_{CC} @ 4.5V, 5.5V | 125 mV/ns |

DC Characteristics for 'ACT Family Devices

| Symbol | Parameter | V_{CC} (V) | 74ACT | | | 54ACT | | | Units | Conditions | | | |
|-----------|-----------------------------------|-----------------|------------------------------|-------------------|-----------|--|-------------------|--|--|------------|---|-------------------|--|
| | | | $T_A = \pm 25^\circ\text{C}$ | | | $T_A = -55^\circ\text{C to } +125^\circ\text{C}$ | | | | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | | |
| | | | Typ | Guaranteed Limits | | Typ | Guaranteed Limits | | | | Typ | Guaranteed Limits | |
| V_{IH} | Minimum High Level Input Voltage | 4.5 | 1.5 | 2.0 | 2.0 | 2.0 | 2.0 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | | | | |
| | | 5.5 | 1.5 | 2.0 | 2.0 | 2.0 | 2.0 | | | | | | |
| V_{IL} | Maximum Low Level Input Voltage | 4.5 | 1.5 | 0.8 | 0.8 | 0.8 | 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | | | | |
| | | 5.5 | 1.5 | 0.8 | 0.8 | 0.8 | 0.8 | | | | | | |
| V_{OH} | Minimum High Level Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | 4.4 | 4.4 | V | $I_{OUT} = -50 \mu\text{A}$ | | | | |
| | | 5.5 | 5.49 | 5.4 | 5.4 | 5.4 | 5.4 | | | | | | |
| | | 4.5 | | 3.86 | 3.70 | 3.76 | V | $^*V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24 \text{ mA}$ | | | | | |
| | | 5.5 | | 4.86 | 4.70 | 4.76 | | | | | | | |
| V_{OL} | Maximum Low Level Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | 0.1 | 0.1 | V | $I_{OUT} = 50 \mu\text{A}$ | | | | |
| | | 5.5 | 0.001 | 0.1 | 0.1 | 0.1 | | | | | | | |
| | | 4.5 | | 0.36 | 0.50 | 0.44 | V | $^*V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 24 \text{ mA}$ | | | | | |
| | | 5.5 | | 0.36 | 0.50 | 0.44 | | | | | | | |
| I_{IN} | Maximum Input Leakage Current | 5.5 | | ± 0.1 | ± 1.0 | ± 1.0 | μA | $V_I = V_{CC}, \text{GND}$ | | | | | |
| I_{OZ} | Maximum TRI-STATE® Current | 5.5 | | ± 0.25 | ± 5.0 | ± 2.5 | μA | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, \text{GND}$ | | | | | |
| I_{CCT} | Maximum I_{CC}/Input | 5.5 | 0.6 | | 1.6 | 1.5 | mA | $V_I = V_{CC} - 2.1V$ | | | | | |

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACT Family Devices (Continued)

| Symbol | Parameter | V _{CC} (V) | 74ACT | | 54ACT | 74ACT | | Units | Conditions |
|------------------|----------------------------------|---------------------|------------------------|-------------------|----------------------------------|---------------------------------|------|-------|--|
| | | | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | | | |
| | | | Typ | Guaranteed Limits | | | | | |
| I _{OLD} | †Minimum Dynamic Output Current | 5.5 | | | 50 | | 75 | mA | V _{OLD} = 1.65V Max |
| I _{OHD} | | 5.5 | | | -50 | | -75 | mA | V _{OHD} = 3.85V Min |
| I _{CC} | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 80.0 | | 40.0 | μA | V _{IN} = V _{CC} or GND |

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

| Symbol | Parameter | V _{CC} * (V) | 74ACT | | | 54ACT | | 74ACT | | Units |
|------------------|--|-----------------------|--|-----|------|--|------|---|------|-------|
| | | | T _A = +25°C C _L = 50 pF | | | T _A = -55°C to +125°C C _L = 50 pF | | T _A = -40°C to +85°C C _L = 50 pF | | |
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| f _{max} | Maximum Clock Frequency | 5.0 | | 100 | | 85 | | 120 | MHz | |
| t _{PLH} | Propagation Delay CP to Q _n | 5.0 | 2.5 | 6.5 | 11.5 | 1.5 | 14.0 | 2.0 | 12.5 | ns |
| t _{PHL} | Propagation Delay CP to Q _n | 5.0 | 2.0 | 6.0 | 10.5 | 1.5 | 13.0 | 2.0 | 12.0 | ns |
| t _{PZH} | Output Enable Time | 5.0 | 2.5 | 6.5 | 12.0 | 1.5 | 14.0 | 2.0 | 12.5 | ns |
| t _{PZL} | Output Enable Time | 5.0 | 2.0 | 6.0 | 11.0 | 1.5 | 13.0 | 2.0 | 11.5 | ns |
| t _{PHZ} | Output Disable Time | 5.0 | 1.5 | 7.0 | 12.5 | 1.5 | 14.5 | 1.0 | 13.5 | ns |
| t _{PLZ} | Output Disable Time | 5.0 | 1.5 | 5.5 | 10.5 | 1.5 | 11.5 | 1.0 | 10.5 | ns |

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

| Symbol | Parameter | V _{CC} * (V) | 74ACT | | 54ACT | 74ACT | | Units |
|----------------|--|-----------------------|--|--------------------|--|---|-----|-------|
| | | | T _A = +25°C C _L = 50 pF | | T _A = -55°C to +125°C C _L = 50 pF | T _A = -40°C to +85°C C _L = 50 pF | | |
| | | | Typ | Guaranteed Minimum | | | | |
| t _s | Setup Time, HIGH or LOW D _n to CP | 5.0 | 1.0 | 3.5 | 5.0 | | 4.0 | ns |
| t _h | Hold Time, HIGH or LOW D _n to CP | 5.0 | -1.0 | 1.0 | 3.0 | | 1.5 | ns |
| t _w | CP Pulse Width HIGH or LOW | 5.0 | 2.0 | 3.5 | 5.0 | | 3.5 | ns |

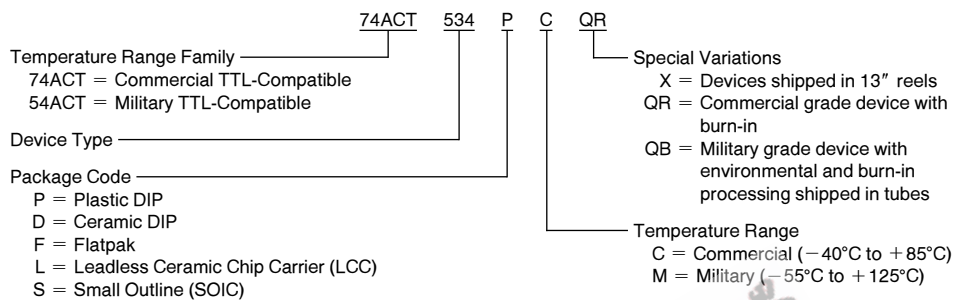
*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

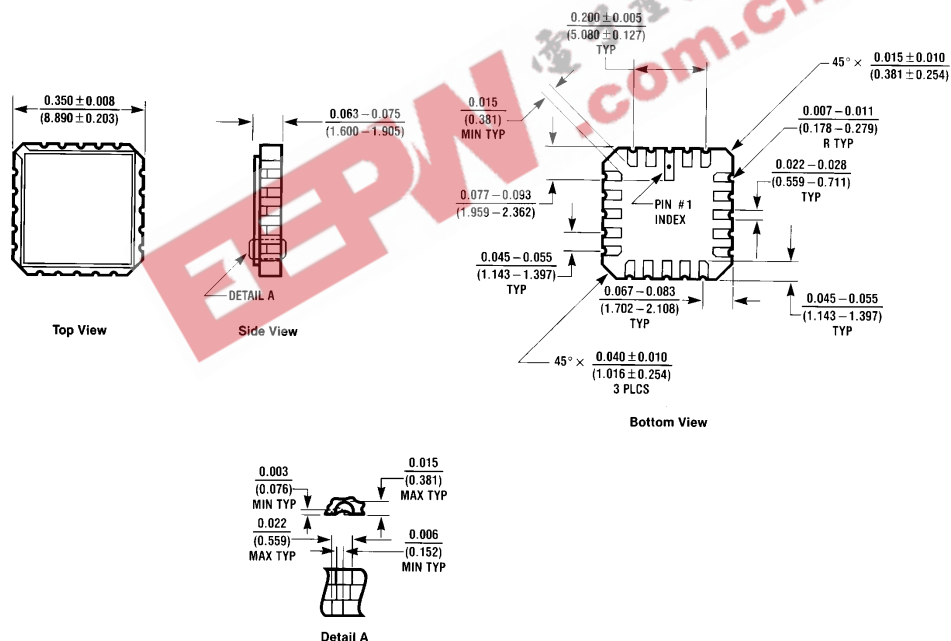
| Symbol | Parameter | Typ | Units | Conditions |
|----------|-------------------------------|------|-------|-----------------|
| C_{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = OPEN$ |
| C_{PD} | Power Dissipation Capacitance | 40.0 | pF | $V_{CC} = 5.0V$ |

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



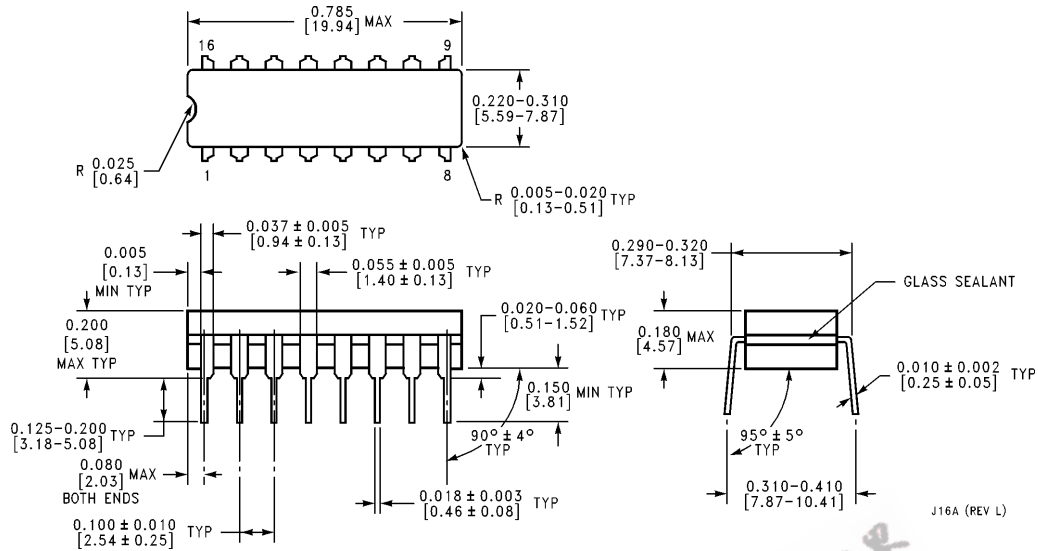
Physical Dimensions inches (millimeters)



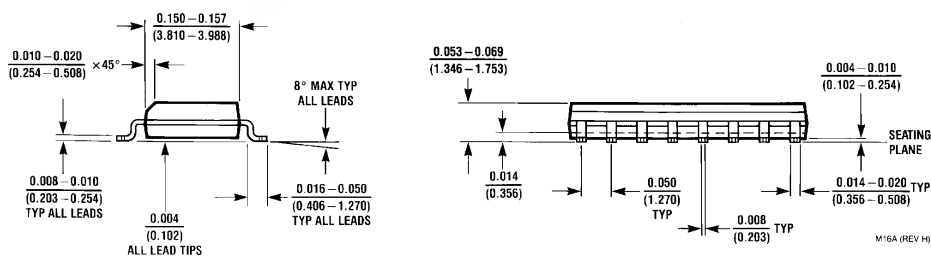
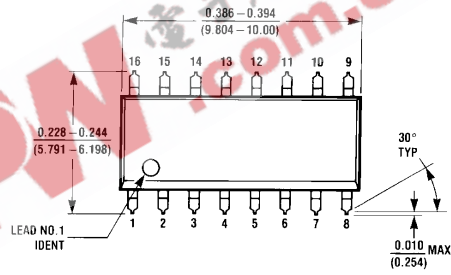
20 Terminal Ceramic Leadless Chip Carrier (L)
 NS Package Number E20A

E20A (REV D)

Physical Dimensions inches (millimeters) (Continued)

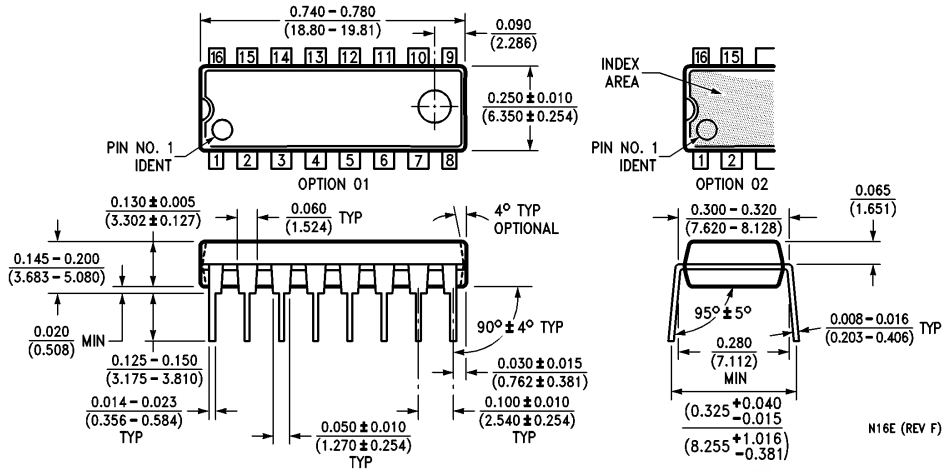


16 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A



16 Lead Small Outline Integrated Circuit (S)
NS Package Number M16A

Physical Dimensions inches (millimeters) (Continued)

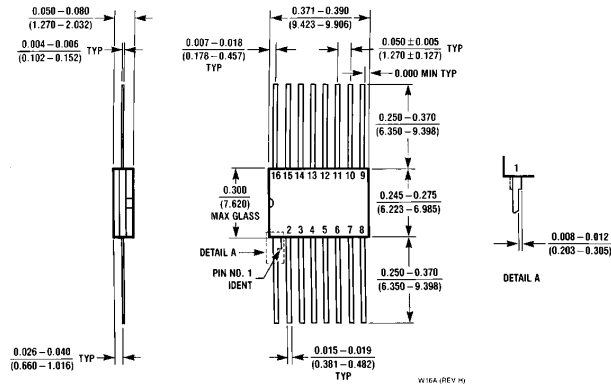


16 Lead Plastic Dual-In-Line Package (P)
NS Package Number N16E

N16E (REV F)

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Physical Dimensions inches (millimeters) (Continued)



**16 Lead Ceramic Flatpak (F)
NS Package Number W16A**



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