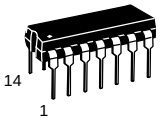
74HC164

Description

The 74HC164 is identical in pinout to the LS/ALS164. The Device inputs are compatible with standard CMOS outputs, with pullup resistors, they are compatible with LS/ALSTTL outputs. The 74HC164 is an 8-bit, serial-input parallel-output shift register. Two serial data inputs, A1 and A2, are provided so that one input May be used as a data enable. Data is entered on each rising Edge of the clock. The active-low asynchronous Reset overrides the Clock and Serial Data inputs.

Features

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices



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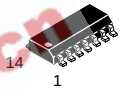

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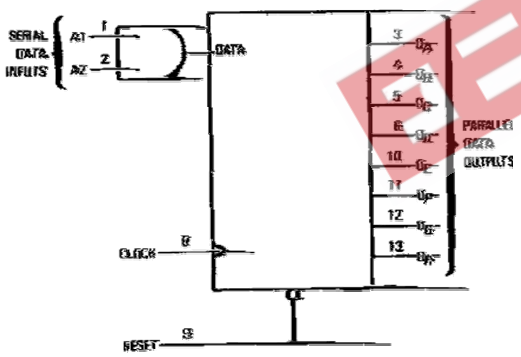
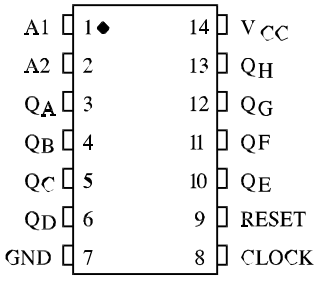
Package

Logic Diagram



Pin Assignment



Function Table

Inputs			Outputs
RESET	CLOCK	A1	QA QB... QH
L	X	X	L L...
H	↓	X X	L
H	↑	X H	no change
		D	D
H	↑		QAn... QGn
			D

D = data input

X = don't care

Q_{An} - Q_{Gn} = data shifted from the previous stage on a rising edge at the clock input.

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
~~V_{IN}~~	~~DC Input Voltage (Referenced to GND)~~	~~-1.5 to V_{CC} +1.5~~	~~V~~
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	
~~mA I_{OUT}~~	~~DC Output Current, per Pin~~	~~±25~~	
mA I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	
mA			
P_D	Power Dissipation in Still Air, Plastic DIP+	750 500	mW
Tstg	Storage Temperature	-65 to +150	℃
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	℃

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/ ℃ from 65 °to 125℃

SOIC Package: : - 7 mW/℃ from 65 °to 125℃

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
~~V_{IN}, V_{OUT}~~	~~DC Input Voltage, Output Voltage (Referenced to GND)~~		~~0~~	~~V_{CC}~~	~~V~~
~~T_A~~	~~Operating Temperature, All Package Types~~		~~-55~~	~~+125~~	~~℃~~
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} =2.0 V V_{CC} =4.5 V V_{CC} =6.0 V	0 0 0	1000 500 400	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must betaken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range

GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

DC Electrical Characteristics

(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit 25 ℃ to -55℃	Guaranteed Limit ≤ 85	Guaranteed Limit ≤ 125	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V I_{OUT} ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low - Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V I_{OUT} ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}= V_{IH} or V_{IL} I_{OUT} ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{IN}= V_{IH} or V_{IL} I_{OUT} ≤ 4.0 mA I_{OUT} ≤ 5.2	4.5 6.0	3.98 5.48	3.84 5.34	3.7 5.2	
V_{OL}	Maximum Low-Level Output Voltage	mA V_{IN}=V_{IH} or V_{IL} I_{OUT} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{IN}=V_{IH} or V_{IL} I_{OUT} ≤ 4.0 mA	4.5 6.0	0.26 0.26	0.33 0.33	0.4 0.4	
I_{IN}	Maximum Input Leakage Current	V_{IN}=V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0μA	6.0	8.0	80	160	μA

AC Electrical Characteristics

(C_L =50pF,Input t_r =t_f

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25 ℃ to -55℃	≤85℃	≤125℃	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t_{PLH}, t_{PHL} (Figures	Maximum Propagation Delay,Clock to Q 1 and 4)	2.0 4.5 6.0	175 35 30	220 44 37	265 53 45	ns
t_{PHL}	Maximum Propagation Delay,Reset to Q (Figures 2 and 4)	2.0 4.5 6.0	205 41 35	255 51 43	310 62 53	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{IN}	Maximum Input Capacitance	-	10	10	10	pF
t_{SU}	Minimum Setup Time,A1 or A2 to Clock (Figure 3)	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
t_h	Minimum Hold Time, Clock to A1 or A2 (Figure 3)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

C_{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: ^{2}f+I$_{CC}$V$_C$P$_D$=C$_{PD}$V	Typical @25℃,V_{CC}=5.0 V 140	pF

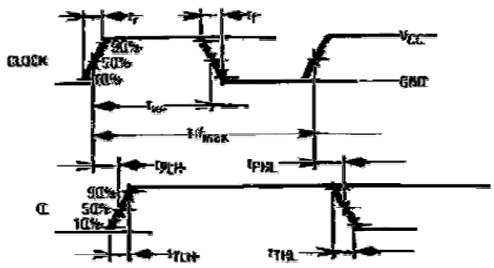


Figure 1. Switching Waveforms

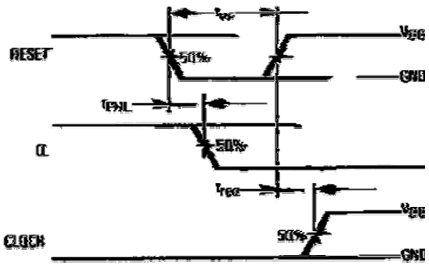


Figure 2. Switching Waveforms

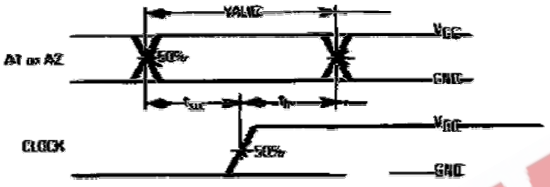


Figure 3. Switching Waveforms

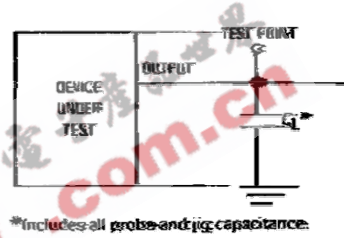
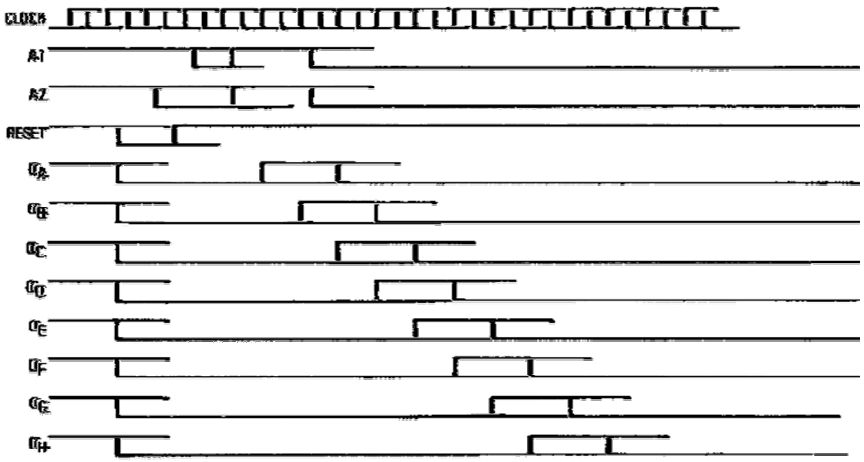


Figure 4. Test Circuit

Timing Diagram



Expanded Logic Diagram

Ordering Information

ORDERING NUMBER	PACKAGE	MARKING
74HC164	DIP - 14 / SOP - 14	ESTEK74HC164

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