

54F/74F646 • 74F646B • 54F/74F648 Octal Transceiver/Register with TRI-STATE® Outputs

General Description

These devices consist of bus transceiver circuits with TRI-STATE, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control \bar{G} and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control \bar{G} is Active LOW. In the isolation mode (control \bar{G} HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

Features

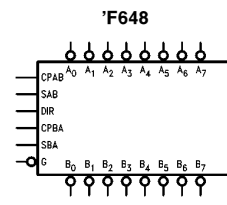
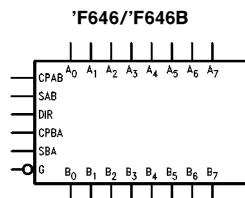
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- 'F648 has inverting data paths
- 'F646/'F646B have non-inverting data paths
- 'F646B is a faster version of the 'F646
- TRI-STATE outputs
- 300 mil slim DIP
- Guaranteed 4000V minimum ESD protection

| Commercial | Military | Package Number | Package Description |
|--------------------|--------------------|----------------|--|
| 74F646SPC | | N24C | 24-Lead (0.300" Wide) Molded Dual-In-Line |
| | 54F646DM (Note 2) | J24F | 24-Lead (0.300" Wide) Ceramic Dual-In-Line |
| 74F646SC (Note 1) | | M24B | 24-Lead (0.300" Wide) Molded Small Outline, JEDEC |
| 74F646MSA (Note 1) | | MSA24 | 24-Lead Molded Shrink Small Outline, EIAJ, Type II |
| | 54F646FM (Note 2) | W24C | 24-Lead Cerpack |
| | 54F646LM (Note 2) | E28A | 28-Lead Ceramic Leadless Chip Carrier, Type C |
| 74F646BSPC | | N24C | 24-Lead (0.300" Wide) Molded Dual-In-Line |
| 74F646BSC (Note 1) | | M24B | 24-Lead (0.300" Wide) Molded Small Outline, JEDEC |
| 74F648SPC | | N24C | 24-Lead (0.300" Wide) Molded Dual-In-Line |
| | 54F648SDM (Note 2) | J24F | 24-Lead (0.300" Wide) Ceramic Dual-In-Line |
| 74F648SC (Note 1) | | M24B | 24-Lead (0.300" Wide) Molded Small Outline, JEDEC |
| | 54F648FM (Note 2) | W24C | 24-Lead Cerpack |
| | 54F648LM (Note 2) | E28A | 24-Lead Ceramic Leadless Chip Carrier, Type C |

Note 1: Devices also available in 13" reel. Use suffix = SCX.

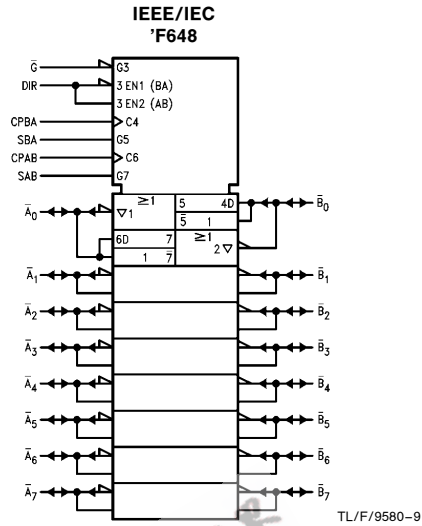
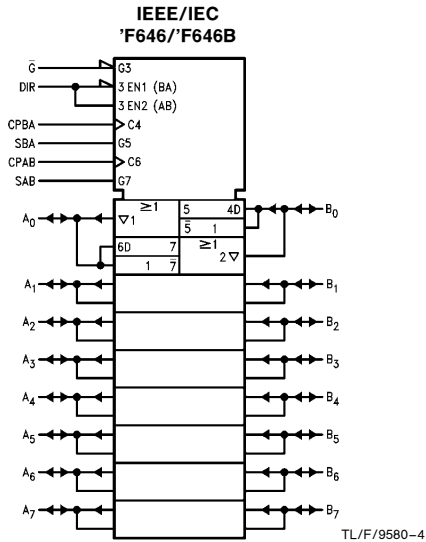
Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbols



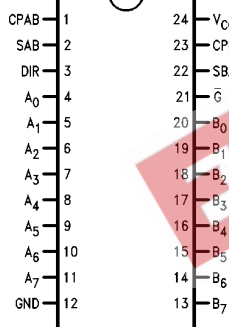
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Logic Symbols (Continued)

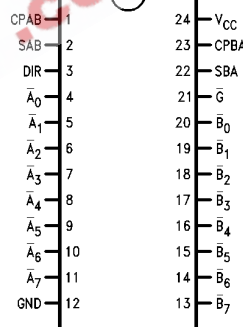


Connection Diagrams

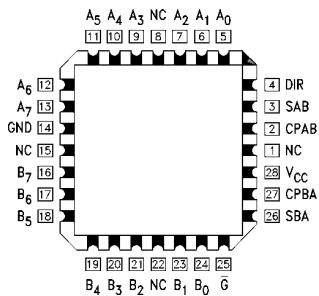
**Pin Assignment
for DIP, SOIC and Flatpak
'F646/'F646B**



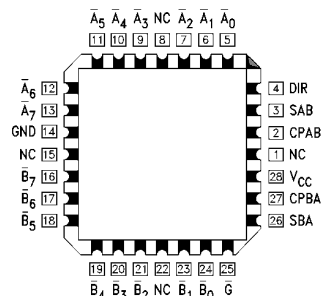
**Pin Assignment
for DIP, SOIC and Flatpak
'F648**



**Pin Assignment
for LCC
'F646/'F646B**



**Pin Assignment
for LCC
'F648**



Unit Loading/Fan Out

| Pin Names | Description | 54F/74F | |
|--------------------------------|--|-----------------------------|--|
| | | U.L. HIGH/LOW | Input I_{IH}/I_{IL} Output I_{OH}/I_{OL} |
| A ₀ –A ₇ | Data Register A Inputs/ TRI-STATE Outputs | 3.5/1.083 600/106.6 (80) | 70 μ A/ –650 μ A –12 mA/64 mA (48 mA) |
| B ₀ –B ₇ | Data Register B Inputs/ TRI-STATE Outputs | 3.5/1.083 600/106.6 (80) | 70 μ A/ –650 μ A –12 mA/64 mA (48 mA) |
| CPAB, CPBA | Clock Pulse Inputs | 1.0/1.0 | 20 μ A/ –0.6 mA |
| SAB, SBA | Select Inputs | 1.0/1.0 | 20 μ A/ –0.6 mA |
| \bar{G} | Output Enable Input | 1.0/1.0 | 20 μ A/ –0.6 mA |
| DIR | Direction Control Input | 1.0/1.0 | 20 μ A/ –0.6 mA |

Function Table

| Inputs | | | | | | Data I/O* | | Function |
|-----------|-----|--------|--------|-----|-----|--------------------------------|--------------------------------|--|
| \bar{G} | DIR | CPAB | CPBA | SAB | SBA | A ₀ –A ₇ | B ₀ –B ₇ | |
| H | X | H or L | H or L | X | X | Input | Input | Isolation |
| H | X | ↗ | X | X | X | | | Clock A _n Data into A Register |
| H | X | X | ↗ | X | X | | | Clock B _n Data into B Register |
| L | H | X | X | L | X | Input | Output | A _n to B _n —Real Time (Transparent Mode) |
| L | H | ↗ | X | L | X | | | Clock A _n Data into A Register |
| L | H | H or L | X | H | X | | | A Register to B _n (Stored Mode) |
| L | H | ↗ | X | H | X | | | Clock A _n Data into A Register and Output to B _n |
| L | L | X | X | X | L | Output | Input | B _n to A _n —Real Time (Transparent Mode) |
| L | L | X | ↗ | X | L | | | Clock B _n Data into B Register |
| L | L | X | H or L | X | H | | | B Register to A _n (Stored Mode) |
| L | L | X | ↗ | X | H | | | Clock B _n Data into B Register and Output to A _n |

*The data output functions may be enabled or disabled by various signals at the \bar{G} and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

H = HIGH Voltage Level

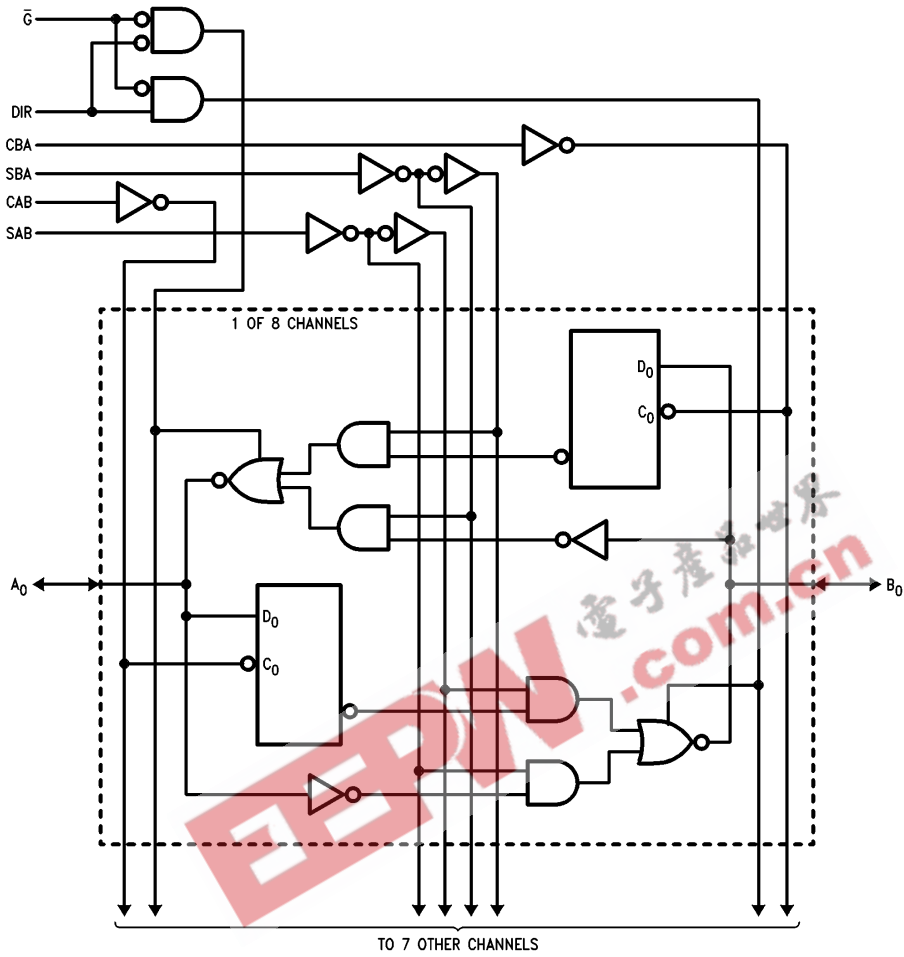
L = LOW Voltage Level

X = Irrelevant

↗ = LOW-to-HIGH Transition

Logic Diagrams (Continued)

'F646/'F646B

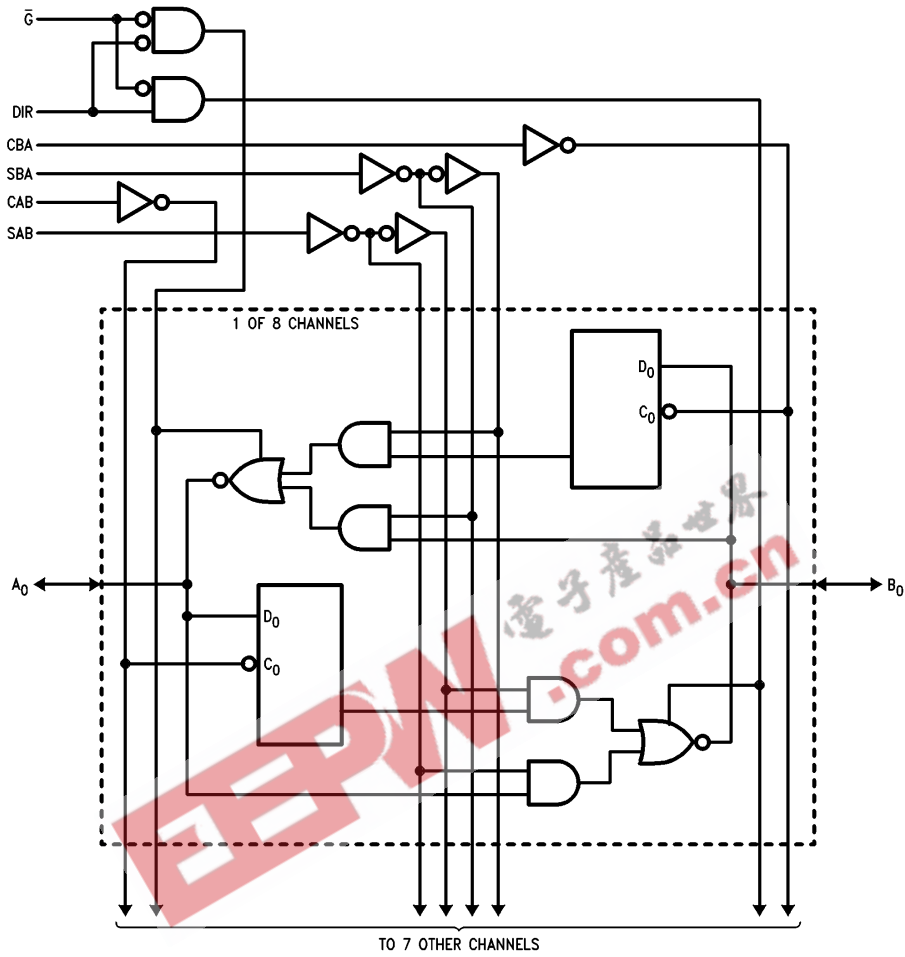


TL/F/9580-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Logic Diagrams (Continued)

'F648



TL/F/9580-6

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|--------------------------------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature under Bias | -55°C to +125°C |
| Junction Temperature under Bias | -55°C to +175°C |
| Plastic | -55°C to +150°C |
| V _{CC} Pin Potential to Ground Pin | -0.5V to +7.0V |
| Input Voltage (Note 2) | -0.5V to +7.0V |
| Input Current (Note 2) | -30 mA to +5.0 mA |
| Voltage Applied to Output in HIGH State (with V _{CC} = 0V) | |
| Standard Output | -0.5V to V _{CC} |
| TRI-STATE Output | -0.5V to +5.5V |
| Current Applied to Output in LOW State (Max) | twice the rated I _{OL} (mA) |
| ESD Last Passing Voltage (Min) | 4000V |

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

| | |
|------------------------------|-----------------|
| Free Air Ambient Temperature | |
| Military | -55°C to +125°C |
| Commercial | 0°C to +70°C |
| Supply Voltage | |
| Military | +4.5V to +5.5V |
| Commercial | +4.5V to +5.5V |

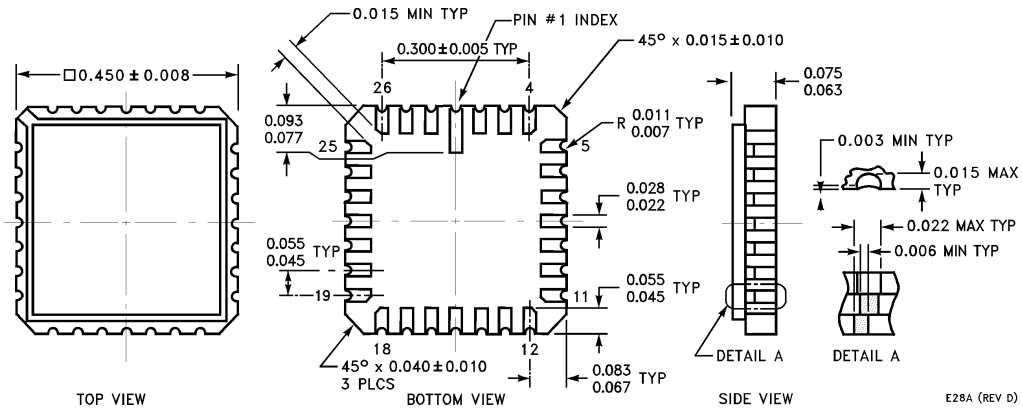
DC Electrical Characteristics

| Symbol | Parameter | 54F/74F | | | Units | V _{CC} | Conditions |
|------------------------------------|------------------------------------|--|--------------|------|-------|-----------------|--|
| | | Min | Typ | Max | | | |
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | | Recognized as a HIGH Signal |
| V _{IL} | Input LOW Voltage | 0.8 | | | V | | Recognized as a LOW Signal |
| V _{CD} | Input Clamp Diode Voltage | -1.2 | | | V | Min | I _{IN} = -18 mA (Non I/O Pins) |
| V _{OH} | Output HIGH Voltage | 54F 10% V _{CC} 74F 10% V _{CC} | 2.0 2.0 | | V | Min | I _{OH} = -12 mA (A _n , B _n) I _{OH} = -15 mA (A _n , B _n) |
| V _{OL} | Output LOW Voltage | 54F 10% V _{CC} 74F 10% V _{CC} | 0.55 0.55 | | V | Min | I _{OL} = 48 mA (A _n , B _n) I _{OL} = 64 mA (A _n , B _n) |
| I _{IH} | Input HIGH Current | 54F 74F | 20.0 5.0 | | μA | Max | V _{IN} = 2.7V (Non I/O Pins) |
| I _{BVI} | Input HIGH Current Breakdown Test | 54F 74F | 100 7.0 | | μA | Max | V _{IN} = 7.0V (Non I/O Pins) |
| I _{BVIT} | Input HIGH Current Breakdown (I/O) | 54F 74F | 1.0 0.5 | | mA | Max | V _{IN} = 5.5V (A _n , B _n) |
| I _{CEX} | Output HIGH Leakage Current | 54F 74F | 250 50 | | μA | Max | V _{OUT} = V _{CC} |
| V _{ID} | Input Leakage Test | 74F | 4.75 | | V | 0.0 | I _{ID} = 1.9 μA All Other Pins Grounded |
| I _{OD} | Output Leakage Circuit Current | 74F | 3.75 | | μA | 0.0 | V _{IOD} = 150 mV All Other Pins Grounded |
| I _{IL} | Input LOW Current | | -0.6 | | mA | Max | V _{IN} = 0.5V (Non I/O Pins) |
| I _{IH} + I _{OZH} | Output Leakage Current | | 70 | | μA | Max | V _{OUT} = 2.7V (A _n , B _n) |
| I _{IL} + I _{OZL} | Output Leakage Current | | -650 | | μA | Max | V _{OUT} = 0.5V (A _n , B _n) |
| I _{OS} | Output Short-Circuit Current | | -100 | -225 | mA | Max | V _{OUT} = 0V |
| I _{ZZ} | Bus Drainage Test | | 500 | | μA | 0.0V | V _{OUT} = 5.25V |
| I _{CCH} | Power Supply Current | | 135 | | mA | Max | V _O = HIGH |
| I _{CCL} | Power Supply Current | | 150 | | mA | Max | V _O = LOW |
| I _{CCZ} | Power Supply Current | | 150 | | mA | Max | V _O = HIGH Z |

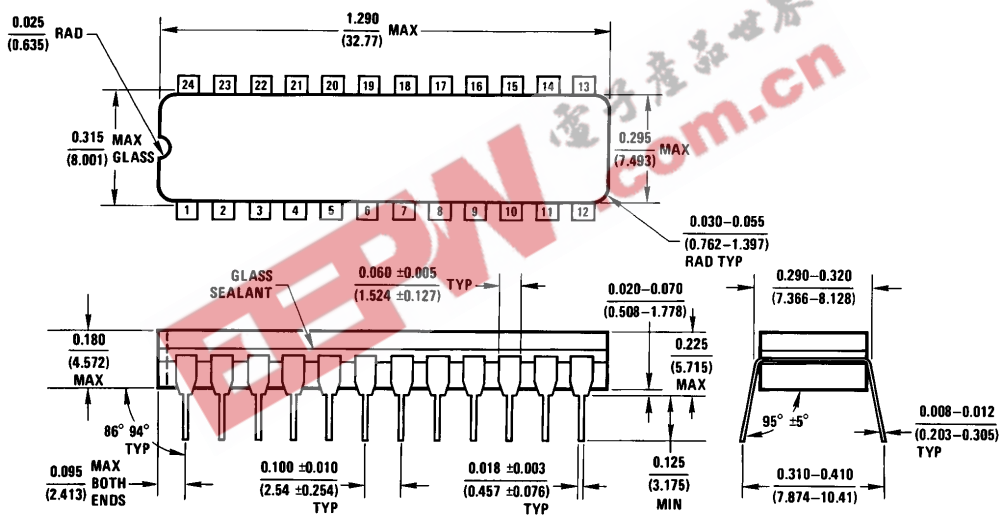
| 'F646/'F648 | | | | | | | | |
|--------------------------------------|---|---|--------------|--|--------------|--|--------------|-------|
| AC Electrical Characteristics | | | | | | | | |
| Symbol | Parameter | 74F | | 54F | | 74F | | Units |
| | | T _A = +25°C V _{CC} = +5.0V C _L = 50 pF | | T _A , V _{CC} = Mil C _L = 50 pF | | T _A , V _{CC} = Com C _L = 50 pF | | |
| | | Min | Max | Min | Max | Min | Max | |
| f _{max} | Maximum Clock Frequency | 90 | | 75 | | 90 | | MHz |
| t _{PLH} t _{PHL} | Propagation Delay Clock to Bus | 2.0 2.0 | 7.0 8.0 | 2.0 2.0 | 8.5 9.5 | 2.0 2.0 | 8.0 9.0 | ns |
| t _{PLH} t _{PHL} | Propagation Delay Bus to Bus ('F646) | 1.0 1.0 | 7.0 6.5 | 1.0 1.0 | 8.0 8.0 | 1.0 1.0 | 7.5 7.0 | ns |
| t _{PLH} t _{PHL} | Propagation Delay Bus to Bus ('F648) | 2.0 1.0 | 8.5 7.5 | 1.0 1.0 | 10.0 9.0 | 2.0 1.0 | 9.0 8.0 | ns |
| t _{PLH} t _{PHL} | Propagation Delay SBA or SAB to A or B | 2.0 2.0 | 8.5 8.0 | 2.0 2.0 | 11.0 10.0 | 2.0 2.0 | 9.5 9.0 | ns |
| t _{PZH} t _{PZL} | Enable Time OE to A or B | 2.0 2.0 | 8.5 12.0 | 2.0 2.0 | 10.0 13.5 | 2.0 2.0 | 9.0 12.5 | ns |
| t _{PHZ} t _{PLZ} | Disable Time OE to A or B | 1.0 2.0 | 7.5 9.0 | 1.0 2.0 | 9.0 11.0 | 1.0 2.0 | 8.5 9.5 | ns |
| t _{PZH} t _{PZL} | Enable Time DIR to A or B | 2.0 2.0 | 14.0 13.0 | 2.0 2.0 | 16.0 15.0 | 2.0 2.0 | 15.0 14.0 | ns |
| t _{PHZ} t _{PLZ} | Disable Time DIR to A or B | 1.0 2.0 | 9.0 11.0 | 1.0 2.0 | 10.0 12.0 | 1.0 2.0 | 9.5 11.5 | ns |

| 'F646/'F648 | | | | | | | | |
|--|---|---|-----|--|-----|--|-----|-------|
| AC Operating Requirements | | | | | | | | |
| Symbol | Parameter | 74F | | 54F | | 74F | | Units |
| | | T _A = +25°C V _{CC} = +5.0V | | T _A , V _{CC} = Mil | | T _A , V _{CC} = Com | | |
| | | Min | Max | Min | Max | Min | Max | |
| t _s (H) t _s (L) | Setup Time, HIGH or LOW Bus to Clock | 5.0 5.0 | | 5.0 5.0 | | 5.0 5.0 | | ns |
| t _h (H) t _h (L) | Hold Time, HIGH or LOW Bus to Clock | 2.0 2.0 | | 2.5 2.5 | | 2.0 2.0 | | ns |
| t _w (H) t _w (L) | Clock Pulse Width HIGH or LOW | 5.0 5.0 | | 5.0 5.0 | | 5.0 5.0 | | ns |

Physical Dimensions inches (millimeters)

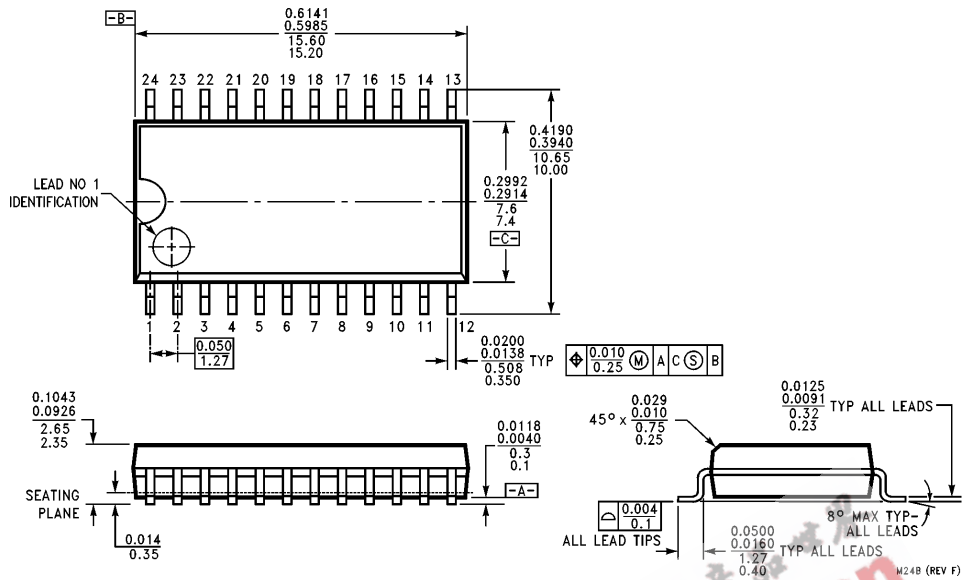


28-Lead Ceramic Leadless Chip Carrier, Type C
NS Package Number E28A



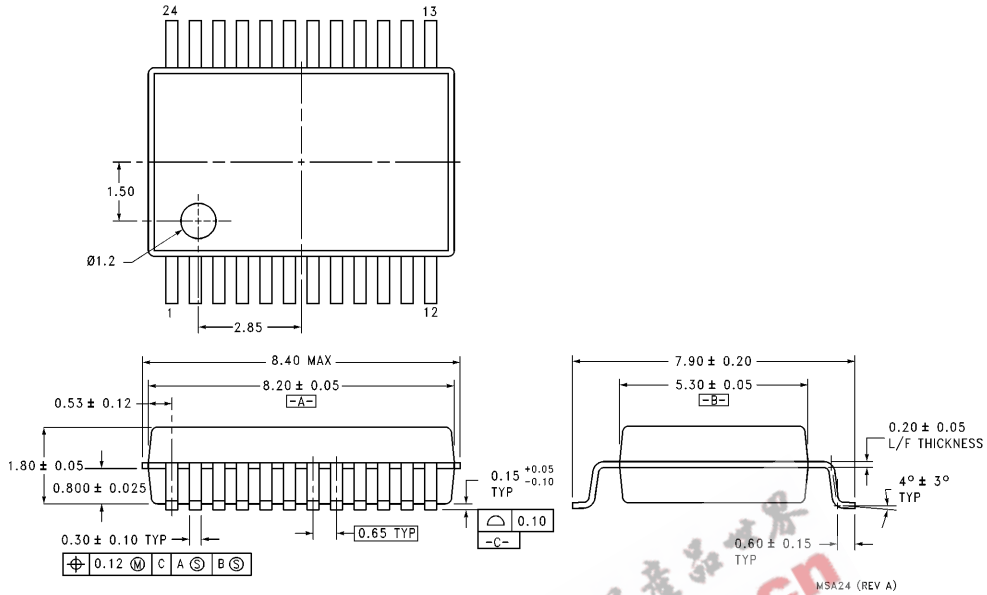
24-Lead (0.300" Wide) Ceramic Dual-In-Line Package (SD)
NS Package Number J24F

Physical Dimensions inches (millimeters) (Continued)

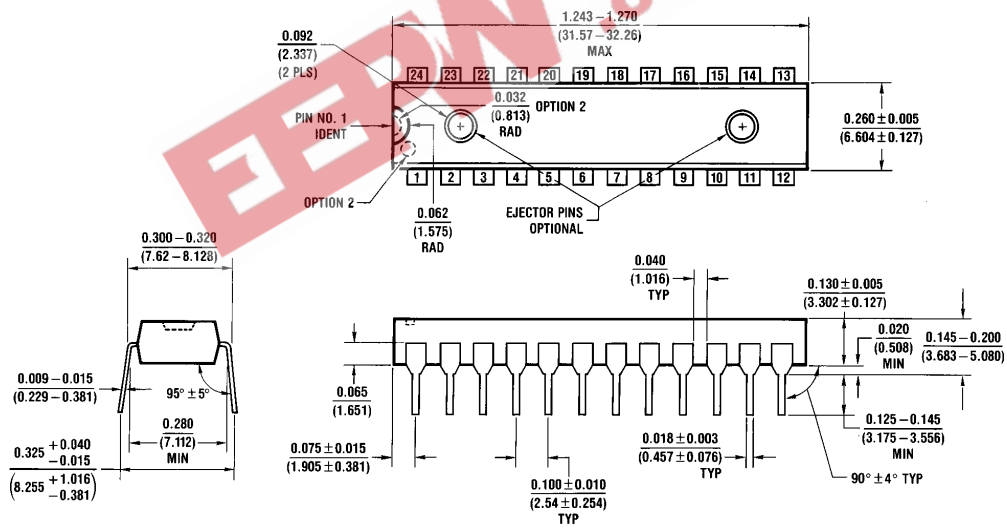


24-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M24B

Physical Dimensions inches (millimeters) (Continued)

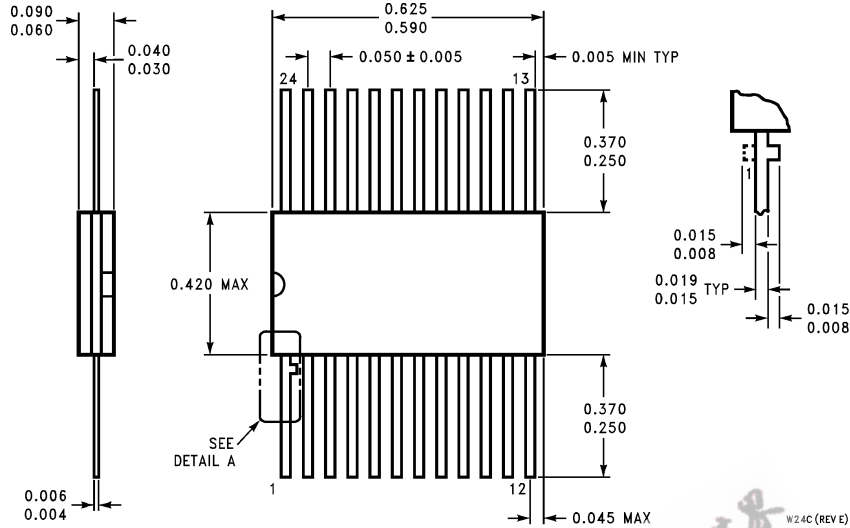


24-Lead Molded Shrink Small Outline Package, EIAJ, Type II
NS Package Number MSA24



24-Lead (0.300" Wide) Molded Dual-In-Line Package (SP)
NS Package Number N24C

Physical Dimensions inches (millimeters) (Continued)



**24-Lead Cerpack
NS Package Number W24C**

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