

74LVQ273

Low Voltage Octal D-Type Flip-Flop

General Description

The LVQ273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (\overline{MR}) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the MR input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Features

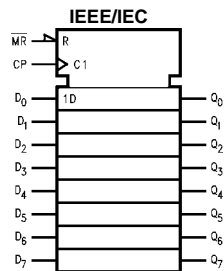
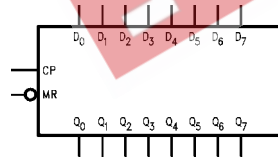
- Ideal for low power/low noise 3.3V applications
- Implements patented EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity

Ordering Code:

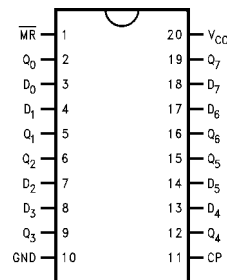
Order Number	Package Number	Package Description
74LVQ273SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVQ273SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVQ273QSC	MQA20	20-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Pin Descriptions

Pin Names	Description
D ₀ -D ₇	Data Inputs
\overline{MR}	Master Reset
CP	Clock Pulse Input
Q ₀ -Q ₇	Data Outputs

Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions (Note 2)	
Supply Voltage (V_{CC})	-0.5V to +7.0V	Supply Voltage (V_{CC})	2.0V to 3.6V
DC Input Diode Current (I_{IK})		Input Voltage (V_I)	0V to V_{CC}
$V_I = -0.5V$	-20 mA	Output Voltage (V_O)	0V to V_{CC}
$V_I = V_{CC} + 0.5V$	+20 mA	Operating Temperature (T_A)	-40°C to +85°C
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$	Minimum Input Edge Rate $\Delta V/\Delta t$	
DC Output Diode Current (I_{OK})		V_{IN} from 0.8V to 2.0V	
$V_O = -0.5V$	-20 mA	V_{CC} @ 3.0V	125 mV/ns
$V_O = V_{CC} + 0.5V$	+20 mA		
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$		
DC Output Source			
or Sink Current (I_O)	± 50 mA		
DC V_{CC} or Ground Current			
(I_{CC} or I_{GND})	± 400 mA		
Storage Temperature (T_{STG})	-65°C to +150°C		
DC Latch-up Source or			
Sink Current	± 300 mA		

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits	Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu\text{A}$	
		3.0		2.58	2.48	V	$V_{IN} = V_{IL}$ or V_{IH} (Note 3) $I_{OH} = -12 \text{ mA}$	
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu\text{A}$	
		3.0		0.36	0.44	V	$V_{IN} = V_{IL}$ or V_{IH} (Note 3) $I_{OL} = 12 \text{ mA}$	
I_{IN}	Maximum Input Leakage Current	3.6		± 0.1	± 1.0	μA	$V_I = V_{CC}$, GND	
I_{OLD}	Minimum Dynamic Output Current (Note 4)	3.6			36	mA	$V_{OLD} = 0.8V$ Max (Note 5)	
I_{OHD}	Output Current (Note 4)	3.6			-25	mA	$V_{OHD} = 2.0V$ Min (Note 5)	
I_{CC}	Maximum Quiescent Supply Current	3.6		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	0.4	0.8		V	(Note 6)(Note 7)	
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	-0.3	-0.8		V	(Note 6)(Note 7)	
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0		V	(Note 6)(Note 8)	
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8		V	(Note 6)(Note 8)	

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: Incident wave switching on transmission lines with impedances as low as 75 Ω for commercial temperature range is guaranteed for.

Note 6: Worst case package.

Note 7: Max number of outputs defined as (n). Data Inputs are driven 0V to 3.3V; one output at GND.

Note 8: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), $f = 1 \text{ MHz}$.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	2.7 3.3 ± 0.3	50 90			45 75		MHz
t _{PLH}	Propagation Delay CP to Q _n	2.7 3.3 ± 0.3	4.0 4.0	9.6 8.0	17.6 12.5	3.0 3.0	20.0 14.0	ns
t _{PHL}	Propagation Delay CP to Q _n	2.7 3.3 ± 0.3	4.0 4.0	10.2 8.5	18.3 13.0	3.5 3.5	20.5 14.5	ns
t _{PHL}	Propagation Delay $\overline{\text{MR}}$ to Q _n	2.7 3.3 ± 0.3	4.0 4.0	10.2 8.5	18.3 13.0	3.5 3.5	20.0 14.0	ns
t _{OSSL}	Output to Output	2.7		1.0	1.5		1.5	ns
t _{OSSLH}	Skew (Note 9)	3.3 ± 0.3		1.0	1.5		1.5	ns

Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSSLH}). Parameter guaranteed by design. Not tested.

AC Operating Requirements

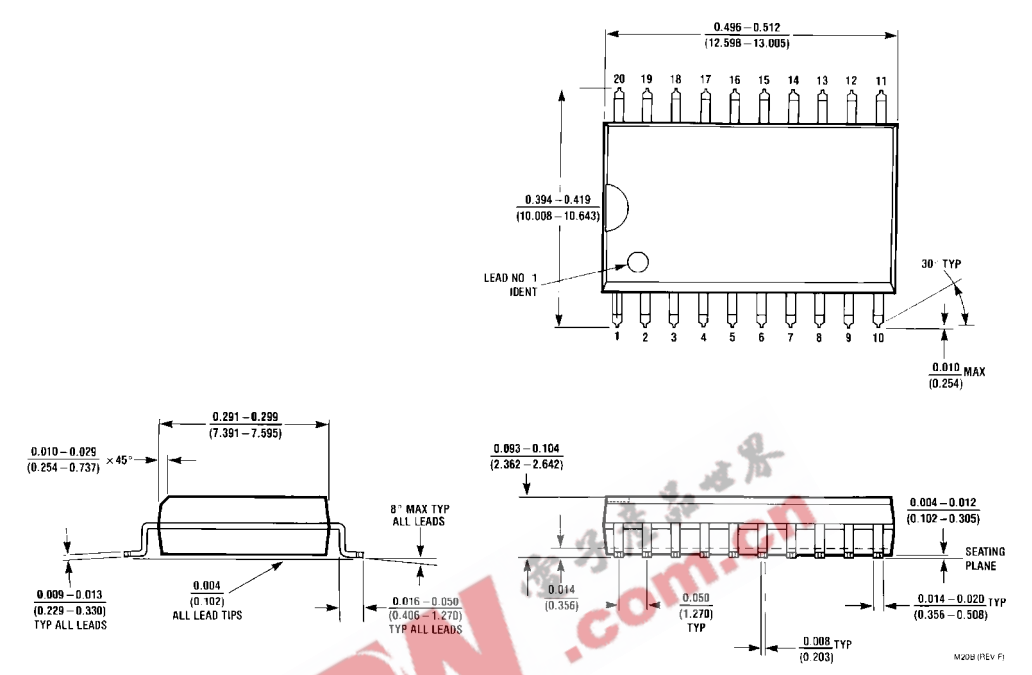
Symbol	Parameter	V _{CC} (V)	T _A = +25°C C _L = 50 pF	T _A = -40°C to +85°C C _L = 50 pF	Units
			Typ	Guaranteed Minimum	
t _S	Setup Time, HIGH or LOW D _n to CP	2.7 3.3 ± 0.3	6.5 5.0	8.5 6.0	ns
t _H	Hold Time, HIGH or LOW D _n to CP	2.7 3.3 ± 0.3	0.0 0.0	0.0 0.0	ns
t _W	Clock Pulse Width HIGH or LOW	2.7 3.3 ± 0.3	7.0 5.5	8.5 6.0	ns
t _W	$\overline{\text{MR}}$ Pulse Width HIGH or LOW	2.7 3.3 ± 0.3	7.0 5.5	8.5 6.0	ns
t _W	Recovery Time $\overline{\text{MR}}$ to CP	2.7 3.3 ± 0.3	5.0 4.0	6.5 4.5	ns

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = Open
C _{PD} (Note 10)	Power Dissipation Capacitance	35	pF	V _{CC} = 3.3V

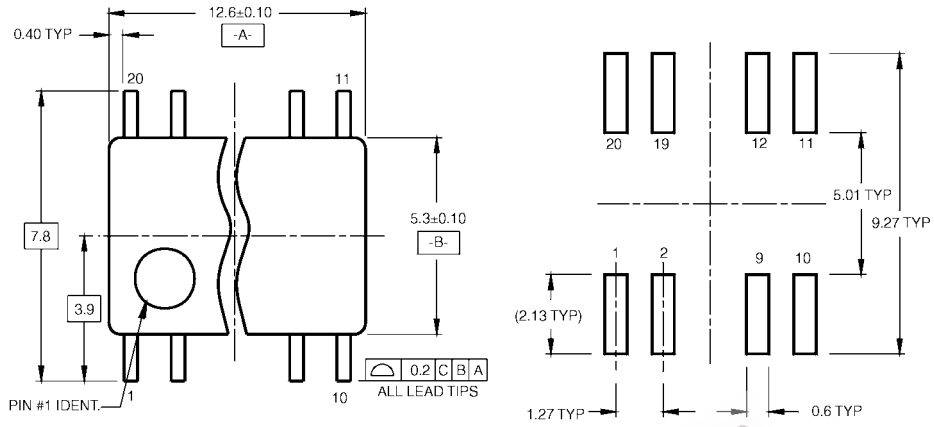
Note 10: C_{PD} is measured at 10 MHz.

Physical Dimensions inches (millimeters) unless otherwise noted

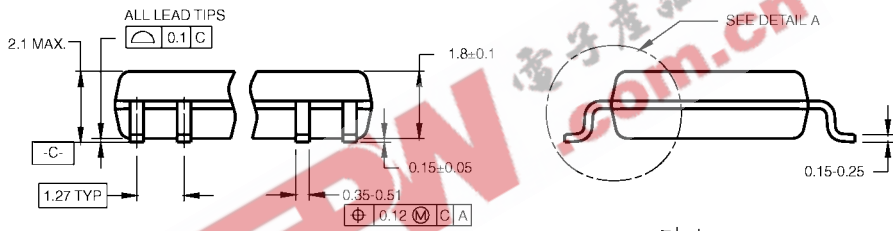


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION

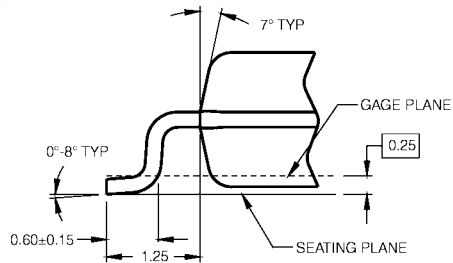


DIMENSIONS ARE IN MILLIMETERS

NOTES:

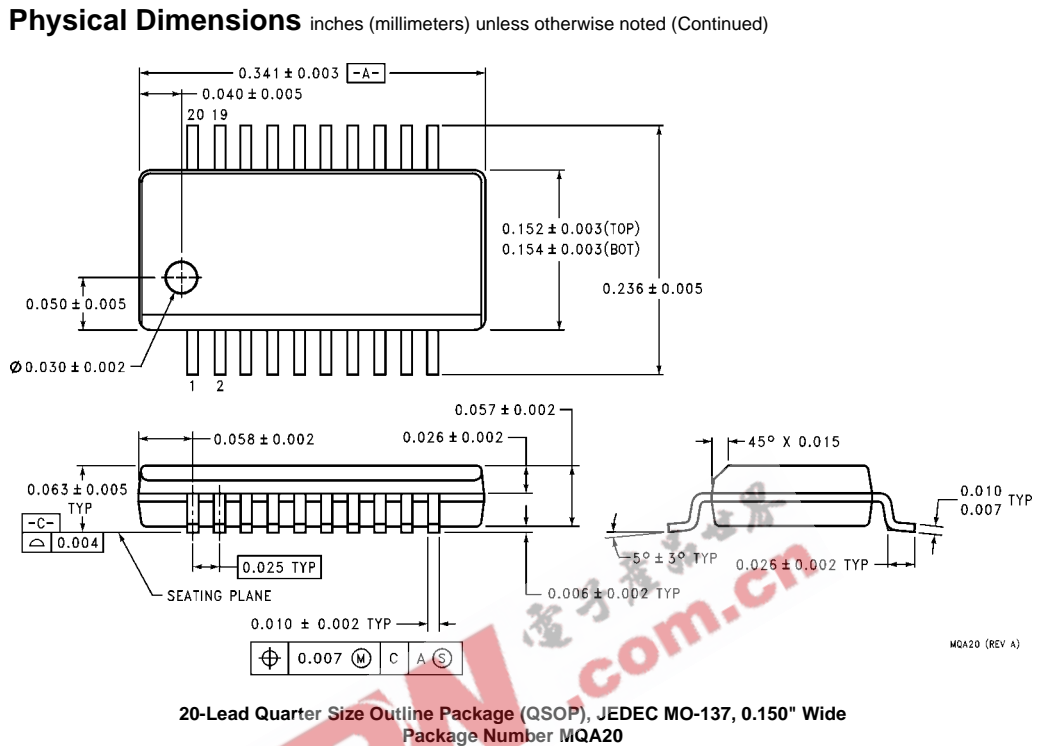
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- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1



DETAIL A

20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D



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