

## 74ALVCH16244

### Low Voltage 16-Bit Buffer/Line Driver with Bushold

#### General Description

The ALVCH16244 contains sixteen non-inverting buffers with 3-STATE outputs to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble (4-bit) controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

The ALVCH16244 data inputs include active bushold circuitry, eliminating the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level.

The 74ALVCH16244 is designed for low voltage (1.65V to 3.6V)  $V_{CC}$  applications with output capability up to 3.6V.

The 74ALVCH16244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

#### Features

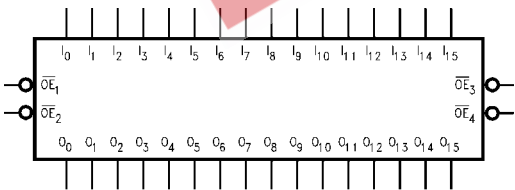
- 1.65V to 3.6V  $V_{CC}$  supply operation
- 3.6V tolerant control inputs and outputs
- Bushold on data inputs eliminating the need for external pull-up/pull-down resistors
- $t_{PD}$ 
  - 3 ns max for 3.0V to 3.6V  $V_{CC}$
  - 3.7 ns max for 2.3V to 2.7V  $V_{CC}$
  - 6.0 ns max for 1.65V to 1.95V  $V_{CC}$
- Uses patented noise/EMI reduction circuitry
- Latch-up conforms to JEDEC JED78
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V

#### Ordering Code:

Order Number	Package Number	Package Description
74ALVCH16244T	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

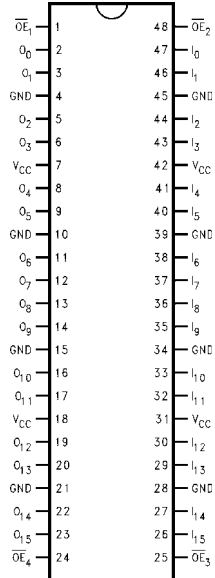
#### Logic Symbol



#### Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$I_0$ - $I_{15}$	Bushold Inputs
$O_0$ - $O_{15}$	Outputs

### Connection Diagram



### Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$I_0-I_3$	$O_0-O_3$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	$I_8-I_{11}$	$O_8-O_{11}$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	$I_4-I_7$	$O_4-O_7$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	$I_{12}-I_{15}$	$O_{12}-O_{15}$
L	L	L
L	H	H
H	X	Z

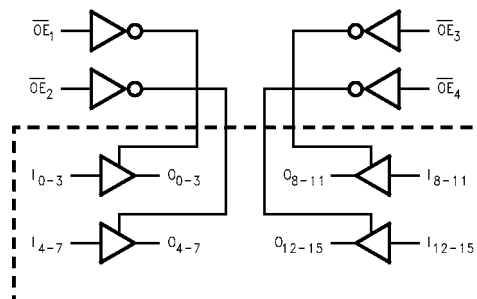
H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial (HIGH or LOW, inputs may not float)  
 Z = High Impedance

### Functional Description

The 74ALVCH16244 contains sixteen non-inverting buffers with 3-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of each other. The control pins may be shorted together to obtain full 16-bit operation. The 3-STATE out-

puts are controlled by an Output Enable ( $\overline{OE}_n$ ) input. When  $\overline{OE}_n$  is LOW, the outputs are in the 2-state mode. When  $\overline{OE}_n$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the inputs.

### Logic Diagram



Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions (Note 3)	
Supply Voltage ( $V_{CC}$ )	-0.5V to +4.6V	Power Supply	
DC Input Voltage ( $V_I$ )	-0.5V to 4.6V	Operating	1.65V to 3.6V
Output Voltage ( $V_O$ ) (Note 2)	-0.5V to $V_{CC} + 0.5V$	Input Voltage ( $V_I$ )	0V to $V_{CC}$
DC Input Diode Current ( $I_{IK}$ )		Output Voltage ( $V_O$ )	0V to $V_{CC}$
$V_I < 0V$	-50 mA	Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
DC Output Diode Current ( $I_{OK}$ )		Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	
$V_O < 0V$	-50 mA	$V_{IN} = 0.8V$ to $2.0V$ , $V_{CC} = 3.0V$	10 ns/V
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	±50 mA	<b>Note 1:</b> The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.	
DC $V_{CC}$ or GND Current per Supply Pin ( $I_{CC}$ or GND)	±100 mA	<b>Note 2:</b> $I_O$ Absolute Maximum Rating must be observed, limited to 4.6V.	
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C	<b>Note 3:</b> Floating or unused control inputs must be held HIGH or LOW.	

### DC Electrical Characteristics

Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units
$V_{IH}$	HIGH Level Input Voltage		1.65 - 1.95 2.3 - 2.7 2.7 - 3.6	$0.65 \times V_{CC}$ 1.7 2.0		V
$V_{IL}$	LOW Level Input Voltage		1.65 - 1.95 2.3 - 2.7 2.7 - 3.6		$0.35 \times V_{CC}$ 0.7 0.8	V
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$ $I_{OH} = -4 mA$ $I_{OH} = -6 mA$ $I_{OH} = -12 mA$ $I_{OH} = -24 mA$	1.65 - 3.6 1.65 2.3 2.3 2.7 3.0 3.0	$V_{CC} - 0.2$ 1.2 2.0 1.7 2.2 2.4 2		V
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$ $I_{OL} = 4 mA$ $I_{OL} = 6 mA$ $I_{OL} = 12 mA$ $I_{OL} = 24 mA$	1.65 - 3.6 1.65 2.3 2.3 2.7 3.0		0.2 0.45 0.4 0.7 0.4 0.55	V
$I_I$	Input Leakage Current	$0 \leq V_I \leq 3.6V$	3.6		±5.0	μA
$I_{I(HOLD)}$	Bushold Input Minimum Drive Hold Current	$V_{IN} = 0.58V$ $V_{IN} = 1.07V$ $V_{IN} = 0.7V$ $V_{IN} = 1.7V$ $V_{IN} = 0.8V$ $V_{IN} = 2.0V$ $0 < V_O \leq 3.6V$	1.65 1.65 2.3 2.3 3.0 3.0 3.6	25 -25 45 -45 75 -75		μA
$I_{OZ}$	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$	3.6		±10	μA
$I_{CC}$	Quiescent Supply Current	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6		40	μA
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	$V_{IH} = V_{CC} - 0.6V$	3 - 3.6		750	μA

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AC Electrical Characteristics										
Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, R <sub>L</sub> = 500Ω								Units
		C <sub>L</sub> = 50 pF				C <sub>L</sub> = 30 pF				
		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 1.8V ± 0.15V		
		Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay	1.0	3		3.6	1.0	3.7	1.5	6.0	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	1.0	4.4		5.4	1.0	5.7	1.5	8.2	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time	1.0	4.1		4.6	1.0	5.2	1.5	6.8	ns
Capacitance										
Symbol	Parameter	Conditions	T <sub>A</sub> = +25°C		Units					
			V <sub>CC</sub>	Typical						
C <sub>IN</sub>	Input Capacitance	Control	V <sub>I</sub> = 0V or V <sub>CC</sub>	3.3	3	pF				
		Data	V <sub>I</sub> = 0V or V <sub>CC</sub>	3.3	6					
C <sub>OUT</sub>	Output Capacitance		V <sub>I</sub> = 0V or V <sub>CC</sub>	3.3	7	pF				
C <sub>PD</sub>	Power Dissipation Capacitance	Outputs Enabled	f = 10 MHz, C <sub>L</sub> = 50 pF	3.3	19	pF				
				2.5	16					
		Outputs Disabled	f = 10 MHz, C <sub>L</sub> = 50 pF	3.3	5					
				2.5	4					

## AC Loading and Waveforms

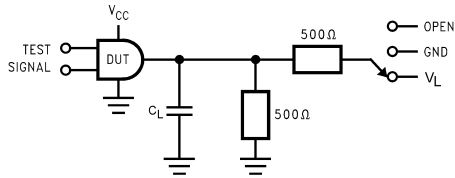


FIGURE 1. AC Test Circuit

TABLE 1. Values for Figure 1

TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	$V_L$
$t_{PZH}$ , $t_{PHZ}$	GND

TABLE 2. Variable Matrix

(Input Characteristics:  $f = 1\text{MHz}$ ;  $t_r = t_f = 2\text{ns}$ ;  $Z_0 = 50\Omega$ )

Symbol	$V_{CC}$			
	$3.3\text{V} \pm 0.3\text{V}$	$2.7\text{V}$	$2.5\text{V} \pm 0.2\text{V}$	$1.8\text{V} \pm 0.15\text{V}$
$V_{mi}$	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_{mo}$	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_X$	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.15\text{V}$	$V_{OL} + 0.15\text{V}$
$V_Y$	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.15\text{V}$	$V_{OH} - 0.15\text{V}$
$V_L$	6V	6V	$V_{CC} * 2$	$V_{CC} * 2$

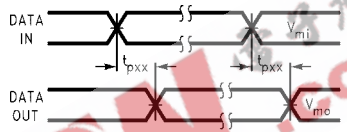


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

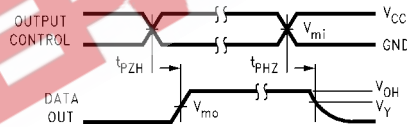


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

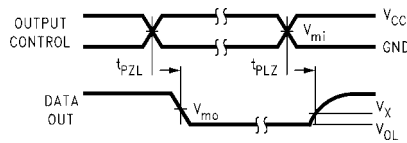
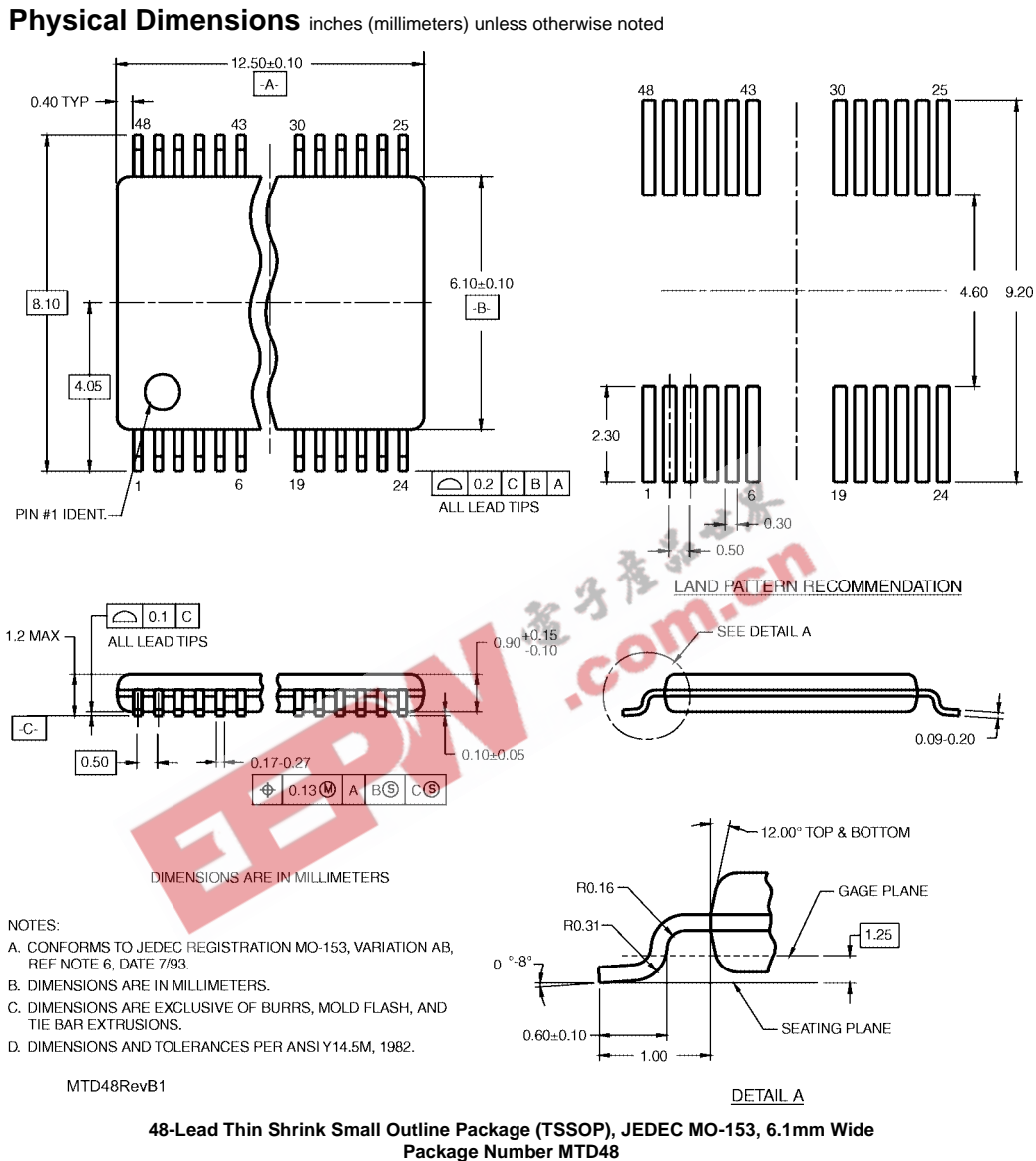


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic



- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
  - D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48RevB1

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