

DATA SHEET

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74LV688

8-bit magnitude comparator

Product specification
Supersedes data of 1997 May 15
IC24 Data Handbook

1998 Jun 23

8-bit magnitude comparator

74LV688

FEATURES

- Wide operating voltage: 1.0 to 5.5V
- Optimized for low voltage applications: 1.0V to 3.6V
- Accepts TTL input levels between $V_{CC} = 2.7V$ and $V_{CC} = 3.6V$
- Typical V_{OLP} (output ground bounce) $< 0.8V$ at $V_{CC} = 3.3V$, $T_{amb} = 25^{\circ}C$
- Typical V_{OHV} (output V_{OH} undershoot) $> 2V$ at $V_{CC} = 3.3V$, $T_{amb} = 25^{\circ}C$
- Compare two 8-bit words
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV688 is a high-speed Si-gate CMOS device, pin compatible with the 74HC/HCT688

The 74LV688 is an 8-bit magnitude comparator. It performs comparisons of two 8-bit binary or BCD words. The output provides $P = Q$ (equal-to).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay P_n , Q_n to $\overline{P=Q}$	$C_L = 15pF$ $V_{CC} = 3.3V$	17	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	$V_I = GND$ to V_{CC}^1	22	pF

NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz; C_L = output load capacity in pF;

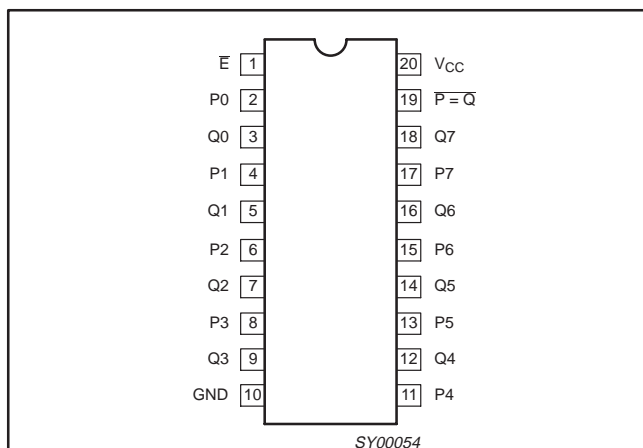
f_o = output frequency in MHz; V_{CC} = supply voltage in V;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
20-Pin Plastic DIL	$-40^{\circ}C$ to $+125^{\circ}C$	74LV688 N	74LV688 N	SOT146-1
20-Pin Plastic SO	$-40^{\circ}C$ to $+125^{\circ}C$	74LV688 D	74LV688 D	SOT163-1
20-Pin Plastic SSOP Type II	$-40^{\circ}C$ to $+125^{\circ}C$	74LV688 DB	74LV688 DB	SOT339-1
20-Pin Plastic TSSOP Type I	$-40^{\circ}C$ to $+125^{\circ}C$	74LV688 PW	74LV688PW DH	SOT360-1

PIN CONFIGURATION



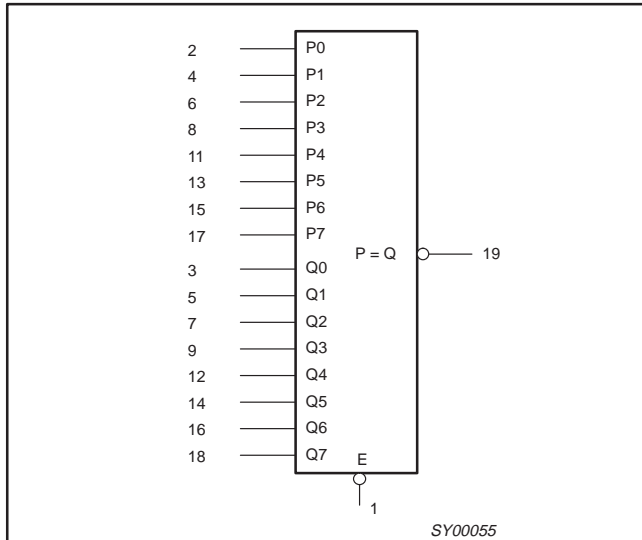
PIN DESCRIPTION

PIN NO.	SYMBOL	FUNCTION
1	E	Enable input (active LOW)
2, 4, 6, 8, 11, 13, 15, 17	P0 to P7	Word inputs
3, 5, 7, 9, 12, 14, 16, 18	Q0 to Q7	Word inputs
10	GND	Ground (0V)
19	$\overline{P=Q}$	Equal to output
20	V_{CC}	Positive Supply Voltage

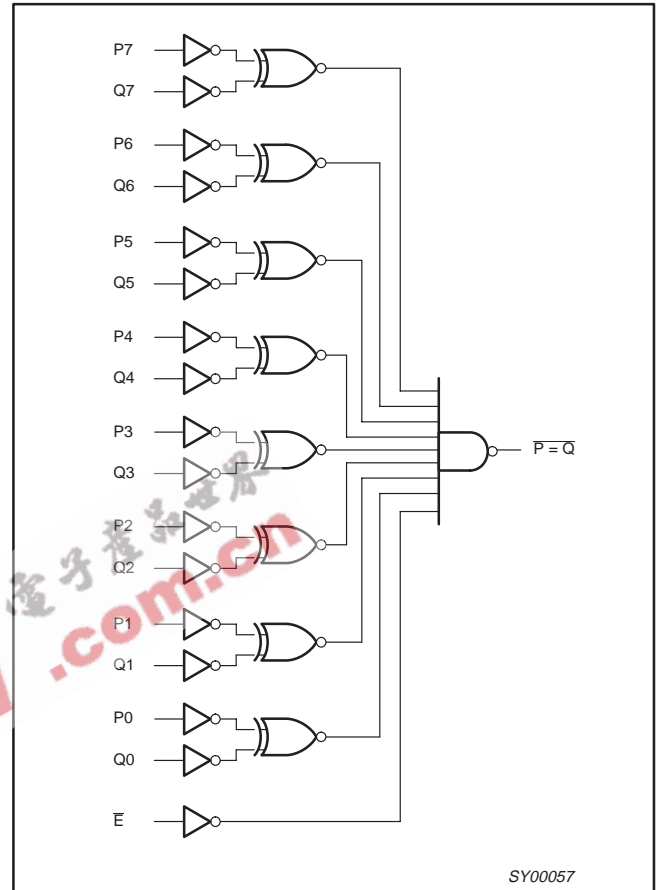
8-bit magnitude comparator

74LV688

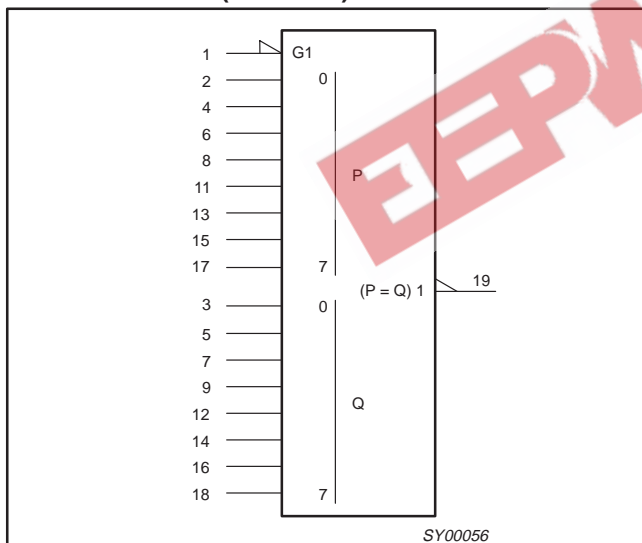
LOGIC SYMBOL



LOGIC DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		OUTPUT
DATA Pn, Qn	ENABLE E	$\overline{P = Q}$
P = Q	L	L
X	H	H
P > Q	L	H
P < Q	L	H

NOTES:

- H = HIGH voltage level
- L = LOW voltage level
- X = Don't care

8-bit magnitude comparator

74LV688

ABSOLUTE MAXIMUM RATINGS^{1, 2}

In accordance with the Absolute Maximum Rating System (IEC 134).

Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	DC supply voltage		-0.5	+7.0	V
I_{IK}	DC input diode current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	± 20	mA
I_{OK}	DC output diode current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	± 50	mA
I_O	DC output source or sink current - standard outputs	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$		± 25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with - standard outputs			± 50	mA
T_{stg}	Storage temperature range		-65	+150	°C
P_{tot}	power dissipation per package - plastic DIL - plastic mini-pack (SO) - plastic medium-shrink SO (SSOP and TSSOP)	for temperature range: -40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	-	750 500 400	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	DC supply voltage	see note 1	1.0	3.3	5.5	V
V_I	DC Input voltage		0	-	V_{CC}	V
V_O	DC output voltage		0	-	V_{CC}	V
T_{amb}	Operating ambient temperature range in free-air	See DC and AC characteristics	-40 -40	- -	+85 +125	°C
t_r , t_f ($\Delta t/\Delta v$)	Input rise and fall times	$V_{CC} = 1.0\text{ V}$ to 2.0 V $V_{CC} = 2.0\text{ V}$ to 2.7 V $V_{CC} = 2.7\text{ V}$ to 3.6 V $V_{CC} = 3.6\text{ V}$ to 5.5 V		- - - -	500 200 100 50	ns/V

NOTE:

- The LV is guaranteed to function down to $V_{CC} = 1.0\text{ V}$ (input levels GND or V_{CC}); DC characteristics are guaranteed from $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 5.5\text{ V}$.

8-bit magnitude comparator

74LV688

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP ¹	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	$V_{CC} = 1.2V$	0.9			0.9		V
		$V_{CC} = 2.0V$	1.4			1.4		
		$V_{CC} = 2.7$ to $3.6V$	2.0			2.0		
		$V_{CC} = 4.5$ to $5.5V$	$0.7 * V_{CC}$			$0.7 * V_{CC}$		
V_{IL}	LOW level Input voltage	$V_{CC} = 1.2V$			0.3		0.3	V
		$V_{CC} = 2.0V$			0.6		0.6	
		$V_{CC} = 2.7$ to $3.6V$			0.8		0.8	
		$V_{CC} = 4.5$ to 5.5			$0.3 * V_{CC}$		$0.3 * V_{CC}$	
V_{OH}	HIGH level output voltage; all outputs	$V_{CC} = 1.2V; V_I = V_{IH}$ or $V_{IL}; -I_O = 100\mu A$		1.2				V
		$V_{CC} = 2.0V; V_I = V_{IH}$ or $V_{IL}; -I_O = 100\mu A$	1.8	2.0		1.8		
		$V_{CC} = 2.7V; V_I = V_{IH}$ or $V_{IL}; -I_O = 100\mu A$	2.5	2.7		2.5		
		$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; -I_O = 100\mu A$	2.8	3.0		2.8		
		$V_{CC} = 4.5V; V_I = V_{IH}$ or $V_{IL}; -I_O = 100\mu A$	4.3	4.5		4.3		
	HIGH level output voltage; STANDARD outputs	$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; -I_O = 6mA$	2.40	2.82		2.20		
$V_{CC} = 4.5V; V_I = V_{IH}$ or $V_{IL}; -I_O = 12mA$		3.60	4.20		3.50			
V_{OL}	LOW level output voltage; all outputs	$V_{CC} = 1.2V; V_I = V_{IH}$ or $V_{IL}; I_O = 100\mu A$		0				V
		$V_{CC} = 2.0V; V_I = V_{IH}$ or $V_{IL}; I_O = 100\mu A$		0	0.2		0.2	
		$V_{CC} = 2.7V; V_I = V_{IH}$ or $V_{IL}; I_O = 100\mu A$		0	0.2		0.2	
		$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; I_O = 100\mu A$		0	0.2		0.2	
		$V_{CC} = 4.5V; V_I = V_{IH}$ or $V_{IL}; I_O = 100\mu A$		0	0.2		0.2	
	LOW level output voltage; STANDARD outputs	$V_{CC} = 3.0V; V_I = V_{IH}$ or $V_{IL}; I_O = 6mA$		0.25	0.40		0.50	
		$V_{CC} = 4.5V; V_I = V_{IH}$ or $V_{IL}; I_O = 12mA$		0.35	0.55		0.65	
I_I	Input leakage current	$V_{CC} = 5.5V; V_I = V_{CC}$ or GND			1.0		1.0	μA
I_{CC}	Quiescent supply current; MSI	$V_{CC} = 5.5V; V_I = V_{CC}$ or GND; $I_O = 0$			20.0		160	μA
ΔI_{CC}	Additional quiescent supply current	$V_{CC} = 2.7V$ to $3.6V; V_I = V_{CC} - 0.6V$			500		850	μA

NOTE:1. All typical values are measured at $T_{amb} = 25^\circ C$.

8-bit magnitude comparator

74LV688

AC CHARACTERISTICS

GND = 0V; $t_r = t_f = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 1\text{K}\Omega$

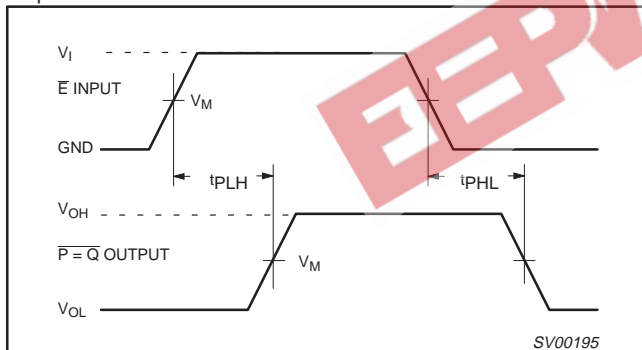
SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				-40 to +85 °C			-40 to +125 °C		
				$V_{CC}(\text{V})$	MIN	TYP ¹	MAX	MIN	
t_{PHL}/t_{PLH}	Propagation delay P_n, Q_n to $\overline{P=Q}$	2	1.2		100	–		–	ns
			2.0		28	45		57	
			2.7		20	32		40	
			3.0 to 3.6		16 ²	26		33	
			4.5 to 5.5		11 ²	18		22	
t_{PHL}/t_{PLH}	Propagation delay E to $\overline{P=Q}$	1	1.2		50	–		–	ns
			2.0		17	29		38	
			2.7		13	21		27	
			3.0 to 3.6		10 ²	17		22	
			4.5 to 5.5		7 ²	12		15	

NOTES:

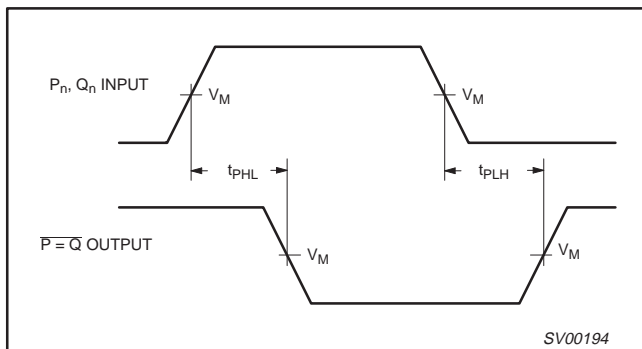
1. Unless otherwise stated, all typical values are at $T_{amb} = 25^\circ\text{C}$.
2. Typical value measured at $V_{CC} = 3.3\text{V}$.
3. Typical value measured at $V_{CC} = 5.0\text{V}$.

AC WAVEFORMS

$V_M = 1.5\text{V}$ at $V_{CC} \geq 2.7\text{V}$; $V_M = 0.5 V_{CC}$ at $V_{CC} < 2.7\text{V}$.
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

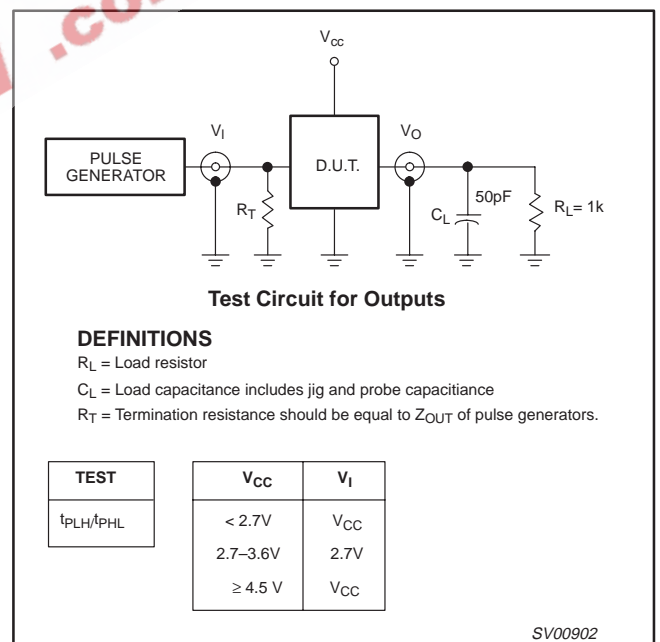


Waveform 1. Propagation delays from the enable input (E) to the equal-to output ($\overline{P=Q}$).



Waveform 2. Propagation delays from the inputs (P_n, Q_n) to the equal-to output ($\overline{P=Q}$).

TEST CIRCUIT



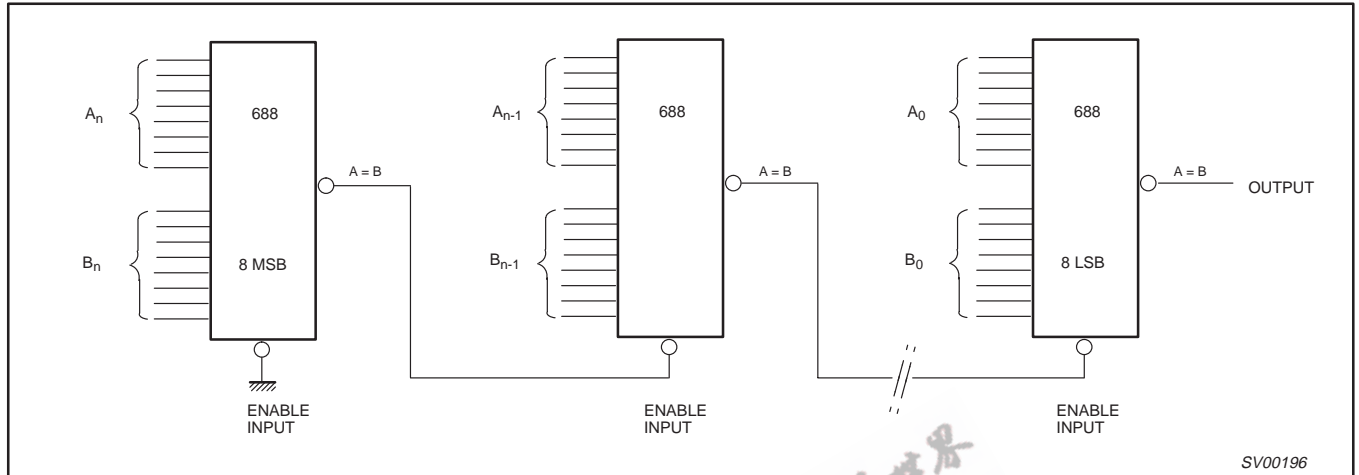
Waveform 3. Load circuitry for switching times

8-bit magnitude comparator

74LV688

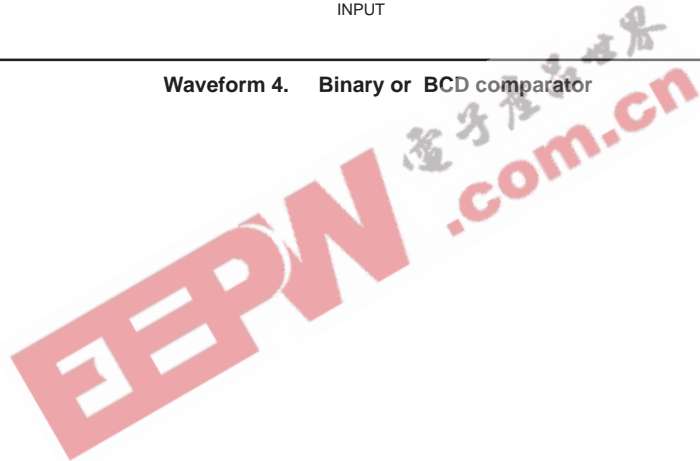
APPLICATION INFORMATION

Two or more "688" 8-bit magnitude comparators may be cascaded to compare binary or BCD numbers of more than 8 bits.



Waveform 4. Binary or BCD comparator

SV00196

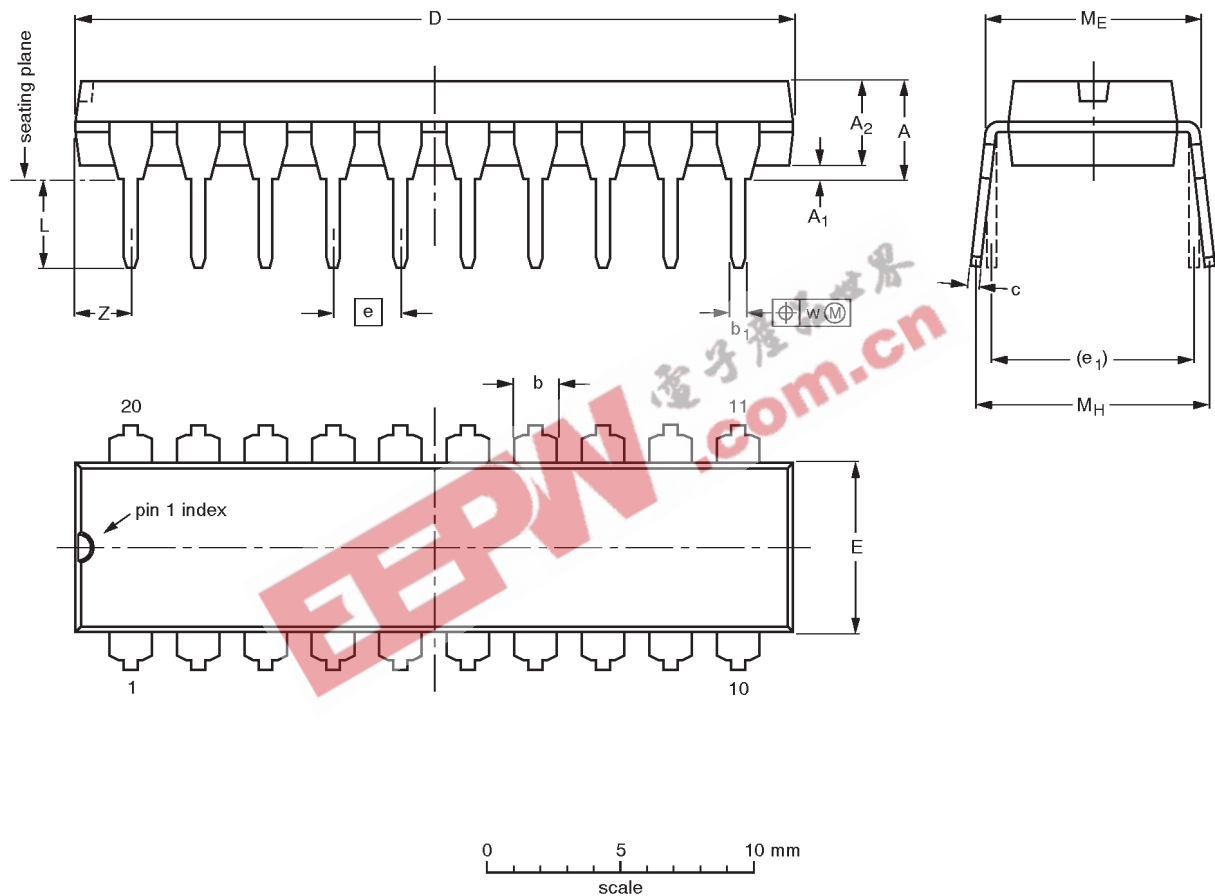


8-bit magnitude comparator

74LV688

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

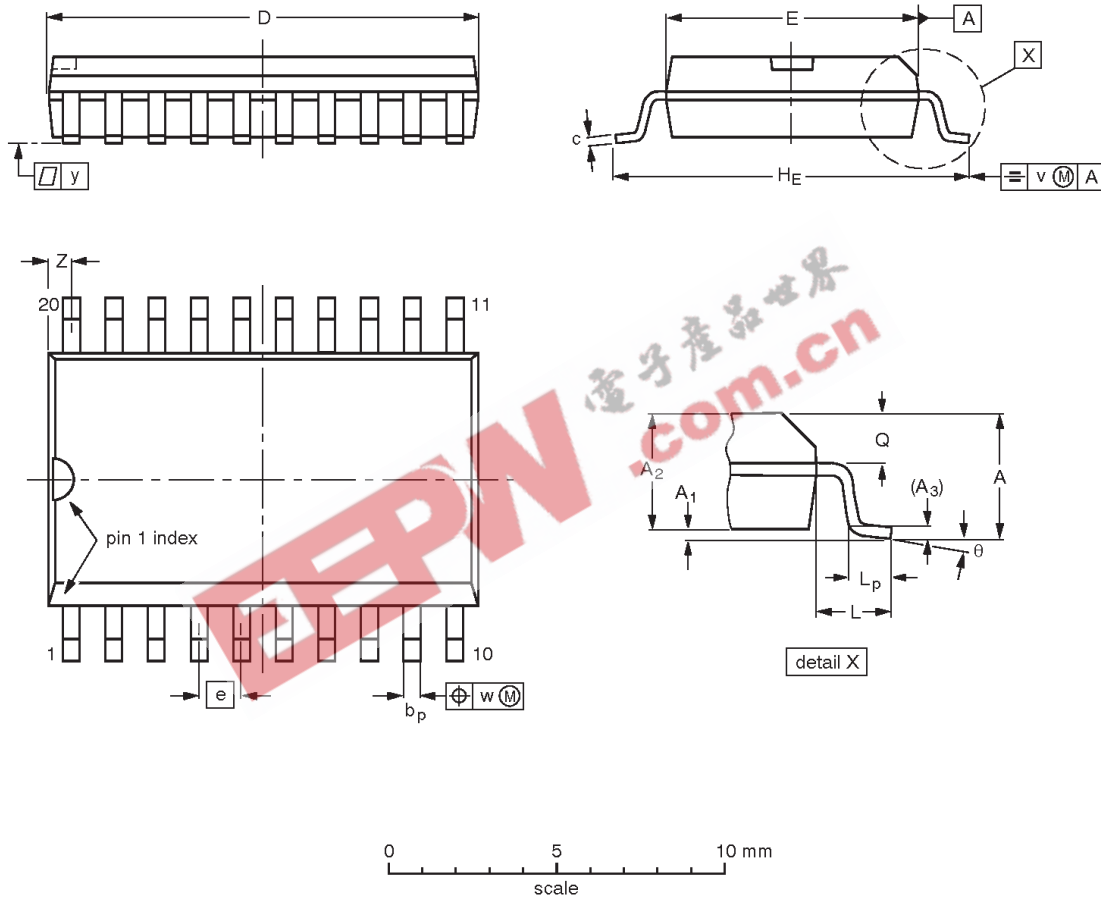
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

8-bit magnitude comparator

74LV688

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

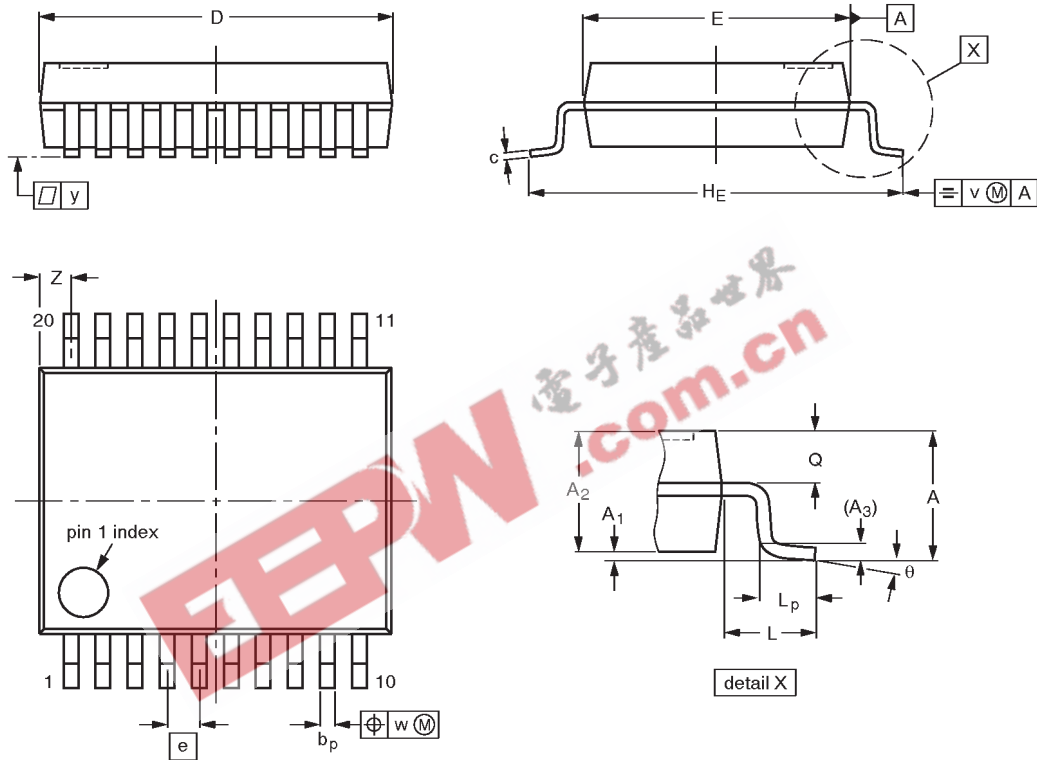
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				92-11-17 95-01-24

8-bit magnitude comparator

74LV688

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

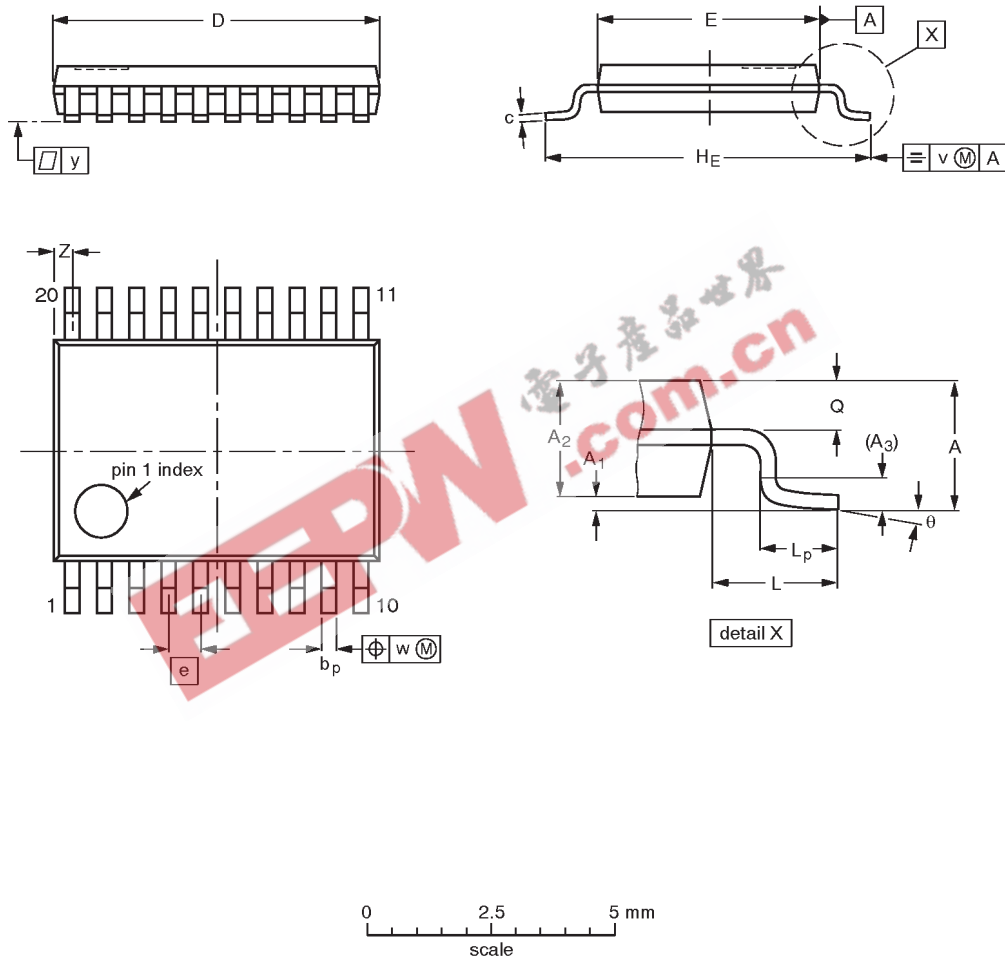
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				93-09-08 95-02-04

8-bit magnitude comparator

74LV688

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				93-06-16 95-02-04

8-bit magnitude comparator

74LV688

DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
<i>Product Specification</i>	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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