

## 74LVX74

### Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop

#### General Description

The LVX74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary ( $Q$ ,  $\bar{Q}$ ) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

#### Asynchronous Inputs:

- LOW input to  $\bar{S}_D$  (Set) sets  $Q$  to HIGH level
- LOW input to  $\bar{C}_D$  (Clear) sets  $Q$  to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$  makes both  $Q$  and  $\bar{Q}$  HIGH

#### Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance

#### Ordering Code:

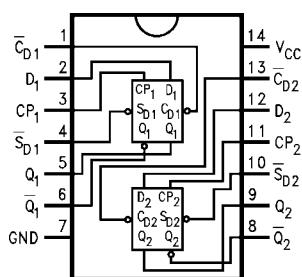
Order Number	Package Number	Package Description
74LVX74M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LVX74SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVX74MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74LVX74MTCX_NL (Note 1)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Pb-Free package per JEDEC J-STD-020B.

Note 1: "\_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

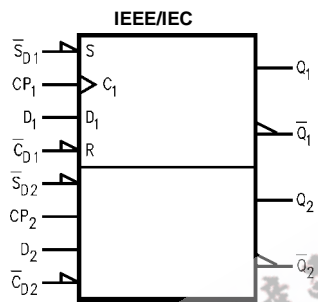
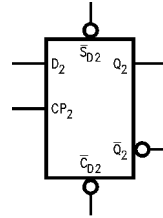
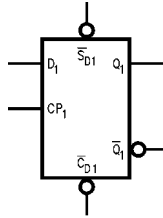
#### Connection Diagram



#### Pin Descriptions

Pin Names	Description
$D_1, D_2$	Data Inputs
$CP_1, CP_2$	Clock Pulse Inputs
$\bar{C}_D1, \bar{C}_D2$	Direct Clear Inputs
$\bar{S}_D1, \bar{S}_D2$	Direct Set Inputs
$Q_1, \bar{Q}_1, Q_2, \bar{Q}_2$	Outputs

Logic Symbols



Truth Table

(Each Half)

Inputs			Outputs		
$\bar{S}_D$	$\bar{C}_D$	CP	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↗	H	H	L
H	H	↗	L	L	H
H	H	L	X	Q <sub>0</sub>	$\bar{Q}_0$

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 ↗ = LOW-to-HIGH Clock Transition  
 Q<sub>0</sub>( $\bar{Q}_0$ ) = Previous Q( $\bar{Q}$ ) before LOW-to-HIGH Transition of Clock

**Absolute Maximum Ratings** (Note 2)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
DC Input Voltage ( $V_I$ )	-0.5V to 7V
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source	
or Sink Current ( $I_O$ )	$\pm 25$ mA
DC $V_{CC}$ or Ground Current	
( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation	180 mW

**Recommended Operating Conditions** (Note 3)

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
Input Voltage ( $V_I$ )	0V to 5.5V
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Input Rise and Fall Time ( $\Delta t/\Delta V$ )	0 ns/V to 100 ns/V

**Note 2:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 3:** Unused inputs must be held HIGH or LOW. They may not float.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$	$T_A = +25^\circ\text{C}$			$T_A = -40^\circ\text{C to } -85^\circ\text{C}$		Units	Conditions
			Min	Typ	Max	Min	Max		
$V_{IH}$	HIGH Level Input Voltage	2.0	1.5			1.5		V	
		3.0	2.0			2.0			
		3.6	2.4			2.4			
$V_{IL}$	LOW Level Input Voltage	2.0			0.5		0.5	V	
		3.0			0.8		0.8		
		3.6			0.8		0.8		
$V_{OH}$	HIGH Level Output Voltage	2.0	1.9	2.0		1.9		V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -50 \mu\text{A}$ $I_{OH} = -50 \mu\text{A}$ $I_{OH} = -4 \text{mA}$
		3.0	2.9	3.0		2.9			
		3.0	2.58			2.48			
$V_{OL}$	LOW Level Output Voltage	2.0		0.0	0.1		0.1	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 50 \mu\text{A}$ $I_{OL} = 50 \mu\text{A}$ $I_{OL} = 4 \text{mA}$
		3.0		0.0	0.1		0.1		
		3.0			0.36		0.44		
$I_{IN}$	Input Leakage Current	3.6			$\pm 0.1$		$\pm 1.0$	$\mu\text{A}$	$V_{IN} = 5.5V$ or GND
$I_{CC}$	Quiescent Supply Current	3.6			2.0		20.0	$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND

**Noise Characteristics** (Note 4)

Symbol	Parameter	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$		Units	$C_L$ (pF)
			Typ	Limit		
$V_{OLP}$	Quiet Output Maximum Dynamic $V_{OL}$	3.3	0.3	0.5	V	50
$V_{OLV}$	Quiet Output Minimum Dynamic $V_{OL}$	3.3	-0.3	-0.5	V	50
$V_{IHD}$	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
$V_{ILD}$	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

**Note 4:** Input  $t_r = t_f = 3$  ns

AC Electrical Characteristics										
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units	C <sub>L</sub> (pF)	
			Min	Typ	Max	Min	Max			
t <sub>PLH</sub>	Propagation Delay CP <sub>n</sub> to Q <sub>n</sub> or $\bar{Q}_n$	2.7		7.3	15	1.0	18.5	ns	15	
t <sub>PHL</sub>				9.8	18.5	1.0	22		50	
		3.3 ± 0.3			5.7	9.7	1.0		11.5	15
					8.2	13.2	1.0		15	50
t <sub>PLH</sub>	Propagation Delay $\bar{C}_{Dn}$ to $\bar{S}_{Dn}$ to Q <sub>n</sub> or $\bar{Q}_n$	2.7		8.4	15.6	1.0	18.5	ns	15	
t <sub>PHL</sub>				10.9	19.1	1.0	22		50	
		3.3 ± 0.3			6.6	10.1	1.0		12	15
					9.1	13.6	1.0		15.5	50
t <sub>W</sub>	CP <sub>n</sub> or $\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ Pulse Width	2.7	8.5			10		ns		
		3.3 ± 0.3	6			7				
t <sub>S</sub>	Setup Time D <sub>n</sub> to CP <sub>n</sub>	2.7	8.0			9.5		ns		
		3.3 ± 0.3	5.5			6.5				
t <sub>H</sub>	Hold Time D <sub>n</sub> to CP <sub>n</sub>	2.7	0.5			0.5		ns		
		3.3 ± 0.3	0.5			0.5				
t <sub>REC</sub>	Recovery Time $\bar{C}_{Pn}$ or $\bar{S}_{Dn}$ to CP <sub>n</sub>	2.7	6.5			7.5		ns		
		3.3 ± 0.3	5.0			5.0				
f <sub>MAX</sub>	Maximum Clock Frequency	2.7	55	135		50		MHz	15	
			45	60		40			50	
		3.3 ± 0.3	95	145		80			15	
			60	85		50			50	
t <sub>OSLH</sub>	Output to Output Skew (Note 5)	2.7				1.5		ns	50	
t <sub>OSHL</sub>		3.3				1.5				

**Note 5:** Parameter guaranteed by design.  $t_{OSLH} = |t_{PLHm} - t_{PLHl}|$ ;  $t_{OSHL} = |t_{PHLm} - t_{PHLl}|$

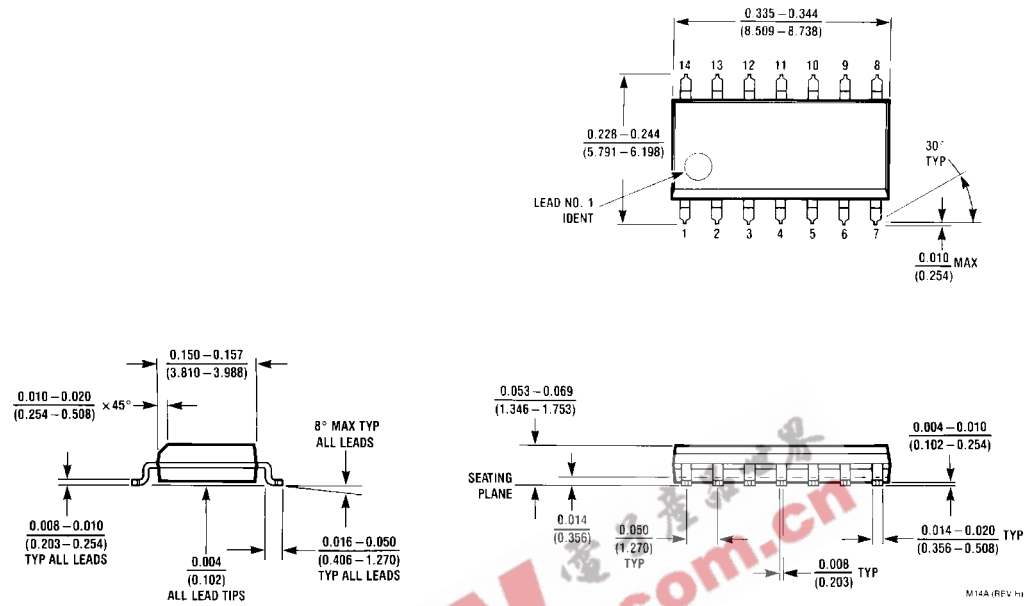
### Capacitance

Symbol	Parameter	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units
		Min	Typ	Max	Min	Max	
C <sub>IN</sub>	Input Capacitance		4	10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 6)		25				pF

**Note 6:** C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

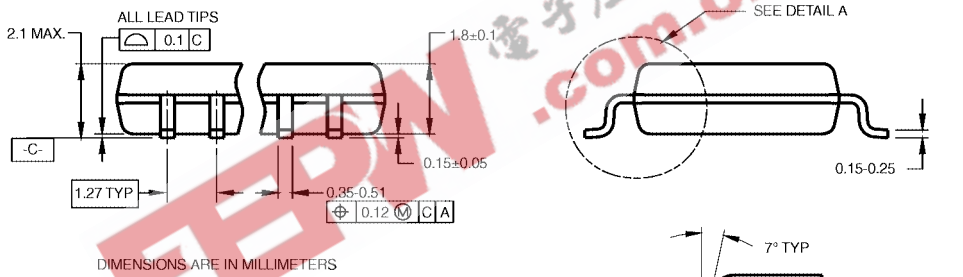
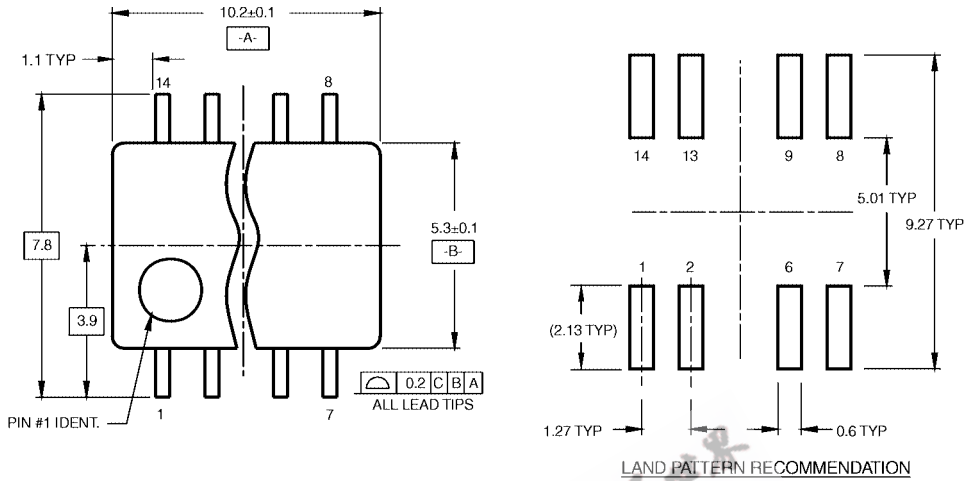
Average operating current can be obtained by the equation:  $I_{CC(opr)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{2 \text{ (per F/F)}}$

**Physical Dimensions** inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

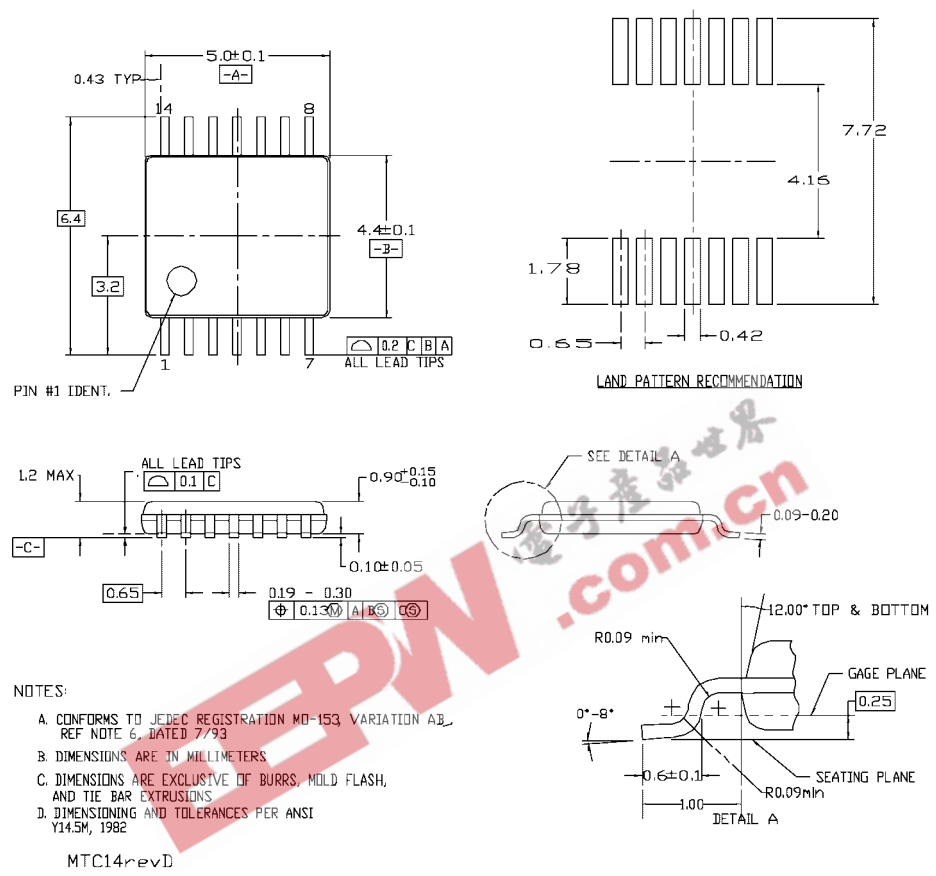


- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

**Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M14D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93
  - B. DIMENSIONS ARE IN MILLIMETERS
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
  - D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- MTC14revD

**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14**

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