

74LCX541

Low Voltage Octal Buffer/Line Driver with 5V Tolerant Inputs and Outputs

General Description

The LCX541 is an octal buffer/line driver designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers. The LCX541 is a non inverting option of the LCX540.

This device is similar in function to the LCX244 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes this device especially useful as an output port for microprocessors, allowing ease of layout and greater PC board density.

The LCX541 is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The LCX541 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant input and outputs
- 2.3V–3.6V V_{CC} specifications provided
- 6.5 ns t_{PD} max ($V_{CC} = 3.3V$), 10 μA I_{CC} max
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- ± 24 mA output drive ($V_{CC} = 3.0V$)
- Implements patented noise/ EMI reduction circuitry
- Latch-up performance exceeds JEDEC 78 conditions
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V
- Leadless Pb-Free DQFN package

Note 1: To ensure the high-impedance state during power up or down, \overline{OE} should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

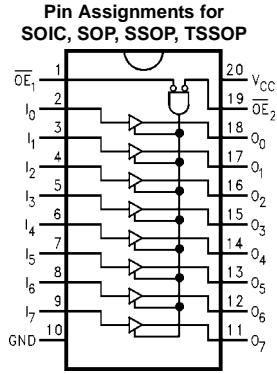
Order Number	Package Number	Package Description
74LCX541WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LCX541SJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX541BQX (Preliminary) (Note 2)	MLP020B	Pb-Free 20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 4.5mm
74LCX541MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74LCX541MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74LCX541MTC_NL (Note 3)	MTC20	Pb-Free 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

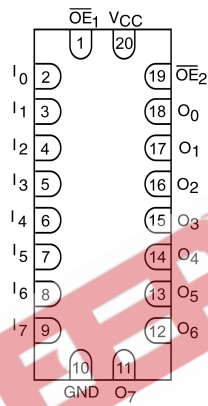
Note 2: DQFN package available in Tape and Reel only.

Note 3: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

Connection Diagrams

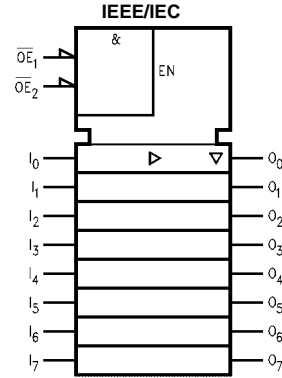


Pad Assignment for DQFN



(Top View)

Logic Symbol



Pin Descriptions

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	3-STATE Output Enable Inputs
I_0, I_7	Inputs
O_0, O_7	Outputs

Truth Table

Inputs			Outputs
\overline{OE}_1	\overline{OE}_2	I	O_n
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

Absolute Maximum Ratings (Note 4)						
Symbol	Parameter	Value	Conditions	Units		
V_{CC}	Supply Voltage	-0.5 to +7.0		V		
V_I	DC Input Voltage	-0.5 to +7.0		V		
V_O	DC Output Voltage	-0.5 to +7.0 -0.5 to $V_{CC} + 0.5$	Output in 3-STATE Output in HIGH or LOW State (Note 5)	V		
I_{IK}	DC Input Diode Current	-50	$V_I < GND$	mA		
I_{OK}	DC Output Diode Current	-50 +50	$V_O < GND$ $V_O > V_{CC}$	mA		
I_O	DC Output Source/Sink Current	± 50		mA		
I_{CC}	DC Supply Current per Supply Pin	± 100		mA		
I_{GND}	DC Ground Current per Ground Pin	± 100		mA		
T_{STG}	Storage Temperature	-65 to +150		°C		
Recommended Operating Conditions (Note 6)						
Symbol	Parameter	Min	Max	Units		
V_{CC}	Supply Voltage	Operating	2.0	3.6	V	
		Data Retention	1.5	3.6		
V_I	Input Voltage	0	5.5	V		
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V	
		3-STATE	0	5.5		
I_{OH}/I_{OL}	Output Current	$V_{CC} = 3.0V - 3.6V$		± 24	mA	
		$V_{CC} = 2.7V - 3.0V$		± 12		
		$V_{CC} = 2.3V - 2.7V$		± 8		
T_A	Free-Air Operating Temperature	-40	85	°C		
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V - 2.0V$, $V_{CC} = 3.0V$	0	10	ns/V		
<p>Note 4: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.</p> <p>Note 5: I_O Absolute Maximum Rating must be observed.</p> <p>Note 6: Unused inputs or I/O's must be held HIGH or LOW. They may not float.</p>						
DC Electrical Characteristics						
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40^\circ C$ to $+85^\circ C$		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.3 - 2.7	1.7		V
			2.7 - 3.6	2.0		
V_{IL}	LOW Level Input Voltage		2.3 - 2.7		0.7	V
			2.7 - 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100\mu A$	2.3 - 3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -8\text{ mA}$	2.3	1.8		
		$I_{OH} = -12\text{ mA}$	2.7	2.2		
		$I_{OH} = -18\text{ mA}$	3.0	2.4		
		$I_{OH} = -24\text{ mA}$	3.0	2.2		
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100\mu A$	2.3 - 3.6		0.2	V
		$I_{OL} = 8\text{ mA}$	2.3		0.6	
		$I_{OL} = 12\text{ mA}$	2.7		0.4	
		$I_{OL} = 16\text{ mA}$	3.0		0.4	
		$I_{OL} = 24\text{ mA}$	3.0		0.55	
I_I	Input Leakage Current	$0 \leq V_I \leq 5.5V$	2.3 - 3.6		± 5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or $V_O = 5.5V$	0		10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3 - 3.6		10	μA
		$3.6V \leq V_I$, $V_O \leq 5.5V$ (Note 7)	2.3 - 3.6		± 10	
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} = 0.6V$	2.3 - 3.6		500	μA

DC Electrical Characteristics (Continued)

Note 7: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}, R_L = 500\Omega$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5V \pm 0.2V$		
		$C_L = 50\text{ pF}$		$C_L = 50\text{ pF}$		$C_L = 30\text{ pF}$		
		Min	Max	Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.5	6.5	1.5	7.5	1.5	7.8	ns
t_{PLH}		1.5	6.5	1.5	7.5	1.5	7.8	
t_{PZL}	Output Enable Time	1.5	8.5	1.5	9.5	1.5	10.5	ns
t_{PZH}		1.5	8.5	1.5	9.5	1.5	10.5	
t_{PLZ}	Output Disable Time	1.5	7.5	1.5	8.5	1.5	9.0	ns
t_{PHZ}		1.5	7.5	1.5	8.5	1.5	9.0	
t_{OSHL}	Output to Output Skew (Note 8)		1.0					ns
t_{OSLH}			1.0					

Note 8: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25^\circ\text{C}$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50\text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$	3.3	0.8	V
		$C_L = 30\text{ pF}, V_{IH} = 2.5V, V_{IL} = 0V$	2.5	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50\text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$	3.3	-0.8	V
		$C_L = 30\text{ pF}, V_{IH} = 2.5V, V_{IL} = 0V$	2.5	-0.6	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = \text{Open}, V_I = 0V \text{ or } V_{CC}$	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V, V_I = 0V \text{ or } V_{CC}$	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V, V_I = 0V \text{ or } V_{CC}, f = 10\text{ MHz}$	25	pF

AC Loading and Waveforms Generic for LCX Family

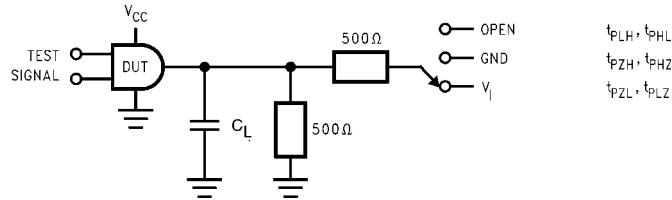
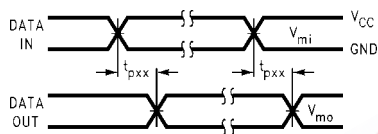
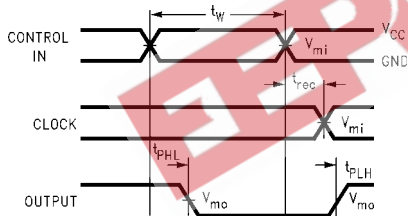


FIGURE 1. AC Test Circuit
(C_L includes probe and jig capacitance)

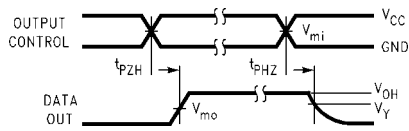
Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$ $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
t_{PZH}, t_{PHZ}	GND



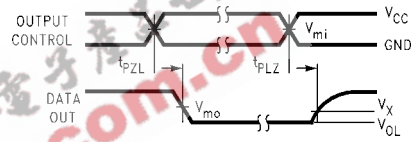
Waveform for Inverting and Non-Inverting Functions



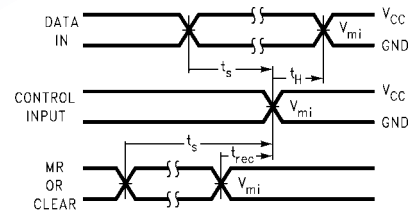
Propagation Delay, Pulse Width and t_{rec} Waveforms



3-STATE Output High Enable and Disable Times for Logic



3-STATE Output Low Enable and Disable Times for Logic



Setup Time, Hold Time and Recovery Time for Logic

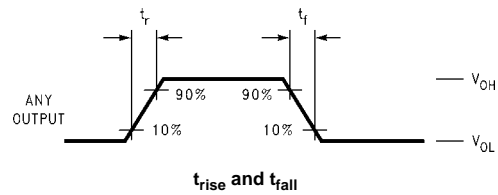
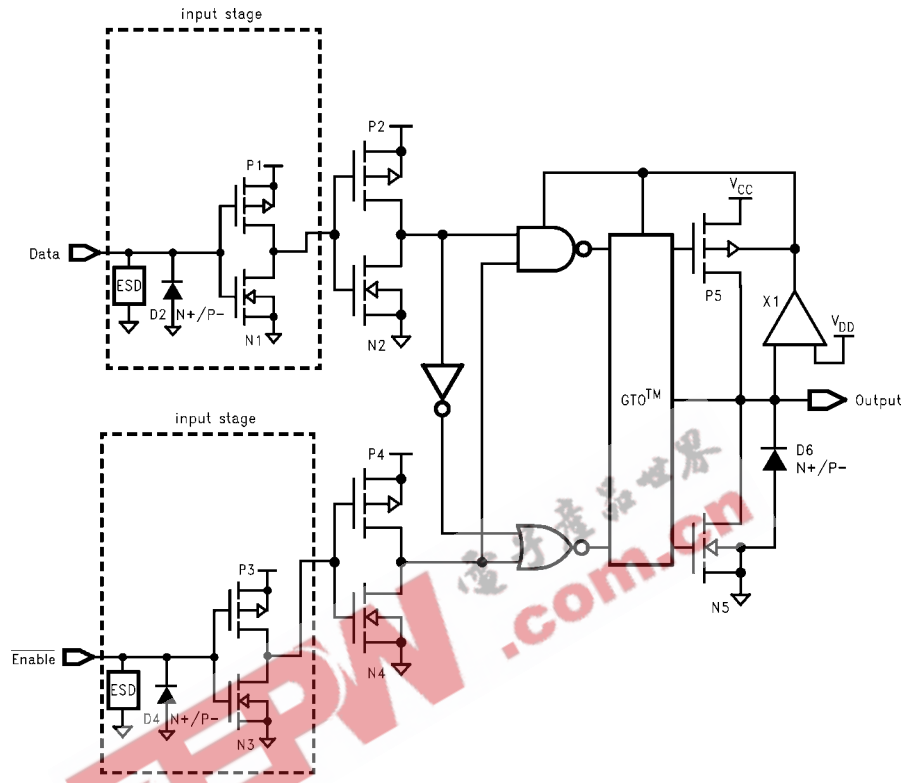


FIGURE 2. Waveforms
(Input Pulse Characteristics; $f = 1\text{MHz}$, $t_r = t_f = 3\text{ns}$)

Symbol	V_{CC}		
	$3.3V \pm 0.3V$	$2.7V$	$2.5V \pm 0.2V$
V_{mi}	1.5V	1.5V	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
V_y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

Schematic Diagram Generic for LCX Family

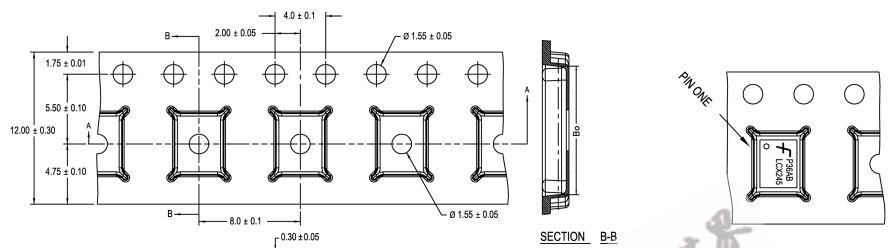


Tape and Reel Specification

Tape Format for DQFN

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)

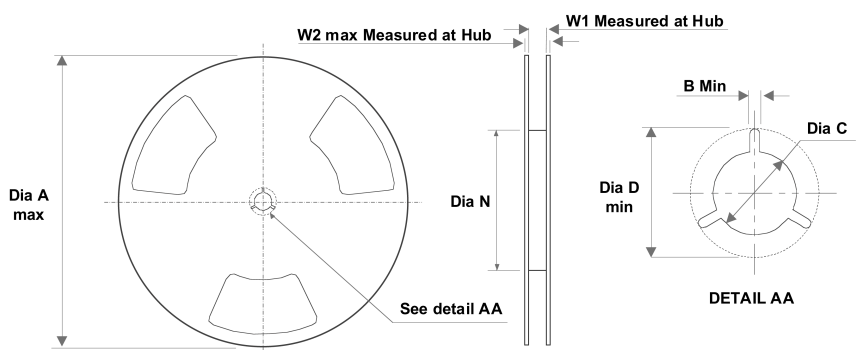


PKG. SIZE	DIM.A _o	DIM.B _o	DIM.K _o
3.5 X 4.5	3.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
3.0 X 3.0	3.3 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 4.5	2.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
2.5 X 3.5	2.8 ± 0.1	3.8 ± 0.1	0.9 ± 0.1
2.5 X 3.0	2.8 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 2.5	2.8 ± 0.1	2.8 ± 0.1	0.9 ± 0.1

DIMENSIONS ARE IN MILLIMETERS

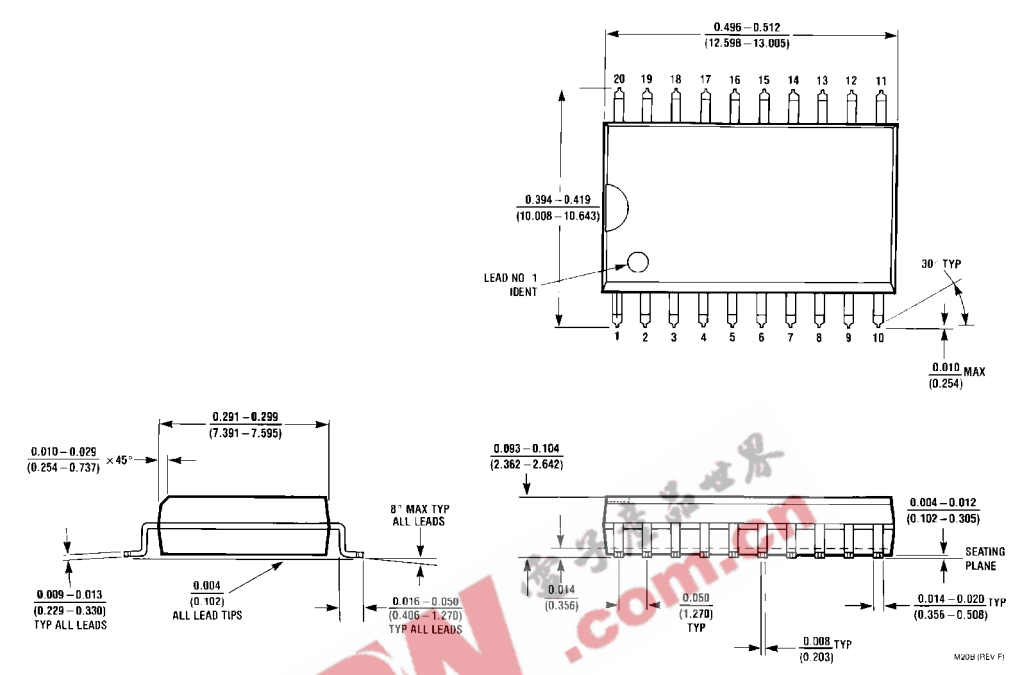
- NOTES: unless otherwise specified
- Cumulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
 - Smallest allowable bending radius.
 - Thru hole inside cavity is centered within cavity.
 - Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
 - A_o and B_o measured on a plane 0.120[0.30] above the bottom of the pocket.
 - K_o measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
 - Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
 - Controlling dimension is millimeter. Dimension in inches rounded.

REEL DIMENSIONS inches (millimeters)



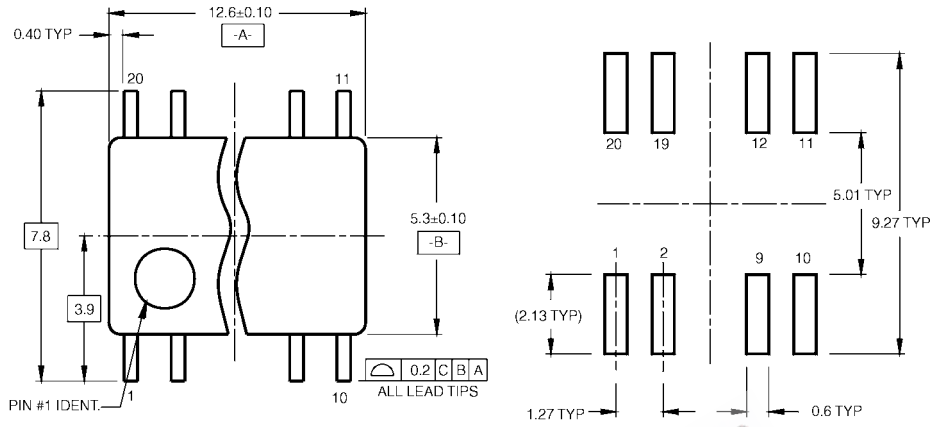
Tape Size	A	B	C	D	N	W1	W2
12 mm	13.0 (330.0)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.488 (12.4)	0.724 (18.4)

Physical Dimensions inches (millimeters) unless otherwise noted

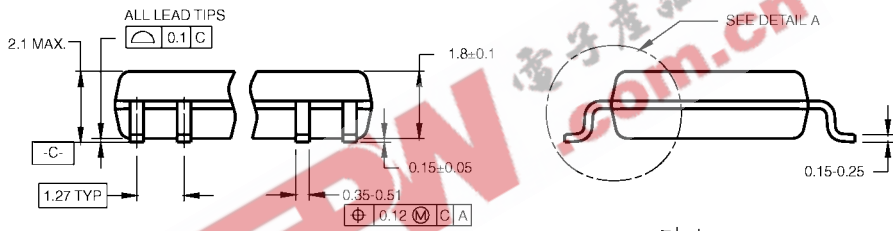


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION

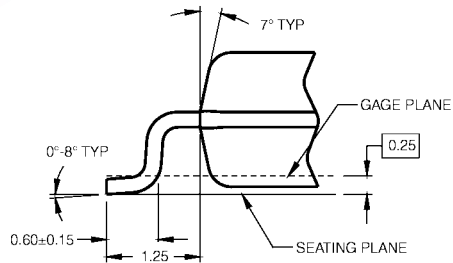


DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

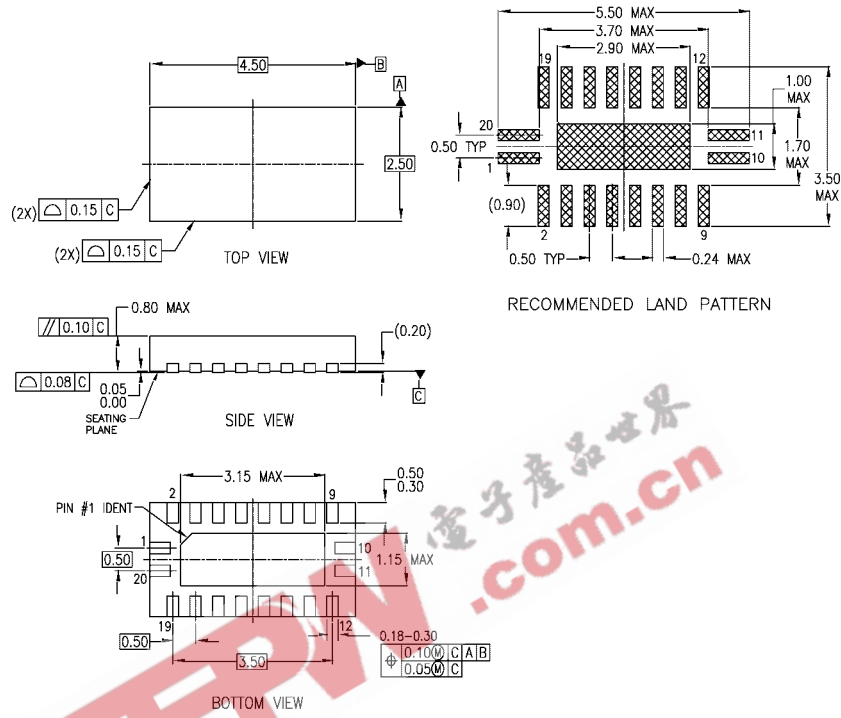
M20DRevB1



DETAIL A

**Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



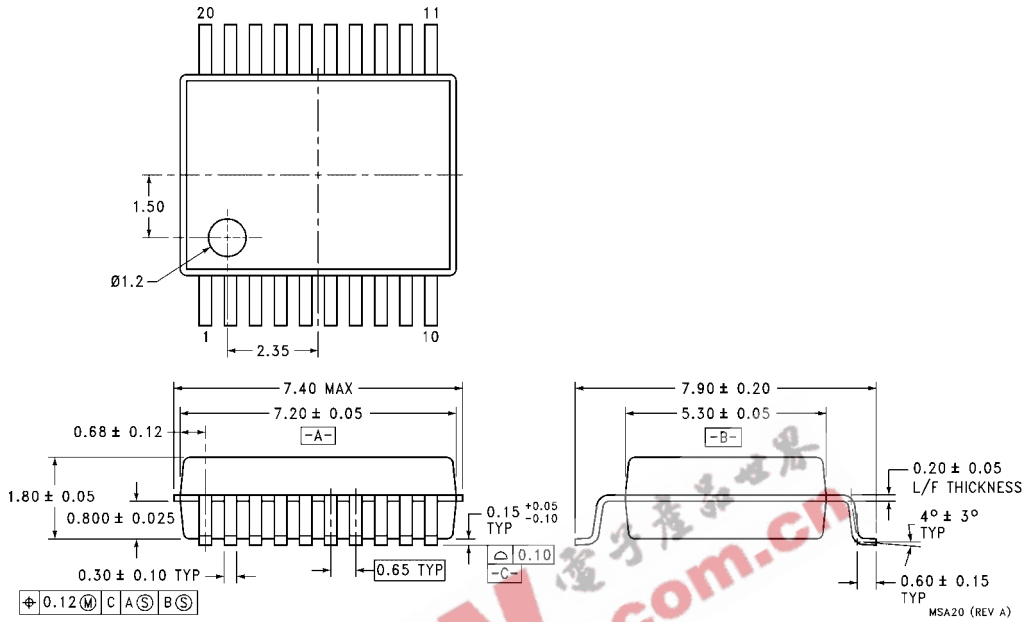
NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AC
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP020BrevA

Pb-Free 20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 4.5mm Package Number MLP020B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
Package Number MSA20**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

PIN #1 IDENT.

LAND PATTERN RECOMMENDATION

DIMENSIONS ARE IN MILLIMETERS

NOTES:

- CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REV D1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20

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