FAIRCHILD

SEMICONDUCTOR™

November 1999
Revised August 2003

74VCXH16244
Low Voltage 16-Bit Buffer/Line Driver with Bushold

General Description

The VCXH16244 contains sixteen non-inverting buffers with 3-STATE outputs to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble (4-bit) controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

The VCXH16244 data inputs include active bushold circuitry, eliminating the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level.

The 74VCXH16244 is designed for low voltage (1.2V to 3.6V) V_{CC} applications with output capability up to 3.6V.

The 74VCXH16244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

■ 1.2V to 3.6V V_{CC} supply operation

■ 3.6V tolerant control inputs and outputs

■ Bushold on data inputs eliminating the need for external pull-up/pull-down resistors

■ t_{PD}
   2.5 ns max for 3.0V to 3.6V V_{CC}

■ Static Drive (I_{OH}/I_{OL})
   ±24 mA @ 3.0V V_{CC}

■ Uses patented noise/EMI reduction circuitry

■ Latch-up performance exceeds 300 mA

■ ESD performance:
   Human body model > 2000V
   Machine model > 200V

■ Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)
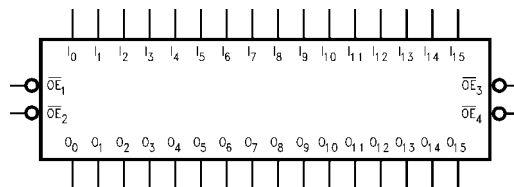
Ordering Code:

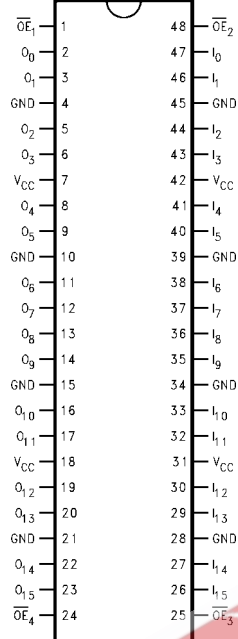| Order Number	Package Number	Package Description
74VCXH16244G (Note 1)(Note 2)	BGA54A (Preliminary)	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74VCXH16244MTD (Note 2)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Note 1: Ordering Code "G" indicates Tray.

Note 2: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
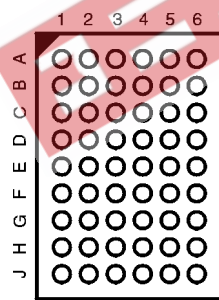
Logic Symbol

Connection Diagrams

74VCXH16244

Pin Assignment for TSSOP

$\overline{OE}_1$	1		48	$\overline{OE}_2$
O_0	2		47	I_0
O_1	3		46	I_1
GND	4		45	GND
O_2	5		44	I_2
O_3	6		43	I_3
V_{CC}	7		42	V_{CC}
O_4	8		41	I_4
O_5	9		40	I_5
GND	10		39	GND
O_6	11		38	I_6
O_7	12		37	I_7
O_8	13		36	I_8
O_9	14		35	I_9
GND	15		34	GND
O_{10}	16		33	I_{10}
O_{11}	17		32	I_{11}
V_{CC}	18		31	V_{CC}
O_{12}	19		30	I_{12}
O_{13}	20		29	I_{13}
GND	21		28	GND
O_{14}	22		27	I_{14}
O_{15}	23		26	I_{15}
$\overline{OE}_4$	24		25	$\overline{OE}_3$

Pin Assignment for FBGA

(Top Thru View)

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$I_0–I_{15}$	Bushold Inputs
$O_0–O_{15}$	Outputs
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
A	O_0	NC	$\overline{OE}_1$	$\overline{OE}_2$	NC	I_0
B	O_2	O_1	NC	NC	I_1	I_2
C	O_4	O_3	V_{CC}	V_{CC}	I_3	I_4
D	O_6	O_5	GND	GND	I_5	I_6
E	O_8	O_7	GND	GND	I_7	I_8
F	O_{10}	O_9	GND	GND	I_9	I_{10}
G	O_{12}	O_{11}	V_{CC}	V_{CC}	I_{11}	I_{12}
H	O_{14}	O_{13}	NC	NC	I_{13}	I_{14}
J	O_{15}	NC	$\overline{OE}_4$	$\overline{OE}_3$	NC	I_{15}

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$I_0–I_3$	$O_0–O_3$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_4-I_7	O_4-O_7
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8-I_{11}	$O_8–O_{11}$
L	L	L
L	H	H
H	X	Z

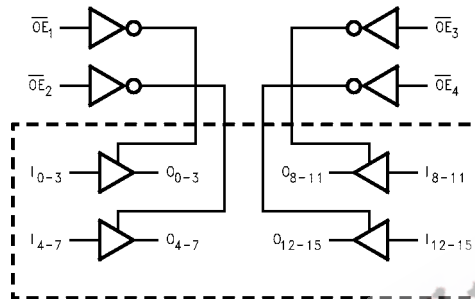| Inputs		Outputs
$\overline{OE}_4$	I_{12}-I_{15}	O_{12}-O_{15}
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs may not float)
Z = High Impedance

Functional Description

The 74VCXH16244 contains sixteen non-inverting buffers with 3-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of each other. The control pins may be shorted together to obtain full 16-bit operation.The 3-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW, the outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the inputs.

Logic Diagram

Absolute Maximum Ratings(Note 3)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to +4.6V
Output Voltage (V_O)	
Outputs 3-STATED	−0.5V to +4.6V
Outputs Active (Note 4)	−0.5V to V_{CC} +0.5V
DC Input Diode Current (I_{IK}) $V_I < 0V$	−50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	−50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	±50 mA
DC V_{CC} or GND Current per	
Supply Pin (I_{CC} or GND)	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 5)

Power Supply	
Operating	1.2V to 3.6V
Input Voltage	−0.3V to +3.6V
Output Voltage (V_O)	
Output in Active States	0.0V to V_{CC}
Output in 3-STATE	0.0V to 3.6V
Output Current in I_{OH}/I_{OL}	
V_{CC} = 3.0V to 3.6V	±24 mA
V_{CC} = 2.3V to 2.7V	±18 mA
V_{CC} = 1.65V to 2.3V	±6 mA
V_{CC} = 1.4V to 1.6V	±2 mA
V_{CC} = 1.2V	±100 µA
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

Note 3: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: I_O Absolute Maximum Rating must be observed.

Note 5: Floating or unused control inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7 - 3.6	2.0		
			2.3 - 2.7	1.6		
			1.65 - 2.3	0.65 x V_{CC}		V
			1.4 - 1.6	0.65 x V_{CC}		
			1.2	0.65 x V_{CC}		
V_{IL}	LOW Level Input Voltage		2.7 - 3.6		0.8	
			2.3 - 2.7		0.7	
			1.65 - 2.3		0.35 x V_{CC}	V
			1.4 - 1.6		0.35 x V_{CC}	
			1.2		0.05 x V_{CC}	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA	2.7 - 3.6	V_{CC} - 0.2		
		I_{OH} = −12 mA	2.7	2.2		
		I_{OH} = −18 mA	3.0	2.4		
		I_{OH} = −24 mA	3.0	2.2		
		I_{OH} = −100 µA	2.3 - 2.7	V_{CC} - 0.2		
		I_{OH} = −6 mA	2.3	2.0		
		I_{OH} = −12 mA	2.3	1.8		V
		I_{OH} = −18 mA	2.3	1.7		
		I_{OH} = −100 µA	1.65 - 2.3	V_{CC} - 0.2		
		I_{OH} = −6 mA	1.65	1.25		
		I_{OH} = −100 µA	1.4 - 1.6	V_{CC} - 0.2		
		I_{OH} = −2 mA	1.4	1.05		
		I_{OH} = −100 µA	1.2	V_{CC} - 0.2		

DC Electrical Characteristics (Continued)

Symbol	Parameter		Conditions	V$_{CC}$ (V)	Min	Max	Units
V$_{OL}$	LOW Level Output Voltage		I$_{OL}$ = 100 µA	2.7 - 3.6		0.2	V
			I$_{OL}$ = 12 mA	2.7		0.4	
			I$_{OL}$ = 18 mA	3.0		0.4	
			I$_{OL}$ = 24 mA	3.0		0.55	
			I$_{OL}$ = 100 µA	2.3 - 2.7		0.2	
			I$_{OL}$ = 12 mA	2.3		0.4	
			I$_{OL}$ = 18 mA	2.3		0.6	
			I$_{OL}$ = 100 µA	1.65 - 2.3		0.2	
			I$_{OL}$ = 6 mA	1.65		0.3	
			I$_{OL}$ = 100 µA	1.4 - 1.6		0.2	
			I$_{OL}$ = 2 mA	1.4		0.35	
			I$_{OL}$ = 100 µA	1.2		0.05	
I$_I$	Input Leakage Current	Control Pins	0 ≤ V$_I$ ≤ 3.6V	1.2 - 3.6		±5.0	µA
		Data Pins	V$_I$ = V$_{CC}$ or GND	1.2 - 3.6		±5.0	µA
I$_{I(HOLD)}$	Bushold Input Minimum Drive Hold Current		V$_{IN}$ = 0.8V	3.0	75.0		µA
			V$_{IN}$ = 2.0V	3.0	−75.0		
			V$_{IN}$ = 0.7V	2.3	45.0		
			V$_{IN}$ = 1.6V	2.3	−45.0		
			V$_{IN}$ = 0.57V	1.65	25.0		
			V$_{IN}$ = 1.07V	1.65	−25.0		
I$_{I(OD)}$	Bushold Input Over-Drive Current to Change State		(Note 6)	3.6	450		µA
			(Note 7)	3.6	−450		
			(Note 6)	2.7	300		
			(Note 7)	2.7	−300		
			(Note 6)	1.95	200		
			(Note 7)	1.95	−200		
I$_{OZ}$	3-STATE Output Leakage		0 ≤ V$_O$ ≤ 3.6V V$_I$ = V$_{IH}$ or V$_{IL}$	2.7 - 3.6		±10.0	µA
I$_{OFF}$	Power-OFF Leakage Current		0 ≤ (V$_O$) ≤ 3.6V	0		10.0	µA
I$_{CC}$	Quiescent Supply Current		V$_I$ = V$_{CC}$ or GND	1.2 - 3.6		20.0	µA
			V$_{CC}$ ≤ (V$_O$) ≤ 3.6V (Note 8)	1.2 - 3.6		±20.0	µA
ΔI$_{CC}$	Increase in I$_{CC}$ per Input		V$_{IH}$ = V$_{CC}$ − 0.6V	2.7 - 3.6		750	µA

Note 6: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 7: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 8: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 9)

Symbol	Parameter	Conditions	V_CC (V)	T_A = −40°C to +85°C Min	T_A = −40°C to +85°C Max	Units	Figure Number
t_{PHL} t_{PLH}	Propagation Delay	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3	0.8	2.5	ns	Figures 1, 2
			2.5 ± 0.2	1.0	3.0		
			1.8 ± 0.15	1.5	6.0		
		$C_L = 15$ pF, $R_L = 2$ kΩ	1.5 ± 0.1	1.0	12.0		Figures 5, 6
			1.2	1.5	30.0		
t_{PZL} t_{PZH}	Output Enable Time	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3	0.8	3.5	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	4.1		
			1.8 ± 0.15	1.5	8.2		
		$C_L = 15$ pF, $R_L = 2$ kΩ	1.5 ± 0.1	1.0	16.4		Figures 5, 7, 8
			1.2	1.5	41.0		
t_{PLZ} t_{PHZ}	Output Disable Time	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3	0.8	3.5	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	3.8		
			1.8 ± 0.15	1.5	6.8		
		$C_L = 15$ pF, $R_L = 2$ kΩ	1.5 ± 0.1	1.0	13.6		Figures 5, 7, 8
			1.2	1.5	34.0		
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 10)	$C_L = 30$ pF, $R_L = 500\Omega$	3.3 ± 0.3		0.5	ns	
			2.5 ± 0.2		0.5		
			1.8 ± 0.15		0.75		
		$C_L = 15$ pF, $R_L = 2$ kΩ	1.5 ± 0.1		1.5		
			1.2		1.5		

Note 9: For $C_L = 50$pF, add approximately 300 ps to the AC maximum specification.

Note 10: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_CC (V)	T_A = +25°C Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0$V	1.8	0.25	V
			2.5	0.6	
			3.3	0.8	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0$V	1.8	−0.25	V
			2.5	−0.6	
			3.3	−0.8	
V_{OHV}	Quiet Output Dynamic Valley V_{OH}	$C_L = 30$ pF, $V_{IH} = V_{CC}$, $V_{IL} = 0$V	1.8	1.5	V
			2.5	1.9	
			3.3	2.2	

Capacitance

Symbol	Parameter	Conditions	T_A = +25°C Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = 1.8$, 2.5V or 3.3V, $V_I = 0$V or V_{CC}	6.0	pF
C_{OUT}	Output Capacitance	$V_I = 0$V or V_{CC}, $V_{CC} = 1.8$V, 2.5V or 3.3V	7.0	pF
C_{PD}	Power Dissipation Capacitance	$V_I = 0$V or V_{CC}, f = 10 MHz, $V_{CC} = 1.8$V, 2.5V or 3.3V	20.0	pF

AC Loading and Waveforms (V$_{CC}$ 3.3V $\pm$ 0.3V to 1.8V $\pm$ 0.15V)
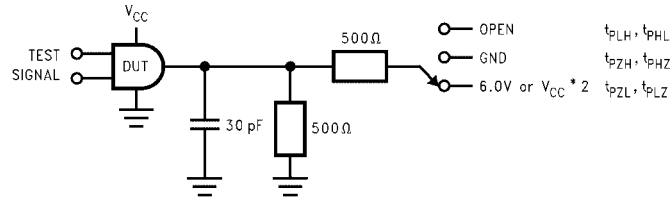
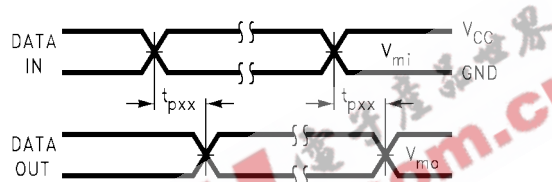| TEST	SWITCH
t$_{PLH}$, t$_{PHL}$	Open
t$_{PZL}$, t$_{PLZ}$	6V at V$_{CC}$ = 3.3 $\pm$ 0.3V; V$_{CC}$ x 2 at V$_{CC}$ = 2.5 $\pm$ 0.2V; 1.8V $\pm$ 0.15V
t$_{PZH}$, t$_{PHZ}$	GND

FIGURE 1. AC Test Circuit

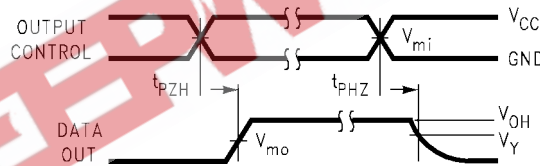**FIGURE 2. Waveform for Inverting and Non-Inverting Functions**

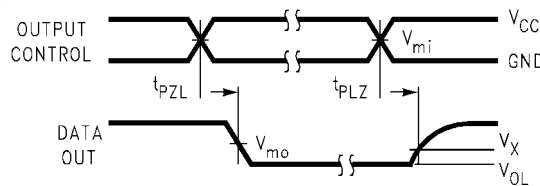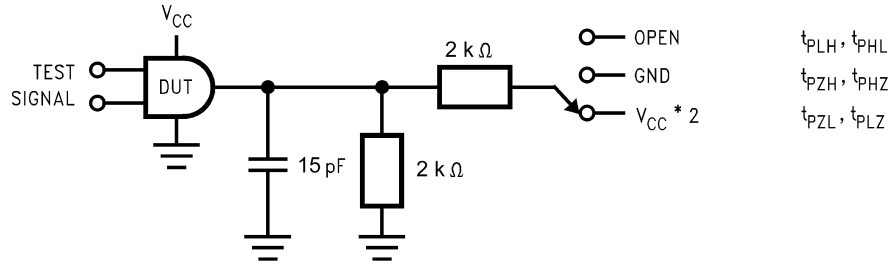**FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic**

FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	V$_{CC}$		
	3.3V $\pm$ 0.3V	2.5V $\pm$ 0.2V	1.8V $\pm$ 0.15V
V$_{mi}$	1.5V	V$_{CC}$/2	V$_{CC}$/2
V$_{mo}$	1.5V	V$_{CC}$/2	V$_{CC}$/2
V$_X$	V$_{OL}$ + 0.3V	V$_{OL}$ + 0.15V	V$_{OL}$ + 0.15V
V$_Y$	V$_{OH}$ − 0.3V	V$_{OH}$ − 0.15V	V$_{OH}$ − 0.15V

AC Loading and Waveforms (V$_{CC}$ 1.5 $\pm$ 0.1V to 1.2V)

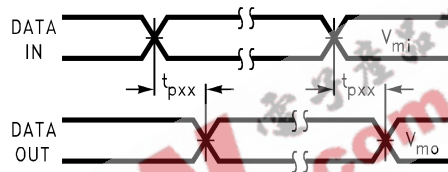| TEST	SWITCH
t$_{PLH}$, t$_{PHL}$	Open
t$_{PZL}$, t$_{PLZ}$	V$_{CC}$ x 2 at V$_{CC}$ = 1.5 $\pm$ 0.1V
t$_{PZH}$, t$_{PHZ}$	GND

FIGURE 5. AC Test Circuit

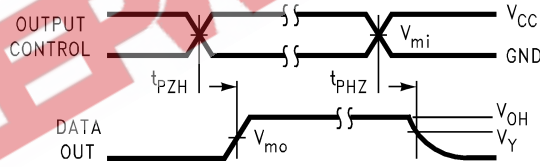**FIGURE 6. Waveform for Inverting and Non-Inverting Functions**

FIGURE 7. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

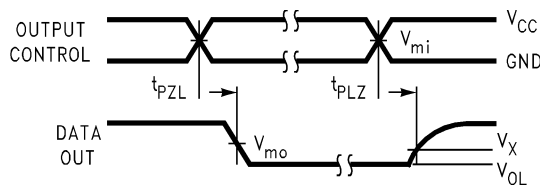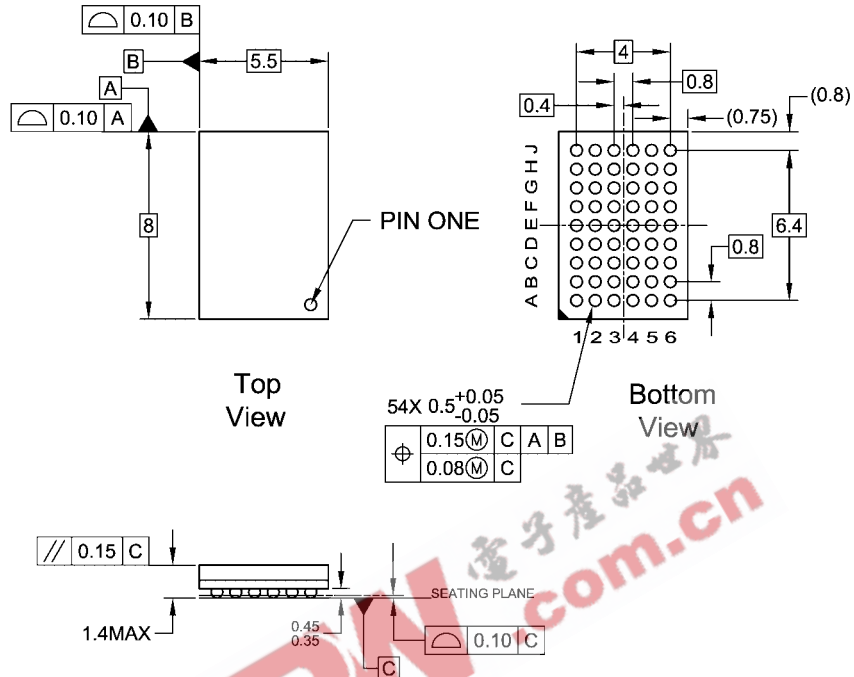**FIGURE 8. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic**

Symbol	V$_{CC}$
	1.5V $\pm$ 0.1V
V$_{mi}$	V$_{CC}$/2
V$_{mo}$	V$_{CC}$/2
V$_X$	V$_{OL}$ + 0.1V
V$_Y$	V$_{OH}$ − 0.1V

Physical Dimensions inches (millimeters) unless otherwise noted

⌓ 0.10 B

B ◄ 5.5

A

⌓ 0.10 A

8

PIN ONE

Top View

4

0.4   0.8   (0.8)

(0.75)

A B C D E F G H J

6.4

0.8

1 2 3 4 5 6

54X 0.5 +0.05 -0.05

⊕ 0.15Ⓜ C A B
0.08Ⓜ C

Bottom View

∥ 0.15 C

SEATING PLANE

1.4MAX

0.45
0.35

⌓ 0.10 C

C

NOTES:
A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
   .35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A
Preliminary

74VCXH16244 Low Voltage 16-Bit Buffer/Line Driver with Bushold *(vertical, left margin)*

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

12.50±0.10
-A-

0.40 TYP

48 43 30 25

8.10

4.05

6.10±0.10
-B-

PIN #1 IDENT.

1 6 19 24

⌒ 0.2 | C | B | A
ALL LEAD TIPS

48 43 30 25

4.60 9.20

2.30

1 6 19 24

0.30
0.50

LAND PATTERN RECOMMENDATION

⌒ 0.1 | C
ALL LEAD TIPS

1.2 MAX

-C-

0.50

0.17-0.27

⊕ | 0.13 Ⓜ | A | B Ⓢ | C Ⓢ

DIMENSIONS ARE IN MILLIMETERS

$0.90^{+0.15}_{-0.10}$

0.10±0.05

SEE DETAIL A

0.09-0.20

NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48RevB1

12.00° TOP & BOTTOM

R0.16
R0.31

GAGE PLANE

1.25

0°-8°

0.60±0.10
1.00

SEATING PLANE

DETAIL A

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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