

74FR2240

Octal Buffer/Line Driver with 25Ω Series Resistors in the Outputs

General Description

The 74FR2240 is an inverting octal buffer and line driver designed to drive capacitive inputs of MOS memory devices, address and clock lines or act as a low undershoot general purpose bus driver.

Features

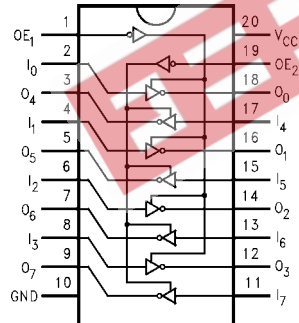
- 3-STATE outputs drive bus lines or buffer memory address registers
- Outputs sink 12 mA and source 15 mA
- 25Ω series resistors in outputs eliminate the need for external resistors
- Designed to drive the capacitive inputs of MOS devices

Ordering Code:

| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| 74FR2240SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide |
| 74FR2240PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

| Pin Names | Description |
|------------------------------------|----------------------------------|
| $\overline{OE}_1, \overline{OE}_2$ | Output Enable Input (Active-LOW) |
| I_0-I_7 | Inputs |
| $\overline{O}_0-\overline{O}_7$ | Outputs |

Truth Tables

| Inputs | | Outputs |
|-------------------|-------|-----------------------|
| \overline{OE}_1 | I_n | (Pins 12, 14, 16, 18) |
| L | L | H |
| L | H | L |
| H | X | Z |

| Inputs | | Outputs |
|-------------------|-------|-------------------|
| \overline{OE}_2 | I_n | (Pins 3, 5, 7, 9) |
| L | L | H |
| L | H | L |
| H | X | Z |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings (Note 1)

| | |
|--|--------------------------------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature under Bias | -55°C to +125°C |
| Junction Temperature under Bias | -55°C to +150°C |
| V _{CC} Pin Potential to Ground Pin | -0.5V to +7.0V |
| Input Voltage (Note 2) | -0.5V to +7.0V |
| Input Current (Note 2) | -30 mA to +5.0 mA |
| Voltage Applied to Output in HIGH State (with V _{CC} = 0V) | |
| Standard Output | -0.5V to V _{CC} |
| 3-STATE Output | -0.5V to +5.5V |
| Current Applied to Output in LOW State (Max) | Twice the Rated I _{OL} (mA) |
| ESD Last Passing Voltage (Min) | 4000V |

Recommended Operating Conditions

| | |
|------------------------------|----------------|
| Free Air Ambient Temperature | 0°C to +70°C |
| Supply Voltage | +4.5V to +5.5V |

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Units | V _{CC} | Conditions |
|------------------|--------------------------------------|------|-----|------|-------|-----------------|--|
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | | Recognized HIGH Signal |
| V _{IL} | Input LOW Voltage | | | 0.8 | V | | Recognized LOW Signal |
| V _{CD} | Input Clamp Diode Voltage | | | -1.2 | V | Min | I _{IN} = -18 mA |
| V _{OH} | Output HIGH Voltage | 2.4 | | | V | Min | I _{OH} = -3 mA |
| | | 2.0 | | | V | Min | I _{OH} = -15 mA |
| V _{OL} | Output LOW Voltage | | | 0.5 | V | Min | I _{OL} = 1 mA |
| | | | | 0.75 | V | Min | I _{OL} = 12 mA |
| I _{IH} | Input HIGH Current | | | 5 | μA | Max | V _{IN} = 2.7V |
| I _{BVI} | Input HIGH Current Breakdown Test | | | 7 | μA | Max | V _{IN} = 7.0V |
| I _{IL} | Input LOW Current | | | -150 | μA | Max | V _{IN} = 0.5V |
| V _{ID} | Input Leakage Test | 4.75 | | | V | 0.0 | I _{ID} = 1.9 μA All Other Pins Grounded |
| I _{OD} | Output Circuit Leakage Current | | | 3.75 | μA | 0.0 | V _{IOD} = 150 mV All Other Pins Grounded |
| I _{OZH} | Output Leakage Current | | | 20 | μA | Max | V _{OUT} = 2.7V |
| I _{OZL} | Output Leakage Current | | | -20 | μA | Max | V _{OUT} = 0.5V |
| I _{OS} | Output Short-Circuit Current | -100 | | -225 | mA | Max | V _{OUT} = 0.0V |
| I _{CEX} | Output HIGH Leakage Current | | | 50 | μA | Max | V _{OUT} = V _{CC} |
| I _{ZZ} | Bus Drainage Test | | | 100 | μA | 0.0 | V _{OUT} = 5.25V |
| I _{CCH} | Power Supply Current | | 9 | 13 | mA | Max | All Outputs HIGH |
| I _{CCL} | Power Supply Current | | 37 | 45 | mA | Max | All Outputs LOW |
| I _{CCZ} | Power Supply Current | | 30 | 38 | mA | Max | Outputs 3-STATE |

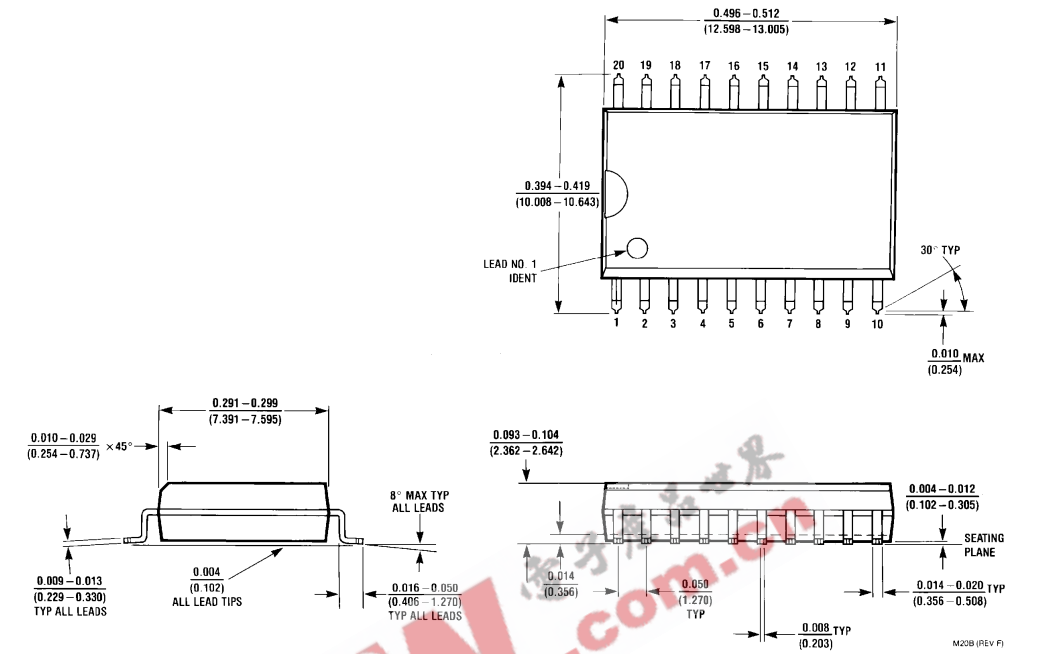
| AC Electrical Characteristics | | | | | | | |
|--|--|---|-----|---|--|-------|-------|
| Symbol | Parameter | T _A = +25°C V _{CC} = +5.0V C _L = 50 pF | | | T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF | | Units |
| | | Min | Typ | Max | Min | Max | |
| t _{PLH} | Propagation Delay | 1.7 | 3.3 | 4.7 | 1.7 | 4.7 | ns |
| t _{PHL} | A _n to B _n or B _n to A _n | 1.7 | 2.9 | 4.7 | 1.7 | 4.7 | |
| t _{PZH} | Output Enable Time | 2.6 | 4.0 | 8.5 | 2.6 | 8.5 | ns |
| t _{PZL} | | 2.6 | 6.3 | 8.5 | 2.6 | 8.5 | |
| t _{PHZ} | Output Disable Time | 2.1 | 3.9 | 6.6 | 2.1 | 6.6 | ns |
| t _{PLZ} | | 2.1 | 3.4 | 6.6 | 2.1 | 6.6 | |
| Extended AC Electrical Characteristics | | | | | | | |
| Symbol | Parameter | T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF Eight Outputs Switching (Note 3) | | T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 250 pF (Note 4) | | Units | |
| | | Min | Max | Min | Max | | |
| t _{PLH} | Propagation Delay | 1.7 | 6.4 | 4.2 | 8.6 | ns | |
| t _{PHL} | A _n to B _n or B _n to A _n | 1.7 | 6.4 | 4.2 | 8.6 | | |
| t _{PZH} | Output Enable Time | 2.6 | 8.9 | | | ns | |
| t _{PZL} | | 2.6 | 8.9 | | | | |
| t _{PHZ} | Output Disable Time | 2.1 | 6.8 | | | ns | |
| t _{PLZ} | | 2.1 | 6.8 | | | | |
| t _{OSSL} (Note 5) | Pin-to-Pin Skew for HL Transitions | | 1.0 | | | ns | |
| t _{OSLH} (Note 5) | Pin-to-Pin Skew for LH Transitions | | 1.1 | | | ns | |
| t _{OST} (Note 5) | Pin-to-Pin Skew for HL/LH Transitions | | 3.0 | | | ns | |

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase, i.e., all LOW-to-HIGH, HIGH-to-LOW, 3-STATE-to-HIGH, etc.

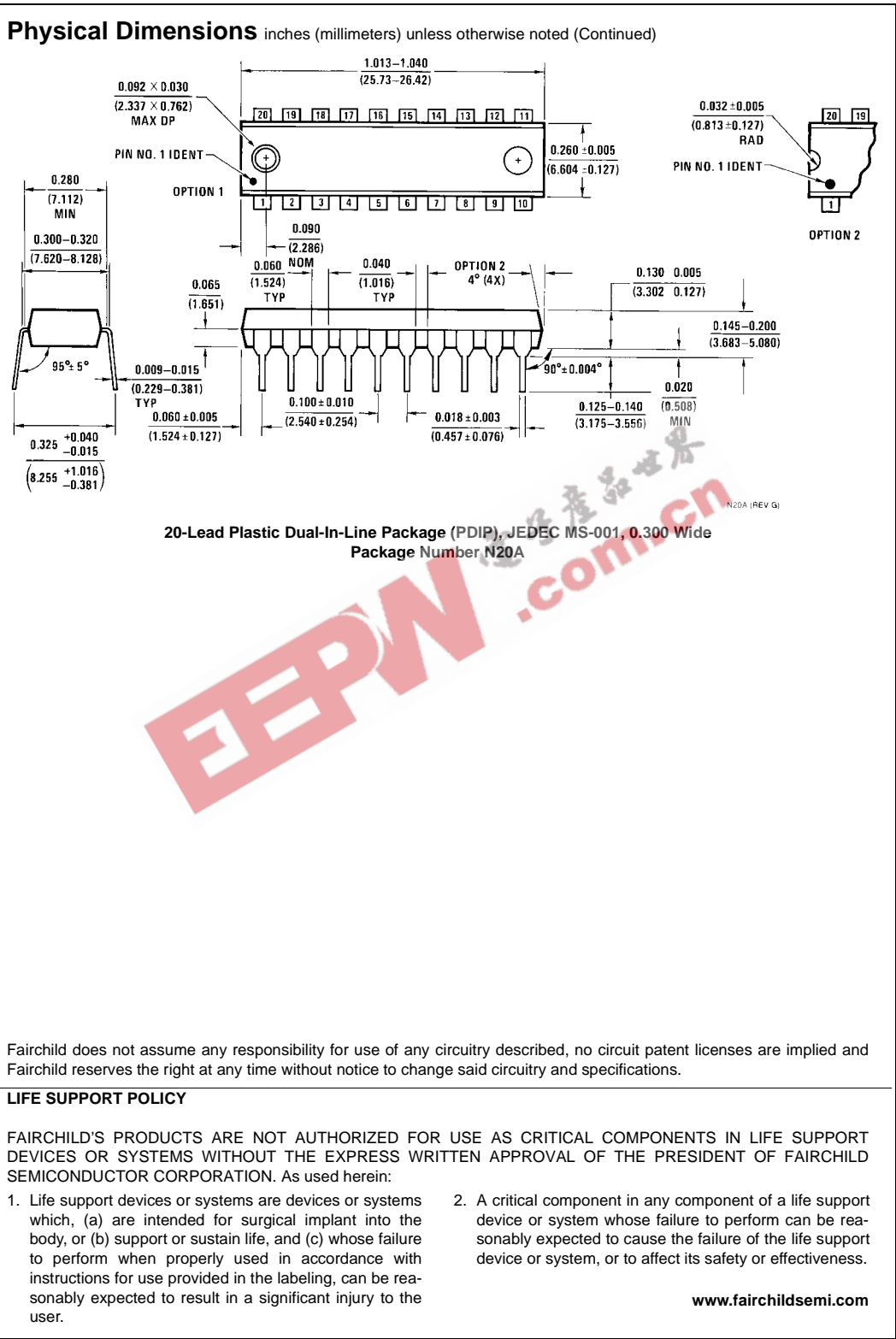
Note 4: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 5: Skew is defined as the absolute value of the difference between the actual propagation delays for any two outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW, (t_{OSSL}), LOW-to-HIGH, (t_{OSLH}), or HIGH-to-LOW and/or LOW-to-HIGH, (t_{OST}). Specifications guaranteed with all outputs switching in phase.

Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B**



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