

# DATA SHEET

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**74F841/842/843/845/846**

**Bus interface latches**

Product specification

Replaces datasheet 74F841/842/843/844/845/846 of 1999 Jan 08

IC15 Data Handbook

1999 Jun 23

## Bus interface latches

## 74F841/74F842/74F843/ 74F845/74F846

74F841/74F842 10-bit bus interface latches, non-inverting/inverting (3-State)

74F843 9-bit bus interface latch, non-inverting (3-State)

74F845/74F846 8-bit bus interface latches, non-inverting/inverting (3-State)

### FEATURES

- High speed parallel latches
- Extra data width for wide address/data paths or buses carrying parity
- High impedance NPN base input structure minimizes bus loading
- IIL is 20 $\mu$ A vs 1000A for AM29841 series
- Buffered control inputs to reduce AC effects
- Ideal where high speed, light loading, or increased fan-in are required as with MOS microprocessors
- Positive and negative over-shoots are clamped to ground
- 3-State outputs glitch free during power-up and power-down
- 48mA sink current
- Slim dual in-line 300 mil package
- Broadside pinout
- Pin-for-pin and function compatible with AMD AM29841-846 series

| TYPE           | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|----------------|---------------------------|--------------------------------|
| 74F841, 74F842 | 5.5ns                     | 60mA                           |
| 74F843, 74F845 | 5.5ns                     | 75mA                           |
| 74F846         | 6.2ns                     | 60mA                           |

### DESCRIPTION

The 74F841–74F846 bus interface latch series are designed to provide extra data width for wider address/data paths of buses carrying parity.

The 74F841–74F846 series are functionally a pin compatible to the AMD AM29841–AM29846 series.

The 74F841 consists of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the LE High-to-Low transition, the data that meets the setup and hold time is latched.

Data appears on the bus when the Output Enable ( $\overline{OE}$ ) is Low. When  $\overline{OE}$  is High the output is in the High-impedance state.

The 74F842 is the inverted output version of the 74F841.

The 74F843 consists of nine D-type latches with 3-State outputs. In addition to the LE and  $\overline{OE}$  pins, the 74F843 has a Master Reset ( $\overline{MR}$ ) pin and Preset ( $\overline{PRE}$ ) pin. These pins are ideal for parity bus interfacing in high performance systems. When  $\overline{MR}$  is Low, the outputs are Low if  $\overline{OE}$  is Low. When  $\overline{MR}$  is High, data can be entered into the latch. When  $\overline{PRE}$  is Low, the outputs are High, if  $\overline{OE}$  is Low,  $\overline{PRE}$  overrides  $\overline{MR}$ .

The 74F845 consists of eight D-type latches with 3-State outputs. In addition to the LE,  $\overline{OE}$ ,  $\overline{MR}$  and  $\overline{PRE}$  pins, the 74F845 has two additional  $\overline{OE}$  pins making a total of three Output Enables ( $\overline{OE}0$ ,  $\overline{OE}1$ ,  $\overline{OE}2$ ) pins.

The multiple Output Enables ( $\overline{OE}0$ ,  $\overline{OE}1$ ,  $\overline{OE}2$ ) allow multi-user control of the interface, e.g., CS, DMA, and RD/ $\overline{WR}$ .

The 74F846 is the inverted output version of the 74F845.

### ORDERING INFORMATION

| PACKAGES                          | COMMERCIAL RANGE<br>$V_{CC} = 5V \pm 10\%$ ; $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$ | PACKAGE DRAWING NUMBER |
|-----------------------------------|---|------------------------|
| 24-pin plastic Slim DIP (300 mil) | N74F841N, N74F842N, N74F843N, N74F845N, N74F846N                                      | SOT222-1               |
| 24-pin plastic SOL                | N74F841D, N74F842D, N74F843D, N74F845D, N74F846D                                      | SOT137-1               |

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

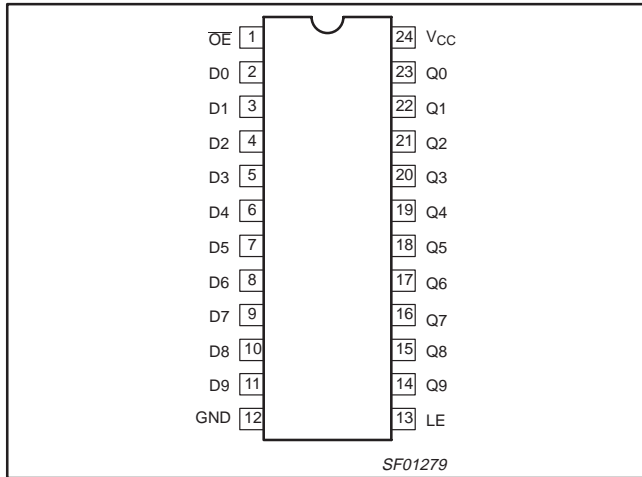
| PINS                               | DESCRIPTION                      | 74F(U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW   |
|------------------------------------|----------------------------------|--------------------|-----------------------|
| Dn                                 | Data inputs                      | 1.0/0.033          | 20 $\mu$ A/20 $\mu$ A |
| LE                                 | Latch Enable input               | 1.0/0.033          | 20 $\mu$ A/20 $\mu$ A |
| $\overline{OE}$ , $\overline{OE}n$ | Output Enable input (active Low) | 1.0/0.033          | 20 $\mu$ A/20 $\mu$ A |
| $\overline{MR}$                    | Master Reset input (active Low)  | 1.0/0.033          | 20 $\mu$ A/20 $\mu$ A |
| $\overline{PRE}$                   | Preset input (active Low)        | 1.0/0.033          | 20 $\mu$ A/20 $\mu$ A |
| Qn                                 | Data outputs                     | 1200/80            | 24mA/48mA             |
| $\overline{Q}n$                    | Data outputs                     | 1200/80            | 24mA/48mA             |

NOTE: One (1.0) FAST Unit Load is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

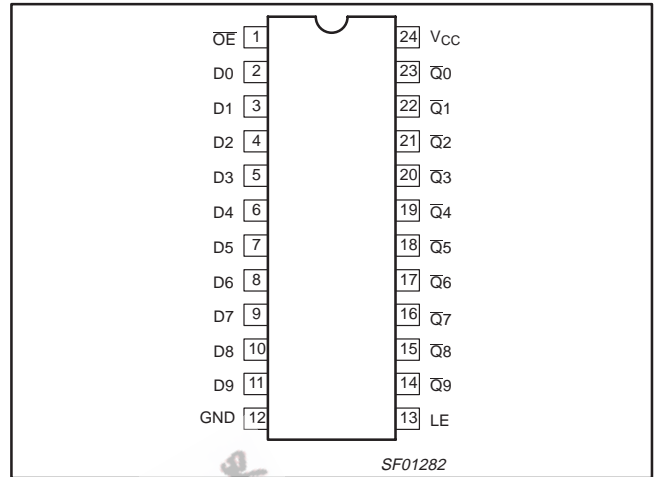
Bus interface latches

74F841/74F842/74F843/  
74F845/74F846

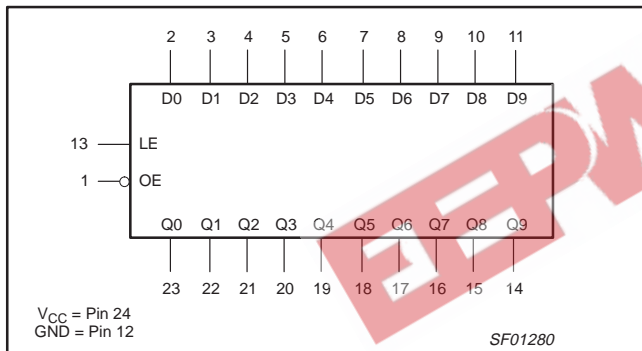
PIN CONFIGURATION for 74F841



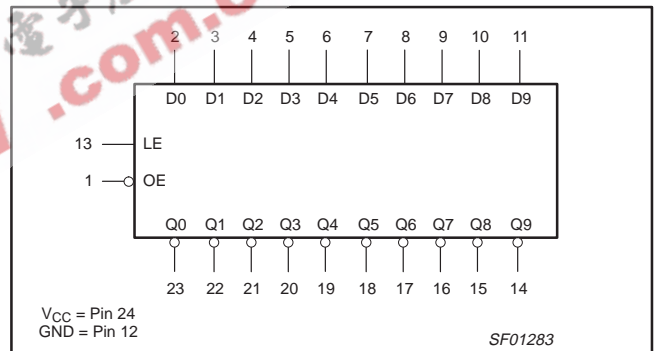
PIN CONFIGURATION for 74F842



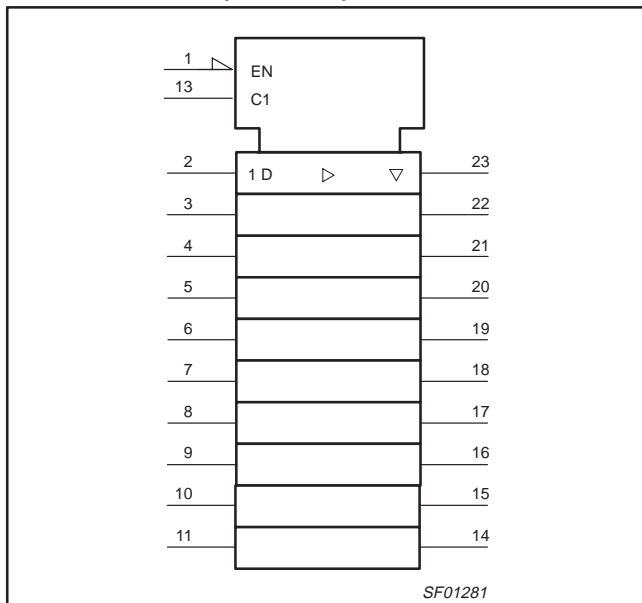
LOGIC SYMBOL for 74F841



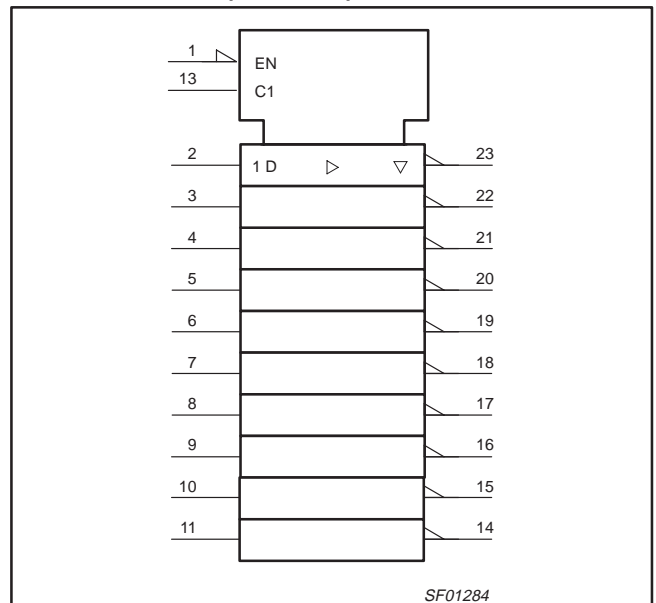
LOGIC SYMBOL for 74F842



LOGIC SYMBOL (IEEE/IEC) for 74F841



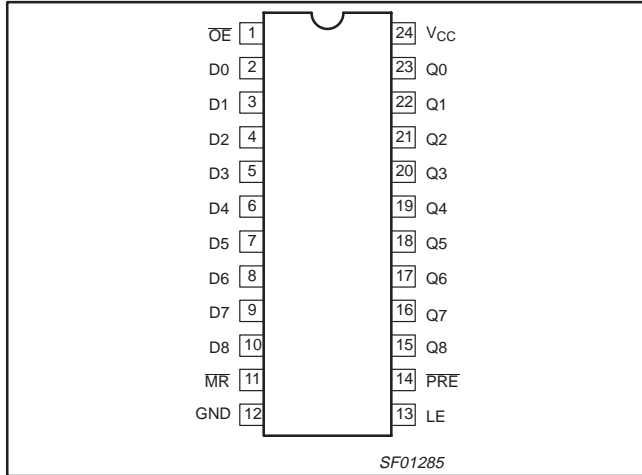
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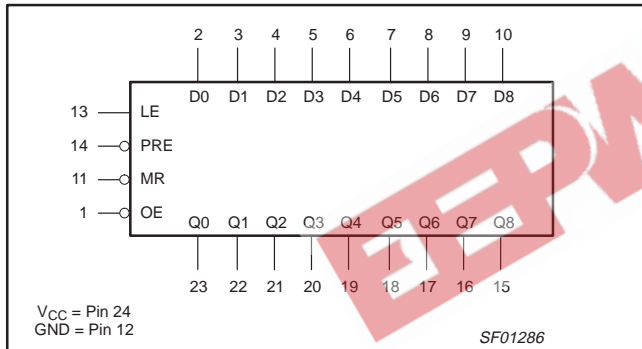
Bus interface latches

74F841/74F842/74F843/  
74F845/74F846

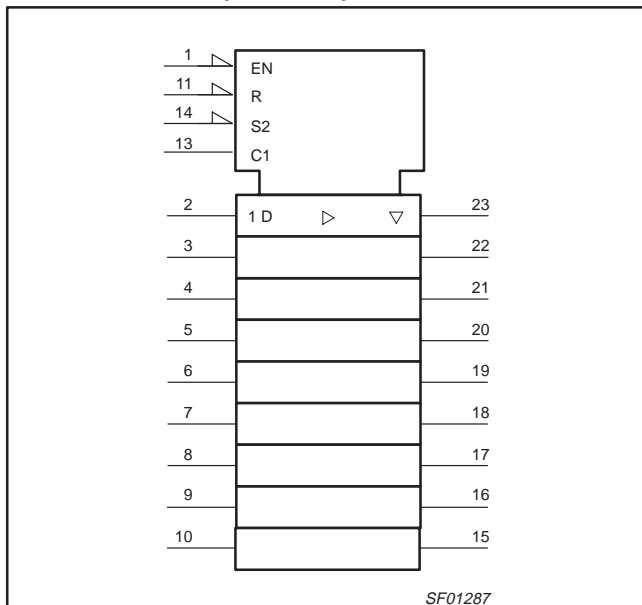
**PIN CONFIGURATION for 74F843**



**LOGIC SYMBOL for 74F843**



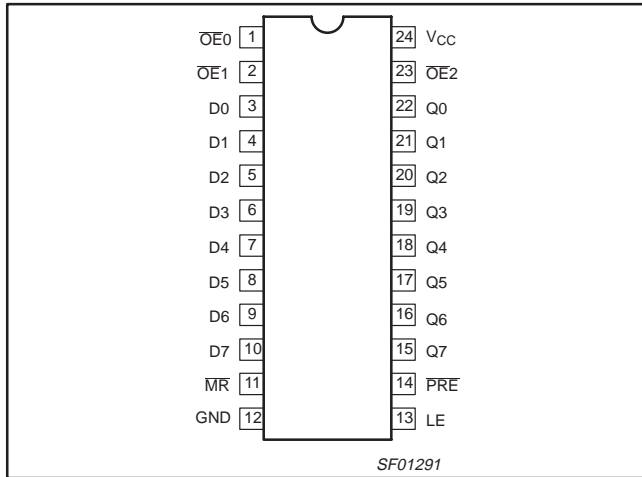
**LOGIC SYMBOL (IEEE/IEC) for 74F843**



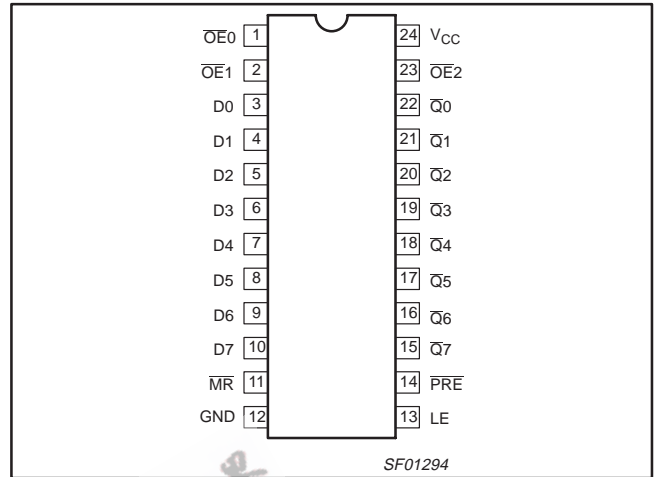
Bus interface latches

74F841/74F842/74F843/  
74F845/74F846

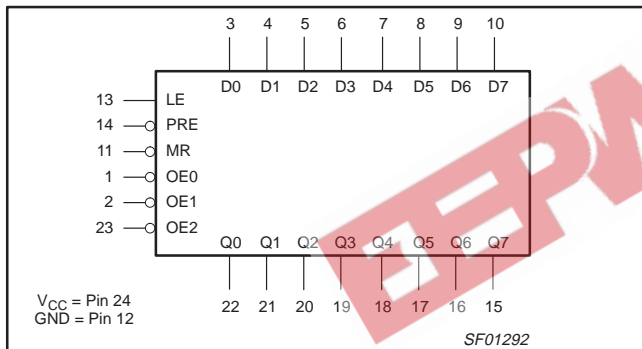
PIN CONFIGURATION for 74F845



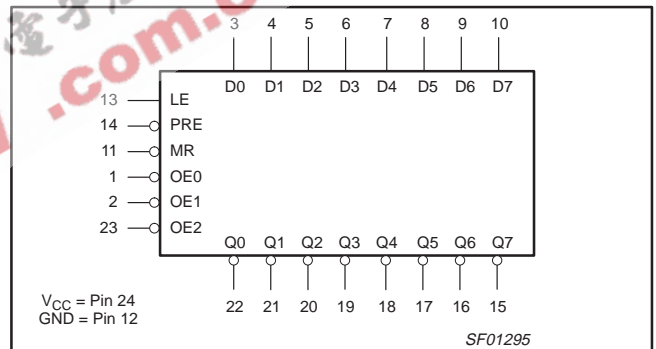
PIN CONFIGURATION for 74F846



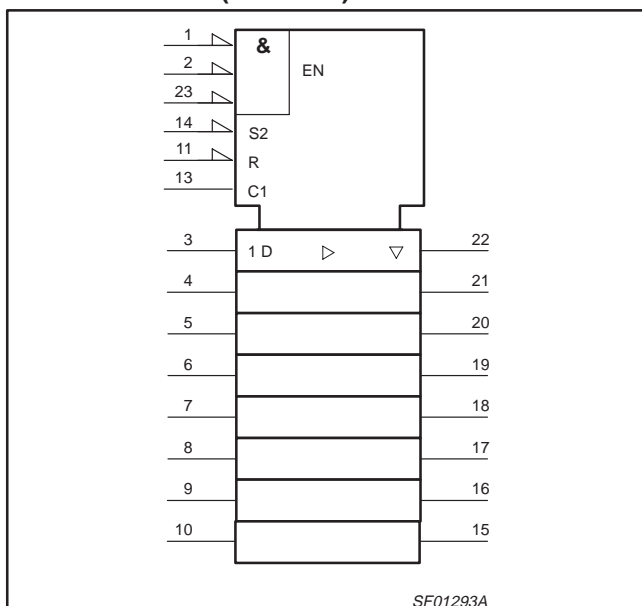
LOGIC SYMBOL for 74F845



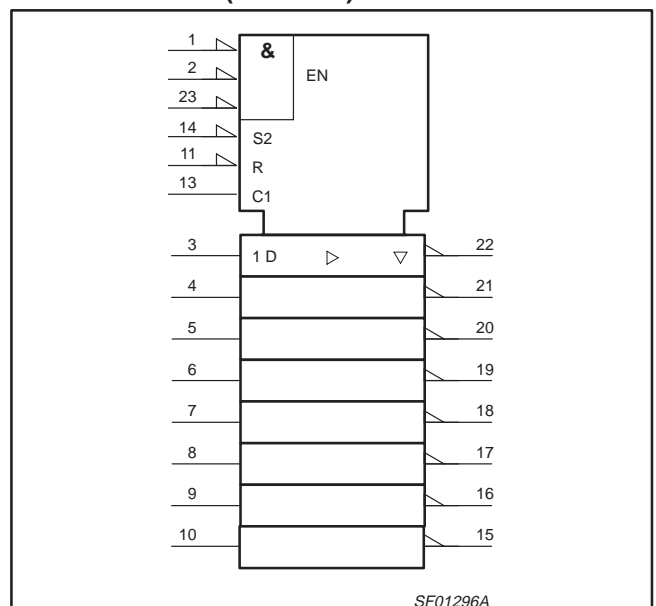
LOGIC SYMBOL for 74F846



LOGIC SYMBOL (IEEE/IEC) for 74F845



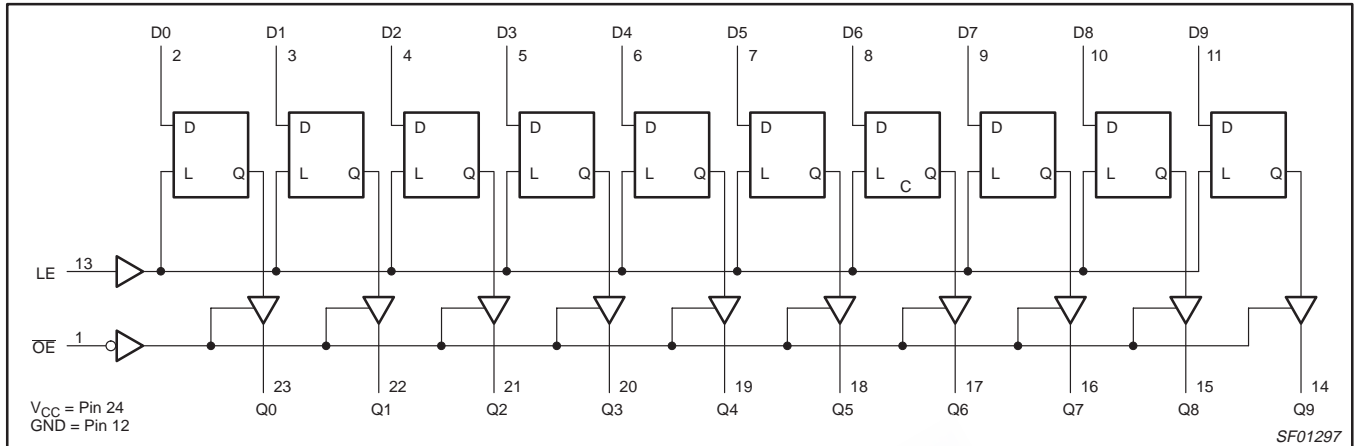
LOGIC SYMBOL (IEEE/IEC) for 74F846



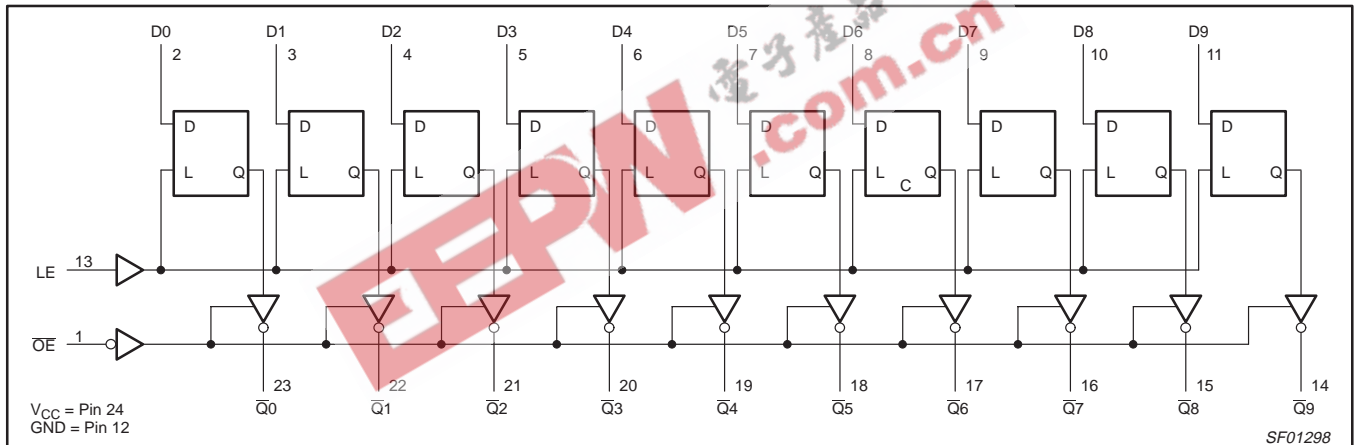
Bus interface latches

74F841/74F842/74F843/  
74F845/74F846

LOGIC DIAGRAM for 74F841



LOGIC DIAGRAM for 74F842



FUNCTION TABLE for 74F841 and 74F842

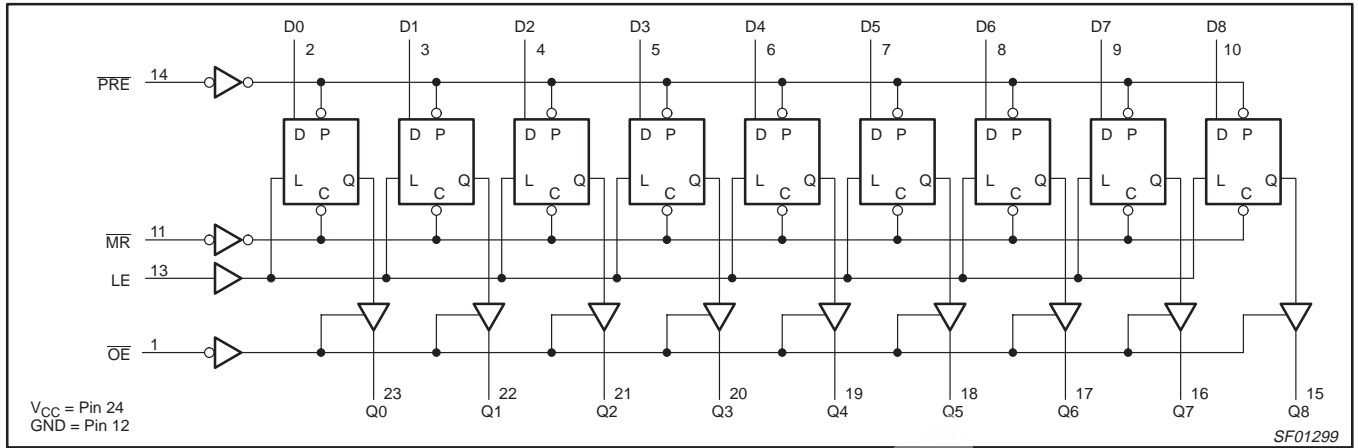
| INPUTS          |    |                | OUTPUTS        |                  | OPERATING MODE |
|-----------------|----|----------------|----------------|------------------|----------------|
| $\overline{OE}$ | LE | D <sub>n</sub> | Q <sub>n</sub> | $\overline{Q}_n$ |                |
| L               | H  | L              | L              | H                | Transparent    |
| L               | H  | H              | H              | L                |                |
| L               | ↓  | l              | L              | H                | Latched        |
| L               | ↓  | h              | H              | L                |                |
| H               | X  | X              | Z              | Z                | High Impedance |
| L               | L  | X              | NC             | NC               | Hold           |

- H = High voltage level
- L = Low voltage level
- h = High state one setup time before the High-to-Low LE transition
- l = Low state one setup time before the High-to-Low LE transition
- ↓ = High-to-Low transition
- X = Don't care
- NC = No change
- Z = High impedance "off" state

Bus interface latches

74F841/74F842/74F843/  
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LOGIC DIAGRAM for 74F843



FUNCTION TABLE for 74F843

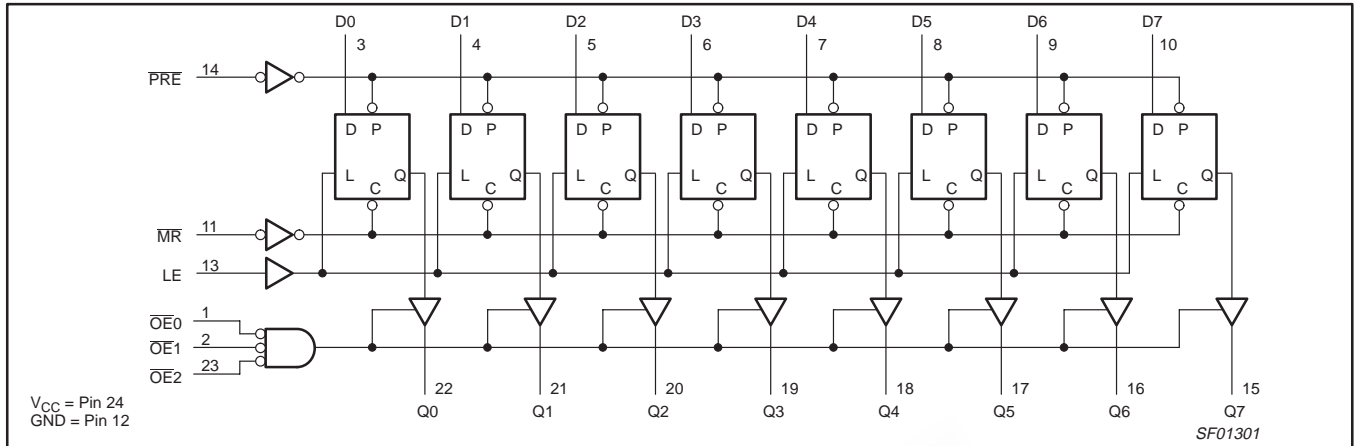
| INPUTS |     |    |    |                | OUTPUTS        | OPERATING MODE |
|--------|-----|----|----|----------------|----------------|----------------|
| OE     | PRE | MR | LE | D <sub>n</sub> | Q <sub>n</sub> |                |
| L      | L   | X  | X  | X              | H              | Preset         |
| L      | H   | L  | X  | X              | L              | Clear          |
| L      | H   | H  | H  | L              | L              | Transparent    |
| L      | H   | H  | H  | H              | H              |                |
| L      | H   | H  | ↓  | l              | L              | Latched        |
| L      | H   | H  | ↓  | h              | H              |                |
| H      | X   | X  | X  | X              | Z              | High Impedance |
| L      | H   | H  | L  | X              | NC             | Hold           |

- H = High voltage level
- L = Low voltage level
- h = High state one setup time before the High-to-Low LE transition
- l = Low state one setup time before the High-to-Low LE transition
- ↓ = High-to-Low transition
- X = Don't care
- NC= No change
- Z = High impedance "off" state

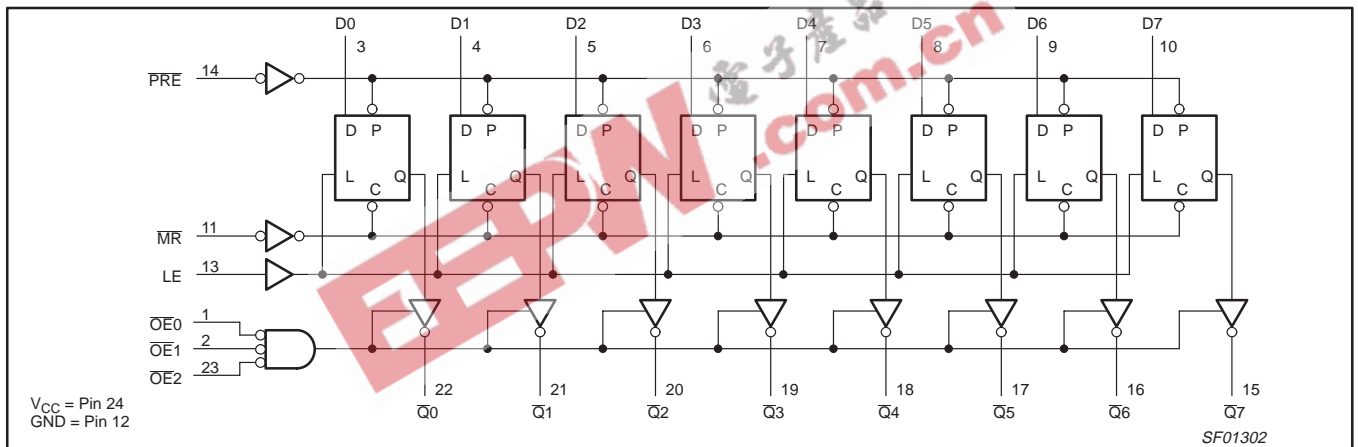
Bus interface latches

74F841/74F842/74F843/  
74F845/74F846

LOGIC DIAGRAM for 74F845



LOGIC DIAGRAM for 74F846



FUNCTION TABLE for 74F845 and 74F846

| INPUTS |     |    |    |    | OUTPUTS |        | OPERATING MODE |
|--------|-----|----|----|----|---------|--------|----------------|
|        |     |    |    |    | 74F845  | 74F846 |                |
| OE     | PRE | MR | LE | Dn | Qn      | Q̄n    |                |
| L      | L   | X  | X  | X  | H       | H      | Preset         |
| L      | H   | L  | X  | X  | L       | L      | Clear          |
| L      | H   | H  | H  | L  | L       | H      | Transparent    |
| L      | H   | H  | H  | H  | H       | L      |                |
| L      | H   | H  | ↓  | l  | L       | H      | Latched        |
| L      | H   | H  | ↓  | h  | H       | L      |                |
| H      | X   | X  | X  | X  | Z       | Z      | High Impedance |
| L      | H   | H  | L  | X  | NC      | NC     | Hold           |

H = High voltage level  
 L = Low voltage level  
 h = High state one setup time before the High-to-Low LE transition  
 l = Low state one setup time before the High-to-Low LE transition  
 ↓ = High-to-Low transition  
 X = Don't care  
 NC = No change  
 Z = High impedance "off" state



## Bus interface latches

74F841/74F842/74F843/  
74F845/74F846**ABSOLUTE MAXIMUM RATINGS**

Operation beyond the limits set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.

| SYMBOL           | PARAMETER                                      | RATING                  | UNIT |
|------------------|--|-------------------------|------|
| V <sub>CC</sub>  | Supply voltage                                 | -0.5 to +7.0            | V    |
| V <sub>IN</sub>  | Input voltage                                  | -0.5 to +7.0            | V    |
| I <sub>IN</sub>  | Input current                                  | -30 to +5               | mA   |
| V <sub>OUT</sub> | Voltage applied to output in High output state | -0.5 to V <sub>CC</sub> | V    |
| I <sub>OUT</sub> | Current applied to output in Low output state  | 84                      | mA   |
| T <sub>amb</sub> | Operating free-air temperature range           | 0 to +70                | °C   |
| T <sub>stg</sub> | Storage temperature range                      | -65 to +150             | °C   |

**RECOMMENDED OPERATING CONDITIONS**

| SYMBOL           | PARAMETER                            | LIMITS |     |     | UNIT |
|------------------|--------------------------------------|--------|-----|-----|------|
|                  |                                      | MIN    | NOM | MAX |      |
| V <sub>CC</sub>  | Supply voltage                       | 4.5    | 5.0 | 5.5 | V    |
| V <sub>IH</sub>  | High-level input voltage             | 2.0    |     |     | V    |
| V <sub>IL</sub>  | Low-level input voltage              |        |     | 0.8 | V    |
| I <sub>IK</sub>  | Input clamp current                  |        |     | -18 | mA   |
| I <sub>OH</sub>  | High-level output current            |        |     | -24 | mA   |
| I <sub>OL</sub>  | Low-level output current             |        |     | 48  | mA   |
| T <sub>amb</sub> | Operating free-air temperature range | 0      |     | +70 | °C   |

## Bus interface latches

74F841/74F842/74F843/  
74F845/74F846

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

| SYMBOL           | PARAMETER   | TEST CONDITIONS <sup>1</sup>   |                         | LIMITS                |                  |      | UNIT |    |
|------------------|---|--|-------------------------|-----------------------|------------------|------|------|----|
|                  |   |  |                         | MIN                   | TYP <sup>2</sup> | MAX  |      |    |
| V <sub>OH</sub>  | High-level output voltage                               | V <sub>CC</sub> = MIN,<br>V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN | I <sub>OH</sub> = -15mA | ±10%V <sub>CC</sub>   | 2.2              |      | V    |    |
|                  |   |  |                         | ±5%V <sub>CC</sub>    | 2.2              | 3.3  | V    |    |
|                  |   |  | I <sub>OH</sub> = -24mA | ±10%V <sub>CC</sub>   | 2.0              |      | V    |    |
|                  |   |  |                         | ±5%V <sub>CC</sub>    | 2.0              |      | V    |    |
| V <sub>OL</sub>  | Low-level output voltage                                | V <sub>CC</sub> = MIN,<br>V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN | I <sub>OL</sub> = 32mA  | ±10%V <sub>CC</sub>   |                  | 0.38 | 0.55 | V  |
|                  |   |  | I <sub>OL</sub> = 48mA  | ±5%V <sub>CC</sub>    |                  | 0.38 | 0.55 | V  |
| V <sub>IK</sub>  | Input clamp voltage                                     | V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>                |                         |                       | -0.73            | -1.2 | V    |    |
| I <sub>I</sub>   | Input current at maximum input voltage                  | V <sub>CC</sub> = 0.0V, V <sub>I</sub> = 7.0V                          |                         |                       |                  | 100  | μA   |    |
| I <sub>IH</sub>  | High-level input current                                | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V                           |                         |                       |                  | 20   | μA   |    |
| I <sub>IL</sub>  | Low-level input current                                 | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V                           |                         |                       |                  | -20  | μA   |    |
| I <sub>OZH</sub> | Off-state output current,<br>High-level voltage applied | V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7V                           |                         |                       |                  | 50   | μA   |    |
| I <sub>OZL</sub> | Off-state output current,<br>Low-level voltage applied  | V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.5V                           |                         |                       |                  | -50  | μA   |    |
| I <sub>OS</sub>  | Short-circuit output current <sup>3</sup>               | V <sub>CC</sub> = MAX  |                         | -100                  |                  | -225 | mA   |    |
| I <sub>CC</sub>  | Supply current<br>(total)                               | 74F841   | I <sub>CCH</sub>        | V <sub>CC</sub> = MAX |                  | 50   | 65   | mA |
|                  |   |  | I <sub>CCL</sub>        |                       |                  | 60   | 80   | mA |
|                  |   |  | I <sub>CCZ</sub>        |                       |                  | 70   | 92   | mA |
|                  |   | 74F842   | I <sub>CCH</sub>        | V <sub>CC</sub> = MAX |                  | 40   | 60   | mA |
|                  |   |  | I <sub>CCL</sub>        |                       |                  | 65   | 90   | mA |
|                  |   |  | I <sub>CCZ</sub>        |                       |                  | 60   | 90   | mA |
|                  |   | 74F843<br>74F845   | I <sub>CCH</sub>        | V <sub>CC</sub> = MAX |                  | 65   | 90   | mA |
|                  |   |  | I <sub>CCL</sub>        |                       |                  | 75   | 100  | mA |
|                  |   |  | I <sub>CCZ</sub>        |                       |                  | 85   | 115  | mA |
|                  |   | 74F846   | I <sub>CCH</sub>        | V <sub>CC</sub> = MAX |                  | 50   | 70   | mA |
|                  |   |  | I <sub>CCL</sub>        |                       |                  | 70   | 95   | mA |
|                  |   |  | I <sub>CCZ</sub>        |                       |                  | 70   | 95   | mA |

## NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I<sub>OS</sub> tests should be performed last.

## Bus interface latches

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74F845/74F846

## AC ELECTRICAL CHARACTERISTICS for 74F841/74F842

| SYMBOL                               | PARAMETER  |        | TEST<br>CONDITION        | LIMITS  |            |             |  |             | UNIT |
|--------------------------------------|--|--------|--------------------------|---|------------|-------------|--|-------------|------|
|                                      |  |        |                          | T <sub>amb</sub> = +25°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |            |             | T <sub>amb</sub> = 0°C to +70°C<br>V <sub>CC</sub> = +5.0V ± 10%<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |             |      |
|                                      |  |        |                          | MIN   | TYP        | MAX         | MIN  | MAX         |      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>Dn to Qn                            | 74F841 | Waveform 1, 2            | 2.0<br>2.5  | 4.0<br>4.5 | 7.5<br>7.5  | 2.0<br>2.5   | 8.0<br>8.0  | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>LE to Qn                            |        | Waveform 1, 2            | 4.5<br>4.0  | 6.5<br>6.0 | 9.5<br>9.0  | 4.0<br>3.5   | 10.0<br>9.5 | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>Dn to Qn                            | 74F842 | Waveform 1, 2            | 3.5<br>3.0  | 5.5<br>5.0 | 8.5<br>8.0  | 4.5<br>4.0   | 9.0<br>8.5  | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>LE to Qn                            |        | Waveform 1, 2            | 5.0<br>4.5  | 7.0<br>6.5 | 10.0<br>9.0 | 3.0<br>3.0   | 10.5<br>9.5 | ns   |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output enable time<br>High or Low-level OEn to Qn or Qn  |        | Waveform 5<br>Waveform 6 | 2.5<br>4.0  | 4.5<br>6.0 | 8.0<br>9.5  | 2.0<br>3.0   | 8.5<br>10.5 | ns   |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Output disable time<br>High or Low-level OEn to Qn or Qn |        | Waveform 5<br>Waveform 6 | 1.0<br>1.0  | 4.5<br>5.0 | 8.0<br>8.0  | 1.0<br>1.0   | 8.5<br>8.5  | ns   |

## AC SETUP REQUIREMENTS for 74F841/74F842

| SYMBOL                                   | PARAMETER                           |        | TEST<br>CONDITION | LIMITS  |     |  |     | UNIT |
|--|-------------------------------------|--------|-------------------|---|-----|--|-----|------|
|  |                                     |        |                   | T <sub>amb</sub> = +25°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |     | T <sub>amb</sub> = 0°C to +70°C<br>V <sub>CC</sub> = +5.0V ± 10%<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |     |      |
|  |                                     |        |                   | MIN   | TYP | MIN  | MAX |      |
| t <sub>s</sub> (H)<br>t <sub>s</sub> (L) | Setup time, High or Low<br>Dn to LE |        | Waveform 4        | 0.0<br>0.0  |     | 1.0<br>1.0   |     | ns   |
| t <sub>h</sub> (H)<br>t <sub>h</sub> (L) | Hold time, High or Low<br>Dn to LE  | 74F841 | Waveform 4        | 2.5<br>3.0  |     | 3.0<br>4.0   |     | ns   |
| t <sub>w</sub> (H)                       | LE pulse width, High                |        | Waveform 4        | 3.5   |     | 4.0  |     | ns   |
| t <sub>h</sub> (H)<br>t <sub>h</sub> (L) | Hold time, High or Low<br>Dn to LE  | 74F842 | Waveform 4        | 3.0<br>3.5  |     | 3.5<br>4.5   |     | ns   |
| t <sub>w</sub> (H)                       | LE pulse width, High                |        | Waveform 4        | 3.0   |     | 3.0  |     | ns   |

## Bus interface latches

74F841/74F842/74F843/  
74F845/74F846

## AC ELECTRICAL CHARACTERISTICS for 74F843/74F845

| SYMBOL                               | PARAMETER  | TEST CONDITION           | LIMITS  |            |            |  |             | UNIT |
|--------------------------------------|--|--------------------------|---|------------|------------|--|-------------|------|
|                                      |  |                          | T <sub>amb</sub> = +25°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |            |            | T <sub>amb</sub> = 0°C to +70°C<br>V <sub>CC</sub> = +5.0V ± 10%<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |             |      |
|                                      |  |                          | MIN   | TYP        | MAX        | MIN  | MAX         |      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>Dn to Qn                      | Waveform 1, 2            | 2.0<br>2.5  | 4.5<br>4.5 | 7.5<br>8.0 | 2.0<br>2.5   | 8.5<br>8.5  | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>LE to Qn                      | Waveform 1, 2            | 4.5<br>4.0  | 6.5<br>6.0 | 9.5<br>8.5 | 4.5<br>4.0   | 10.0<br>8.5 | ns   |
| t <sub>PLH</sub>                     | Propagation delay<br>PRE to Qn                     | Waveform 3               | 3.5   | 5.5        | 8.5        | 3.0  | 9.0         | ns   |
| t <sub>PHL</sub>                     | Propagation delay<br>MR to Qn                      | Waveform 3               | 2.0   | 4.5        | 7.5        | 2.0  | 8.0         | ns   |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output enable time<br>High or Low-level OEn to Qn  | Waveform 5<br>Waveform 6 | 2.5<br>4.0  | 4.5<br>6.0 | 7.5<br>9.5 | 2.0<br>3.0   | 8.0<br>10.5 | ns   |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Output disable time<br>High or Low-level OEn to Qn | Waveform 5<br>Waveform 6 | 1.0<br>1.0  | 4.5<br>5.0 | 8.0<br>8.0 | 1.0<br>1.0   | 8.5<br>8.5  | ns   |

## AC SETUP REQUIREMENTS for 74F843/74F845

| SYMBOL                                   | PARAMETER                           | TEST CONDITION | LIMITS  |     |  |     | UNIT |
|--|-------------------------------------|----------------|---|-----|--|-----|------|
|  |                                     |                | T <sub>amb</sub> = +25°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |     | T <sub>amb</sub> = 0°C to +70°C<br>V <sub>CC</sub> = +5.0V ± 10%<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |     |      |
|  |                                     |                | MIN   | TYP | MIN  | MAX |      |
| t <sub>s</sub> (H)<br>t <sub>s</sub> (L) | Setup time, High or Low<br>Dn to LE | Waveform 4     | 1.0<br>1.0  |     | 0.0<br>0.0   |     | ns   |
| t <sub>h</sub> (H)<br>t <sub>h</sub> (L) | Hold time, High or Low<br>Dn to LE  | Waveform 4     | 3.0<br>4.0  |     | 3.0<br>4.0   |     | ns   |
| t <sub>w</sub> (H)                       | LE pulse width, High                | Waveform 4     | 3.0   |     | 3.0  |     | ns   |
| t <sub>w</sub> (L)                       | PRE pulse width, Low                | Waveform 3     | 4.0   |     | 5.0  |     | ns   |
| t <sub>w</sub> (H)                       | MR pulse width, Low                 | Waveform 3     | 4.0   |     | 5.0  |     | ns   |
| t <sub>REC</sub>                         | PRE recovery time                   | Waveform 3     | 0.0   |     | 0.0  |     | ns   |
| t <sub>REC</sub>                         | MR recovery time                    | Waveform 3     | 3.5   |     | 4.5  |     | ns   |

## Bus interface latches

74F841/74F842/74F843/  
74F845/74F846

## AC ELECTRICAL CHARACTERISTICS for 74F846

| SYMBOL                               | PARAMETER  | TEST CONDITION           | LIMITS  |            |             |  |             | UNIT |
|--------------------------------------|--|--------------------------|---|------------|-------------|--|-------------|------|
|                                      |  |                          | T <sub>amb</sub> = +25°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |            |             | T <sub>amb</sub> = 0°C to +70°C<br>V <sub>CC</sub> = +5.0V ± 10%<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |             |      |
|                                      |  |                          | MIN   | TYP        | MAX         | MIN  | MAX         |      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>Dn to Qn                      | Waveform 1, 2            | 3.5<br>3.0  | 5.5<br>5.0 | 8.5<br>8.0  | 3.0<br>3.0   | 9.5<br>8.5  | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>LE to Qn                      | Waveform 1, 2            | 5.0<br>4.5  | 7.0<br>6.5 | 10.0<br>9.0 | 5.0<br>4.5   | 10.5<br>9.5 | ns   |
| t <sub>PLH</sub>                     | Propagation delay<br>PRE to Qn                     | Waveform 3               | 3.5   | 5.5        | 8.5         | 3.0  | 9.5         | ns   |
| t <sub>PHL</sub>                     | Propagation delay<br>MR to Qn                      | Waveform 3               | 5.0   | 7.0        | 10.0        | 4.5  | 10.5        | ns   |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output enable time<br>High or Low-level OEn to Qn  | Waveform 5<br>Waveform 6 | 2.5<br>4.0  | 5.0<br>6.0 | 7.5<br>9.5  | 2.0<br>3.0   | 8.0<br>10.5 | ns   |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Output disable time<br>High or Low-level OEn to Qn | Waveform 5<br>Waveform 6 | 1.0<br>1.0  | 4.5<br>5.0 | 8.0<br>8.0  | 1.0<br>1.0   | 8.5<br>8.5  | ns   |

## AC SETUP REQUIREMENTS for 74F846

| SYMBOL                                   | PARAMETER                           | TEST CONDITION | LIMITS  |     |  |     | UNIT |
|--|-------------------------------------|----------------|---|-----|--|-----|------|
|  |                                     |                | T <sub>amb</sub> = +25°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |     | T <sub>amb</sub> = 0°C to +70°C<br>V <sub>CC</sub> = +5.0V ± 10%<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |     |      |
|  |                                     |                | MIN   | TYP | MIN  | MAX |      |
| t <sub>s</sub> (H)<br>t <sub>s</sub> (L) | Setup time, High or Low<br>Dn to LE | Waveform 4     | 0.0<br>0.0  |     | 0.0<br>0.0   |     | ns   |
| t <sub>h</sub> (H)<br>t <sub>h</sub> (L) | Hold time, High or Low<br>Dn to LE  | Waveform 4     | 3.0<br>4.0  |     | 3.0<br>4.0   |     | ns   |
| t <sub>w</sub> (H)                       | LE pulse width, High                | Waveform 4     | 3.0   |     | 3.0  |     | ns   |
| t <sub>w</sub> (L)                       | PRE pulse width, Low                | Waveform 3     | 4.0   |     | 5.0  |     | ns   |
| t <sub>w</sub> (H)                       | MR pulse width, Low                 | Waveform 3     | 4.0   |     | 5.0  |     | ns   |
| t <sub>REC</sub>                         | PRE recovery time                   | Waveform 3     | 0.0   |     | 0.0  |     | ns   |
| t <sub>REC</sub>                         | MR recovery time                    | Waveform 3     | 3.5   |     | 4.5  |     | ns   |

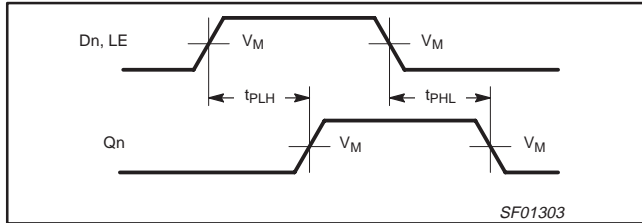
# Bus interface latches

## 74F841/74F842/74F843/ 74F845/74F846

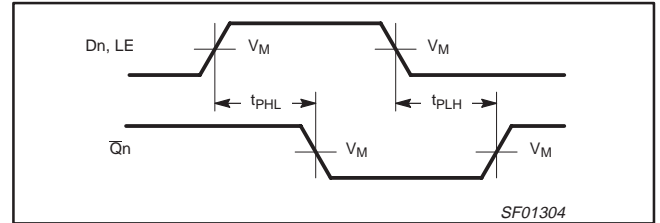
### AC WAVEFORMS

For all waveforms,  $V_M = 1.5V$ .

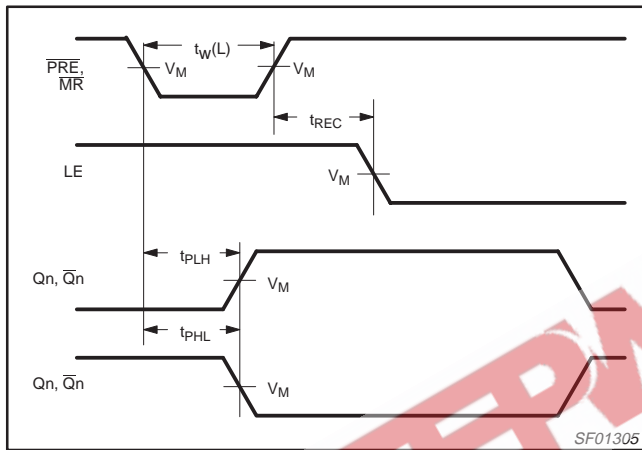
The shaded areas indicate when the input is permitted to change for predictable output performance.



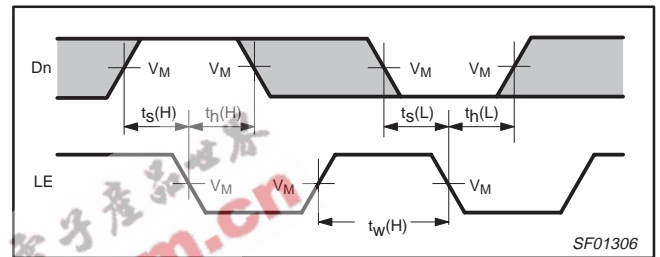
Waveform 1. Propagation Delay, Non-Inverting Path



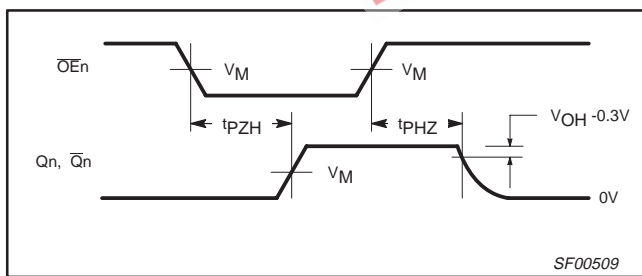
Waveform 2. Propagation Delay, Inverting Path



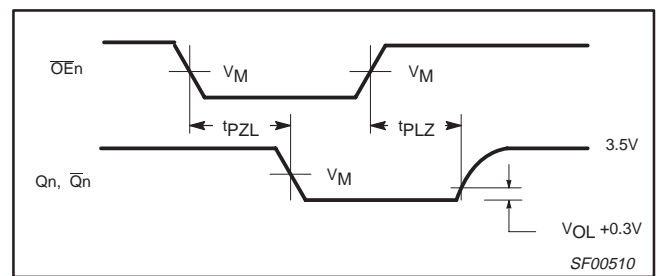
Waveform 3. Master Reset and Preset Pulse Width, Master Reset and Preset to Output Delay, and Master Reset and Preset to Latch Enable Recovery Time



Waveform 4. Data Setup and Hold Times



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 6. 3-State Output Enable Time to Low Level and Output Disable time from Low Level

Bus interface latches

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74F845/74F846

TEST CIRCUIT AND WAVEFORMS

**Test Circuit for 3-State Outputs**

**SWITCH POSITION**

| TEST      | SWITCH |
|-----------|--------|
| $t_{PLZ}$ | closed |
| $t_{pZL}$ | closed |
| All other | open   |

**DEFINITIONS:**  
 $R_L$  = Load resistor; see AC electrical characteristics for value.  
 $C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

**Input Pulse Definition**

| INPUT PULSE REQUIREMENTS |           |       |           |       |           |           |
|--------------------------|-----------|-------|-----------|-------|-----------|-----------|
| family                   | amplitude | $V_M$ | rep. rate | $t_w$ | $t_{TLH}$ | $t_{THL}$ |
| 74F                      | 3.0V      | 1.5V  | 1MHz      | 500ns | 2.5ns     | 2.5ns     |

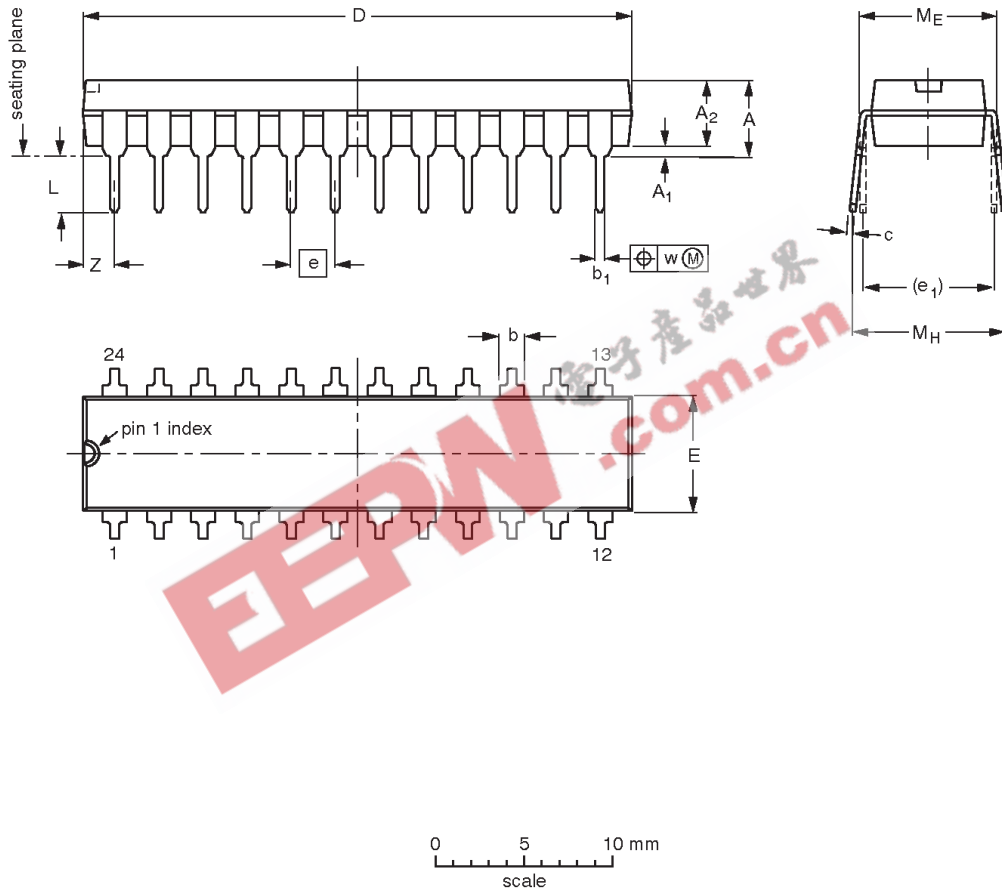
SF00777

Bus interface latches

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DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

| UNIT   | A max. | A <sub>1</sub> min. | A <sub>2</sub> max. | b              | b <sub>1</sub> | c              | D <sup>(1)</sup> | E <sup>(1)</sup> | e     | e <sub>1</sub> | L              | M <sub>E</sub> | M <sub>H</sub> | w    | Z <sup>(1)</sup> max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|------------------|------------------|-------|----------------|----------------|----------------|----------------|------|-----------------------|
| mm     | 4.70   | 0.38                | 3.94                | 1.63<br>1.14   | 0.56<br>0.43   | 0.36<br>0.25   | 31.9<br>31.5     | 6.73<br>6.48     | 2.54  | 7.62           | 3.51<br>3.05   | 8.13<br>7.62   | 10.03<br>7.62  | 0.25 | 2.05                  |
| inches | 0.185  | 0.015               | 0.155               | 0.064<br>0.045 | 0.022<br>0.017 | 0.014<br>0.010 | 1.256<br>1.240   | 0.265<br>0.255   | 0.100 | 0.300          | 0.138<br>0.120 | 0.32<br>0.30   | 0.395<br>0.300 | 0.01 | 0.081                 |

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

| OUTLINE VERSION | REFERENCES |          |      |  | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|------------|
|                 | IEC        | JEDEC    | EIAJ |  |                     |            |
| SOT222-1        |            | MS-001AF |      |  |                     | 95-03-11   |

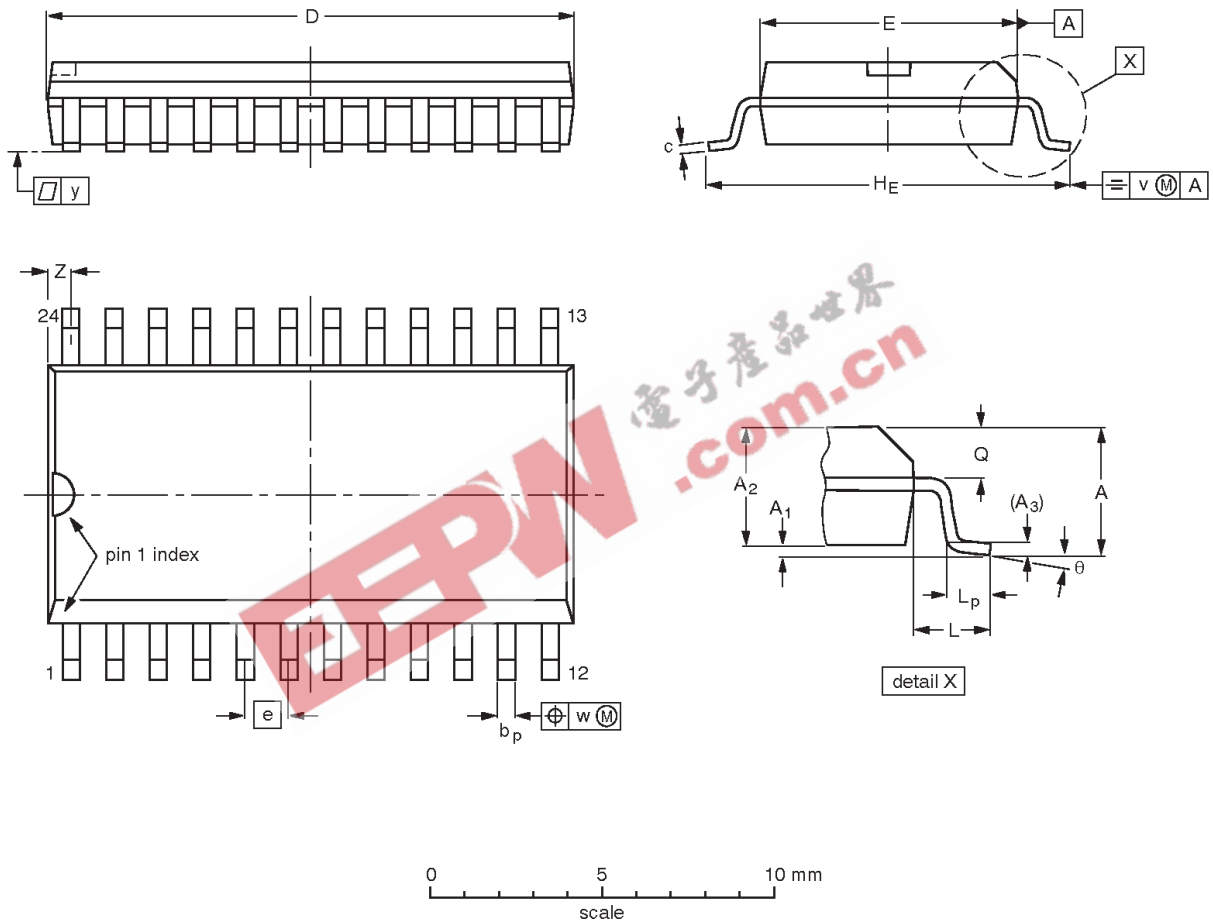


Bus interface latches

74F841/74F842/74F843/  
74F845/74F846

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT   | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c              | D <sup>(1)</sup> | E <sup>(1)</sup> | e     | H <sub>E</sub> | L     | L <sub>p</sub> | Q              | v    | w    | y     | Z <sup>(1)</sup> | θ        |
|--------|--------|----------------|----------------|----------------|----------------|----------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm     | 2.65   | 0.30<br>0.10   | 2.45<br>2.25   | 0.25           | 0.49<br>0.36   | 0.32<br>0.23   | 15.6<br>15.2     | 7.6<br>7.4       | 1.27  | 10.65<br>10.00 | 1.4   | 1.1<br>0.4     | 1.1<br>1.0     | 0.25 | 0.25 | 0.1   | 0.9<br>0.4       | 8°<br>0° |
| inches | 0.10   | 0.012<br>0.004 | 0.096<br>0.089 | 0.01           | 0.019<br>0.014 | 0.013<br>0.009 | 0.61<br>0.60     | 0.30<br>0.29     | 0.050 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016   |          |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |          |      |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|----------|------|--|---------------------|----------------------|
|                 | IEC        | JEDEC    | EIAJ |  |                     |                      |
| SOT137-1        | 075E05     | MS-013AD |      |  |                     | 95-01-24<br>97-05-22 |

# Bus interface latches

74F841/74F842/74F843/  
74F845/74F846

## Data sheet status

| Data sheet status         | Product status | Definition [1]   |
|---------------------------|----------------|--|
| Objective specification   | Development    | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.  |
| Preliminary specification | Qualification  | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| Product specification     | Production     | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.   |

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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