

54F/74F164A Serial-In, Parallel-Out Shift Register

General Description

The 'F164A is a high-speed 8-bit serial-in/parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the LOW-to-HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register, setting all outputs LOW independent of the clock. The 'F164A is a faster version of the 'F164.

Features

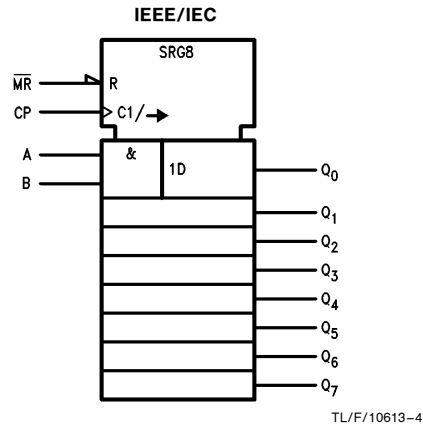
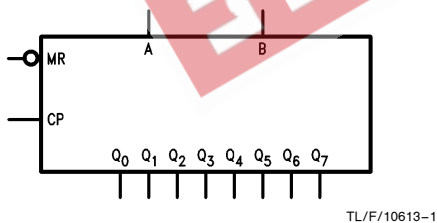
- Typical shift frequency of 90 MHz
- Asynchronous Master Reset
- Gated serial data input
- Fully synchronous data transfers
- Guaranteed 4000V min ESD protection
- 'F164A is a faster version of the 'F164

| Commercial | Military | Package Number | Package Description |
|--------------------|--------------------|----------------|---|
| 74F164APC | | N14A | 14-Lead (0.300" Wide) Molded Dual-In-Line |
| | 54F164ADM (Note 2) | J14A | 14-Lead Ceramic Dual-In-Line |
| 74F164ASC (Note 1) | | M14A | 14-Lead (0.150" Wide) Molded Small Outline, JEDEC |
| 74F164ASJ (Note 1) | | M14D | 14-Lead (0.300" Wide) Molded Small Outline, EIAJ |
| | 74F164AFM (Note 2) | W14B | 14-Lead Cerpack |
| | 74F164ALM (Note 2) | E20A | 20-Lead Ceramic Leadless Chip Carrier, Type C |

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

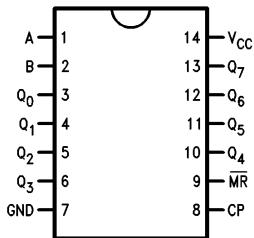
Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbols



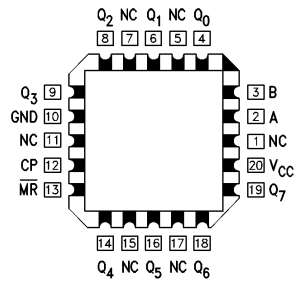
Connection Diagrams

Pin Assignment for
DIP, SOIC and Flatpak



TL/F/10613-2

Pin Assignment
for LCC



TL/F/10613-3

Unit Loading/Fan Out

| Pin Names | Description | 54F/74F | |
|--------------------------------|--|------------------|---|
| | | U.L. HIGH/LOW | Input I _{IH} /I _{IL} Output I _{OH} /I _{OL} |
| A, B | Data Inputs | 1.0/1.0 | 20 μ A/ -0.6 mA |
| CP | Clock Pulse Input (Active Rising Edge) | 1.0/1.0 | 20 μ A/ -0.6 mA |
| $\overline{\text{MR}}$ | Master Reset Input (Active LOW) | 1.0/1.0 | 20 μ A/ -0.6 mA |
| Q ₀ -Q ₇ | Outputs | 50/33.3 | -1 mA/20 mA |

Functional Description

The 'F164A is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q₀ the logical AND of the two data inputs (A • B) that existed before the rising clock edge. A LOW level on the Master Reset ($\overline{\text{MR}}$) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

Mode Select Table

| Operating Mode | Inputs | | | Outputs | |
|----------------|------------------------|---|---|----------------|--------------------------------|
| | $\overline{\text{MR}}$ | A | B | Q ₀ | Q ₁ -Q ₇ |
| Reset (Clear) | L | X | X | L | L-L |
| Shift | H | l | l | L | q ₀ -q ₆ |
| | H | l | h | L | q ₀ -q ₆ |
| | H | h | l | L | q ₀ -q ₆ |
| | H | h | h | H | q ₀ -q ₆ |

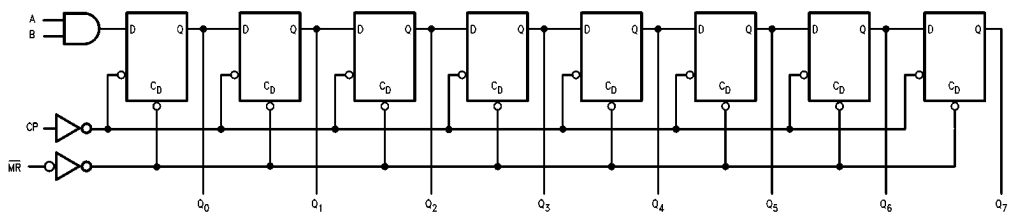
H(h) = HIGH Voltage Levels

L(l) = LOW Voltage Levels

X = Immaterial

q_n = Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

Logic Diagram



TL/F/10613-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|--------------------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature under Bias | -55°C to +125°C |
| Junction Temperature under Bias | -55°C to +175°C |
| Plastic | -55°C to +150°C |
| V _{CC} Pin Potential to Ground Pin | -0.5V to +7.0V |
| Input Voltage (Note 2) | -0.5V to +7.0V |
| Input Current (Note 2) | -30 mA to +5.0 mA |
| Voltage Applied to Output in HIGH State (with V _{CC} = 0V) | |
| Standard Output | -0.5V to V _{CC} |
| TRI-STATE® Output | -0.5V to +5.5V |

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

ESD Last Passing Voltage (Min) 4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

| | |
|------------------------------|-----------------|
| Free Air Ambient Temperature | |
| Military | -55°C to +125°C |
| Commercial | 0°C to +70°C |
| Supply Voltage | |
| Military | +4.5V to +5.5V |
| Commercial | +4.5V to +5.5V |

DC Electrical Characteristics

| Symbol | Parameter | 54F/74F | | | Units | V _{CC} | Conditions |
|------------------|-----------------------------------|--|-------------------|-------------|-------|-----------------|---|
| | | Min | Typ | Max | | | |
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | | Recognized as a HIGH Signal |
| V _{IL} | Input LOW Voltage | | | 0.8 | V | | Recognized as a LOW Signal |
| V _{CD} | Input Clamp Diode Voltage | | | -1.2 | V | Min | I _{IN} = -18 mA |
| V _{OH} | Output HIGH Voltage | 54F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC} | 2.5 2.5 2.7 | | V | Min | I _{OH} = -1 mA I _{OH} = -1 mA I _{OH} = -1 mA |
| V _{OL} | Output LOW Voltage | 54F 10% V _{CC} 74F 10% V _{CC} | | 0.5 0.5 | V | Min | I _{OL} = 20 mA I _{OL} = 20 mA |
| I _{IH} | Input HIGH Current | 54F 74F | | 20.0 5.0 | μA | Max | V _{IN} = 2.7V |
| I _{BVI} | Input HIGH Current Breakdown Test | 54F 74F | | 100 7.0 | μA | Max | V _{IN} = 7.0V |
| I _{CEx} | Output HIGH Leakage Current | 54F 74F | | 250 50 | μA | Max | V _{OUT} = V _{CC} |
| V _{ID} | Input Leakage Test | 74F | 4.75 | | V | 0.0 | I _{ID} = 1.9 μA All other pins grounded |
| I _{OD} | Output Leakage Circuit Current | 74F | | 3.75 | μA | 0.0 | V _{IOD} = 150 mV All other pins grounded |
| I _{IL} | Input LOW Current | | | -0.6 | mA | Max | V _{IN} = 0.5V |
| I _{OS} | Output Short-Circuit Current | | -60 | -150 | mA | Max | V _{OUT} = 0V |
| I _{CC} | Power Supply Current | | 35 | 55 | mA | Max | CP = HIGH MR = GND, A, B = GND |

AC Electrical Characteristics

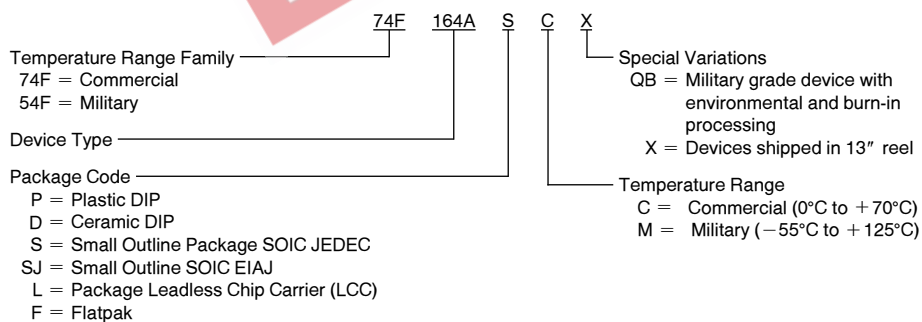
| Symbol | Parameter | 74F | | | 54F | | 74F | | Units |
|------------------|---|---|-----|------|--|------|--|------|-------|
| | | T _A = +25°C V _{CC} = +5.0V C _L = 50 pF | | | T _A , V _{CC} = Mil C _L = 50 pF | | T _A , V _{CC} = Com C _L = 50 pF | | |
| | | Min | Typ | Max | Min | Max | Min | Max | |
| f _{max} | Maximum Clock Frequency | 80 | 120 | | 60 | | 80 | | MHz |
| t _{PLH} | Propagation Delay | 3.0 | 4.8 | 7.5 | 2.5 | 9.0 | 3.0 | 7.5 | ns |
| t _{PHL} | CP to Q _n | 3.5 | 5.0 | 8.0 | 3.0 | 8.5 | 3.5 | 8.0 | |
| t _{PHL} | Propagation Delay MR to Q _n | 5.0 | 7.0 | 10.0 | 4.0 | 12.5 | 5.0 | 10.5 | ns |

AC Operating Requirements

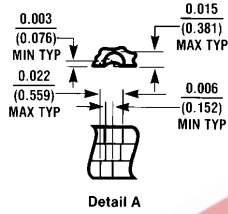
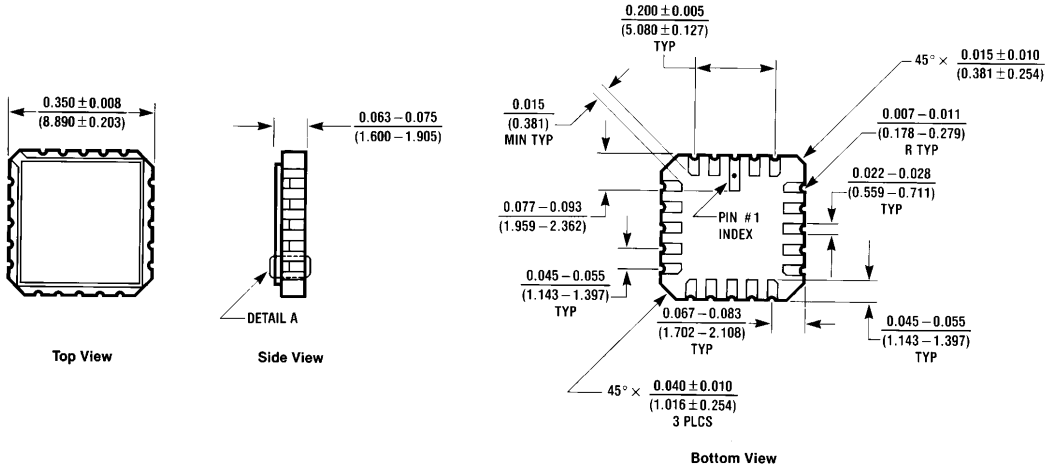
| Symbol | Parameter | 74F | | 54F | | 74F | | Units |
|--------------------|---------------------------|---|-----|--|-----|--|-----|-------|
| | | T _A = +25°C V _{CC} = +5.0V | | T _A , V _{CC} = Mil | | T _A , V _{CC} = Com | | |
| | | Min | Max | Min | Max | Min | Max | |
| t _s (H) | Setup Time, HIGH or LOW | 4.5 | | 5.5 | | 4.5 | | ns |
| t _s (L) | A or B to CP | 4.0 | | 4.0 | | 4.0 | | |
| t _h (H) | Hold Time, HIGH or LOW | 1.0 | | 1.0 | | 1.0 | | ns |
| t _h (L) | A or B to CP | 1.0 | | 1.0 | | 1.0 | | |
| t _w (H) | CP Pulse Width | 4.0 | | 4.0 | | 4.0 | | ns |
| t _w (L) | HIGH or LOW | 7.0 | | 7.0 | | 7.0 | | |
| t _w (L) | MR Pulse Width, LOW | 4.0 | | 5.0 | | 4.0 | | ns |
| t _{rec} | Recovery Time MR to CP | 5.0 | | 6.5 | | 5.0 | | ns |

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

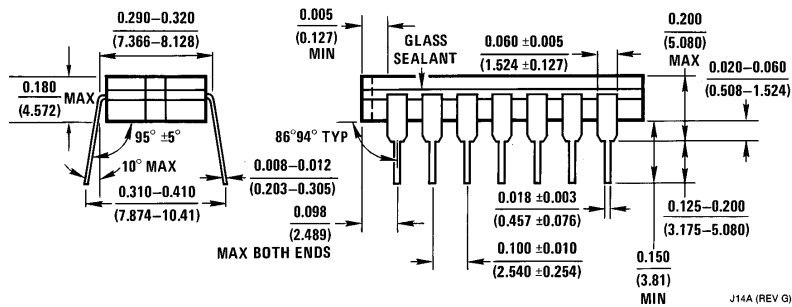
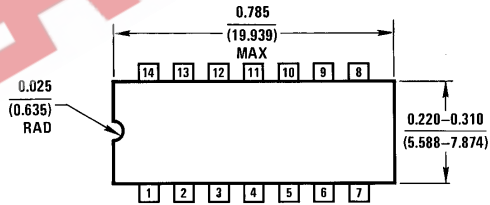


Physical Dimensions inches (millimeters)



20-Lead Ceramic Leadless Chip Carrier, Type C (L)
 NS Package Number E20A

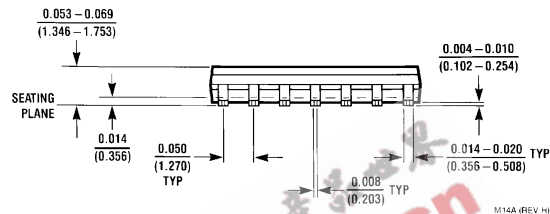
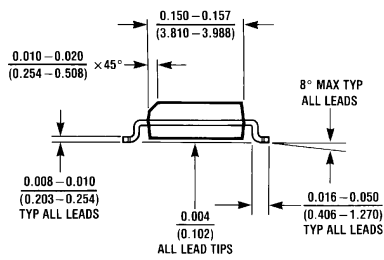
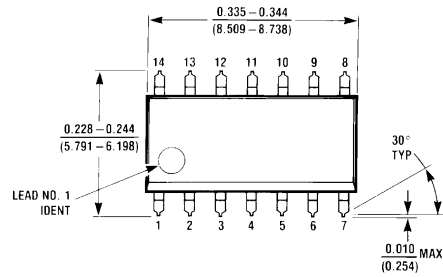
E20A (REV D)



14-Lead Ceramic Dual-In-Line Package (D)
 NS Package Number J14A

J14A (REV G)

Physical Dimensions inches (millimeters) (Continued)

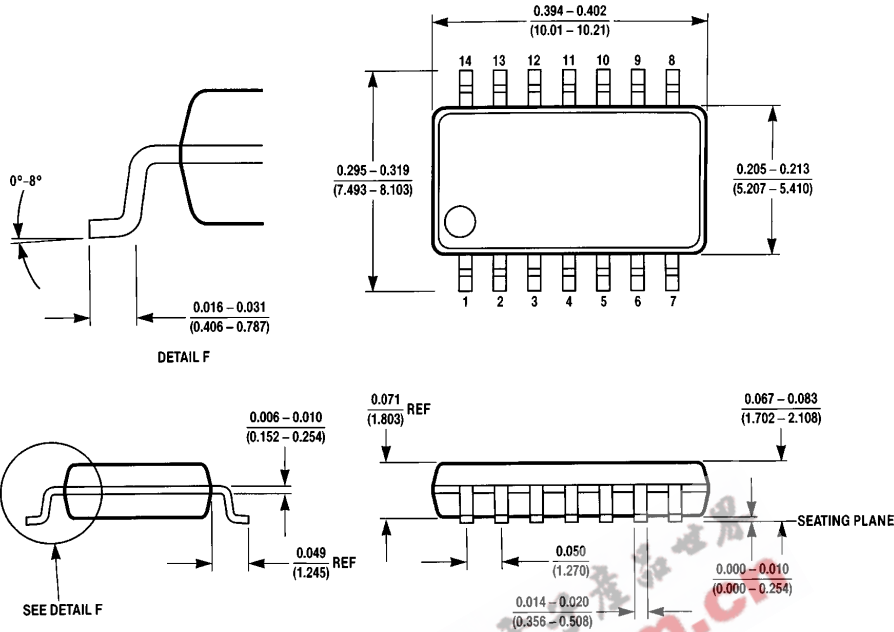


14-Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M14A

M14A (REV. H)

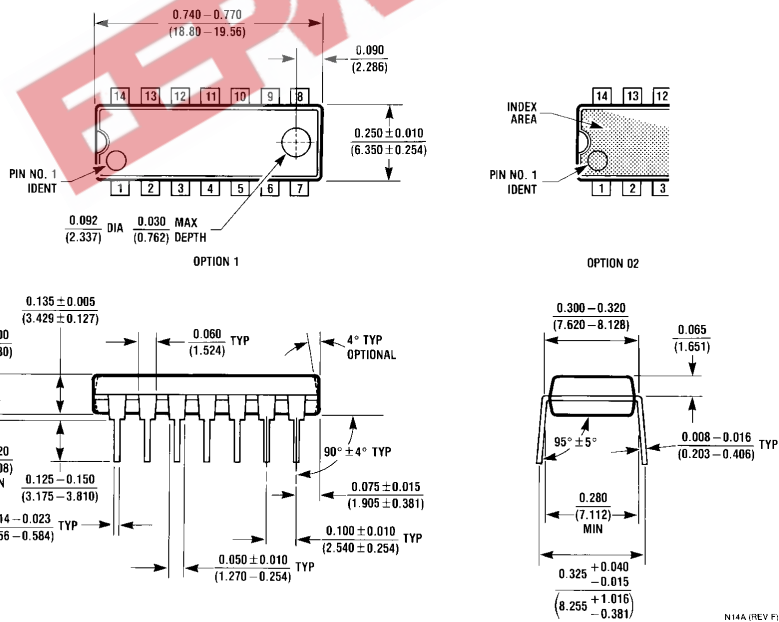
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Physical Dimensions inches (millimeters) (Continued)



14-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M14D

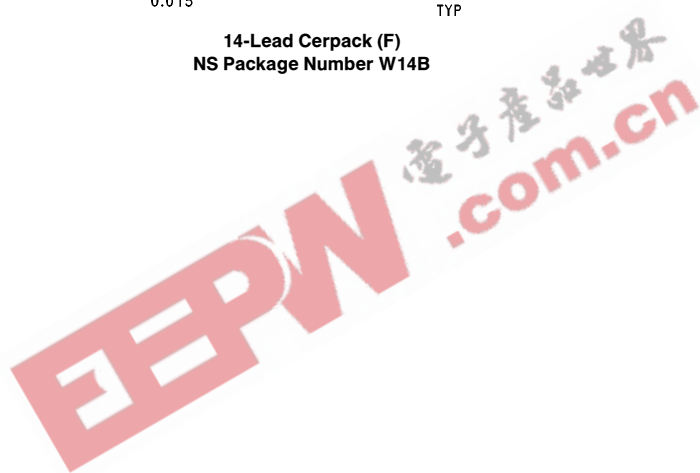
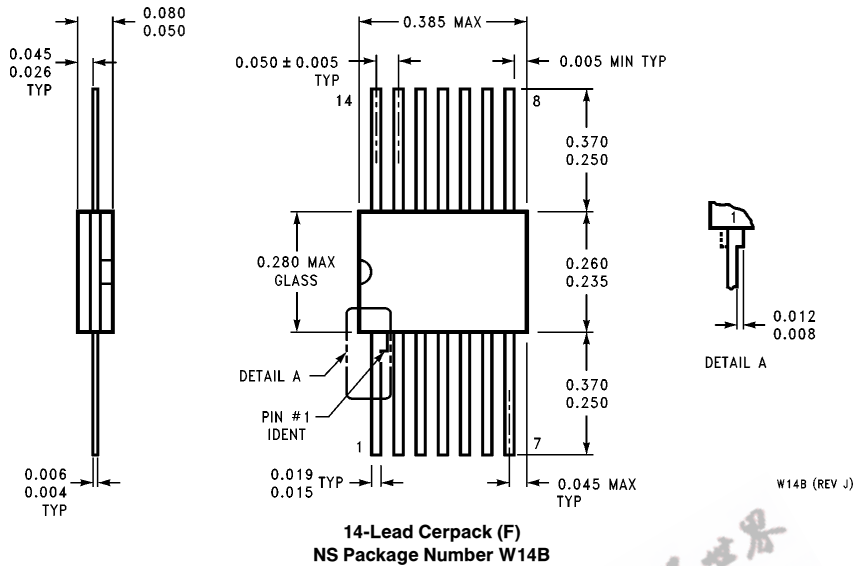
M14D (REV A)



14-Lead (0.300" Wide) Plastic Dual-In-Line Package (P)
NS Package Number N14A

N14A (REV F)

Physical Dimensions inches (millimeters) (Continued)



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