

DATA SHEET

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74ALS164

8-bit serial-in parallel-out shift register

Product specification
IC05 Data Handbook

1991 Feb 08

8-bit serial-in parallel-out shift register

74ALS164

FEATURES

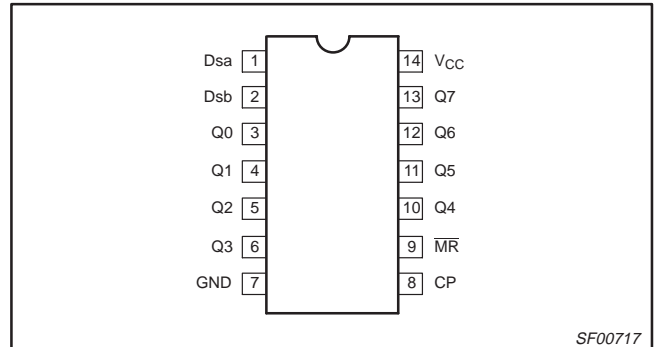
- Gated serial data inputs
- Typical shift frequency of 75MHz
- Asynchronous master reset
- Buffered clock and data inputs
- Fully synchronous data transfer

DESCRIPTION

The 74ALS164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (Dsa, Dsb); either input can be used as an active-high enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied High.

Data shifts one place to the right on each Low-to-high transition of the clock (CP) input, and enters into Q0 the logical AND of the two data inputs (Dsa, Dsb) that existed one setup time before the rising edge. A Low level on the Master reset (\overline{MR}) input overrides all other inputs and clears the register asynchronously, forcing all outputs Low.

PIN CONFIGURATION



| TYPE | TYPICAL f_{MAX} | TYPICAL SUPPLY CURRENT (TOTAL) |
|----------|-------------------|--------------------------------|
| 74ALS164 | 75MHz | 10mA |

ORDERING INFORMATION

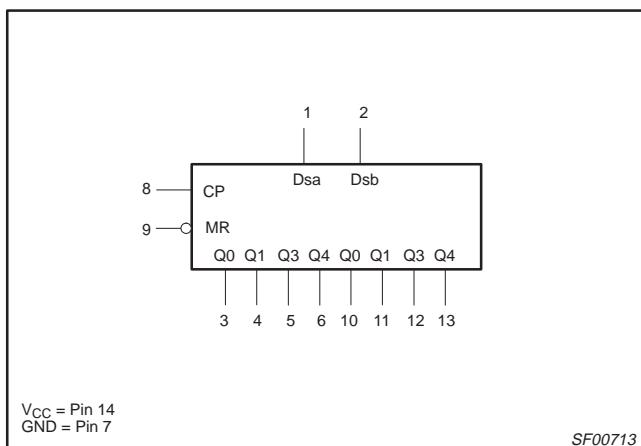
| DESCRIPTION | ORDER CODE | DRAWING NUMBER |
|--------------------|--|----------------|
| | COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$ | |
| 14-pin plastic DIP | 74ALS164N | SOT27-1 |
| 14-pin plastic SO | 74ALS164D | SOT108-1 |

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

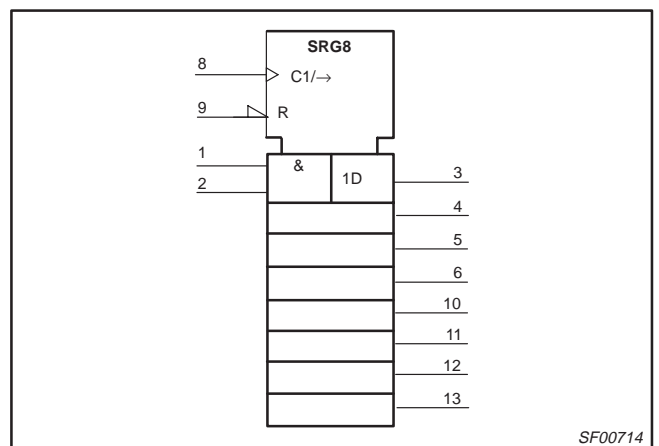
| PINS | DESCRIPTION | 74ALS (U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|-----------------|--|-----------------------|---------------------|
| Dsa, Dsb | Data inputs | 1.0/1.0 | 20 μ A/0.1mA |
| CP | Clock Pulse input (active rising edge) | 1.0/1.0 | 20 μ A/0.1mA |
| \overline{MR} | Master Reset input (active-Low) | 1.0/1.0 | 20 μ A/0.1mA |
| Q0 – Q7 | Data outputs | 20/80 | 0.4mA/8mA |

NOTE: One (1.0) ALS unit load is defined as: 20 μ A in the High state and 0.1mA in the Low state.

LOGIC SYMBOL



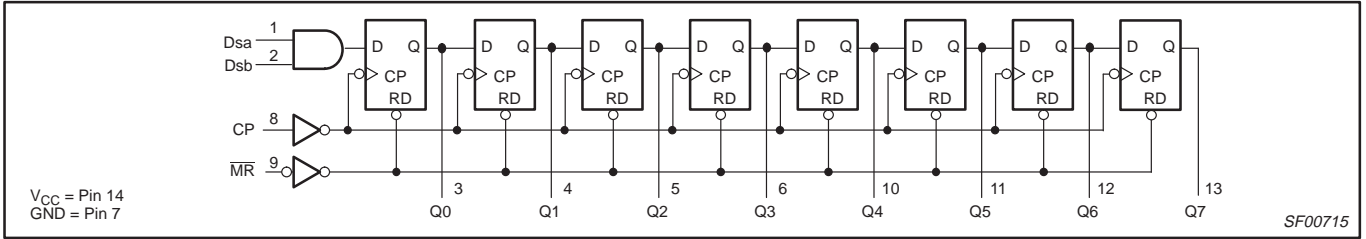
IEC/IEEE SYMBOL



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LOGIC DIAGRAM



MODE SELECT FUNCTION TABLE

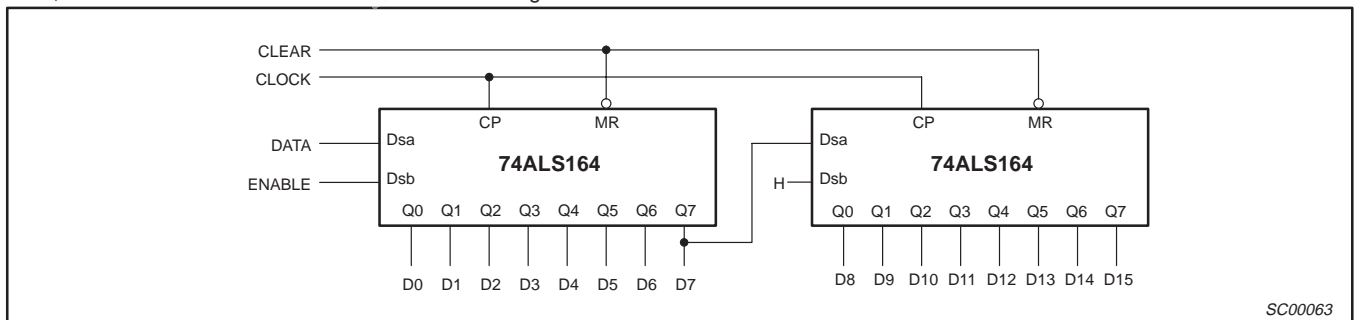
| INPUTS | | | | OUTPUTS | | | | | | | | OPERATING MODE | |
|--------|----|-----|-----|---------|----|----|----|----|----|----|----|----------------|---------------|
| MR | CP | Dsa | Dsb | Q0 | Q1 | Q2 | Q3 | Q4 | Q5 | Q6 | Q7 | | |
| L | X | X | X | L | L | L | L | L | L | L | L | L | Reset (Clear) |
| H | ↑ | l | l | L | q0 | q1 | q2 | q3 | q4 | q5 | q6 | | Shift |
| H | ↑ | l | h | L | q0 | q1 | q2 | q3 | q4 | q5 | q6 | | |
| H | ↑ | h | h | H | q0 | q1 | q2 | q3 | q4 | q5 | q6 | | |

NOTES:

- H = High voltage level
- h = High voltage level one setup time prior to the Low-to-High clock transition
- L = Low voltage level
- l = Low voltage level one setup time prior to the Low-to-High clock transition
- qn = Lower case letter indicate the state of the referenced output one setup time prior to the Low-to-High clock transition.
- X = Don't care
- ↑ = Low-to-High clock transition

APPLICATION

The 74ALS164 can be cascaded to form synchronous shift registers of longer length. Here, two devices are combined to form a 16-bit shift register.



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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

| SYMBOL | PARAMETER | RATING | UNIT |
|-----------|--|------------------|------|
| V_{CC} | Supply voltage | -0.5 to +7.0 | V |
| V_{IN} | Input voltage | -0.5 to +7.0 | V |
| I_{IN} | Input current | -30 to +5 | mA |
| V_{OUT} | Voltage applied to output in High output state | -0.5 to V_{CC} | V |
| I_{OUT} | Current applied to output in Low output state | 16 | mA |
| T_{amb} | Operating free-air temperature range | 0 to +70 | °C |
| T_{stg} | Storage temperature range | -65 to +150 | °C |

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|-----------|--------------------------------------|--------|-----|------|------|
| | | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| V_{IH} | High-level input voltage | 2.0 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | V |
| I_{IK} | Input clamp current | | | -18 | mA |
| I_{OH} | High-level output current | | | -0.4 | mA |
| I_{OL} | Low-level output current | | | 8 | mA |
| T_{amb} | Operating free-air temperature range | 0 | | +70 | °C |

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | TEST CONDITIONS ¹ | LIMITS | | | UNIT |
|----------|--|---|-----------------------|------------------|------|---------------|
| | | | MIN | TYP ² | MAX | |
| V_{OH} | High-level output voltage | $V_{CC} \pm 10\%$, $V_{IL} = \text{MAX}$, $V_{IH} = \text{MIN}$, $I_{OH} = \text{MAX}$ | $V_{CC} - 2$ | | | V |
| V_{OL} | Low-level output voltage | $V_{CC} = \text{MIN}$, $V_{IL} = \text{MAX}$, $V_{IH} = \text{MIN}$ | $I_{OL} = 4\text{mA}$ | 0.25 | 0.4 | V |
| | | | $I_{OL} = 8\text{mA}$ | 0.35 | 0.50 | V |
| V_{IK} | Input clamp voltage | $V_{CC} = \text{MIN}$, $I_I = I_{IK}$ | | -0.73 | -1.5 | V |
| I_I | Input current at maximum input voltage | $V_{CC} = \text{MAX}$, $V_I = 7.0\text{V}$ | | | 100 | μA |
| I_{IH} | High-level input current | $V_{CC} = \text{MAX}$, $V_I = 2.7\text{V}$ | | | 20 | μA |
| I_{IL} | Low-level input current | $V_{CC} = \text{MAX}$, $V_I = 0.5\text{V}$ | | | -0.1 | mA |
| I_O | Output current ³ | $V_{CC} = \text{MAX}$, $V_O = 2.25\text{V}$ | -30 | | -112 | mA |
| I_{CC} | Supply current (total) | $V_{CC} = \text{MAX}$ | | 10 | 15 | mA |

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_{amb} = 25^\circ\text{C}$.
- The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

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AC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | UNIT |
|------------------------|--|----------------|---|--------------|------|
| | | | $T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}, R_L = 500\Omega$ | | |
| | | | MIN | MAX | |
| f_{MAX} | Maximum clock frequency | Waveform 1 | 50 | | MHz |
| t_{PLH} t_{PHL} | Propagation delay CP to Qn | Waveform 1 | 5.0 6.0 | 13.0 15.0 | ns |
| t_{PHL} | Propagation delay, \overline{MR} to Qn | Waveform 2 | 8.0 | 18.0 | ns |

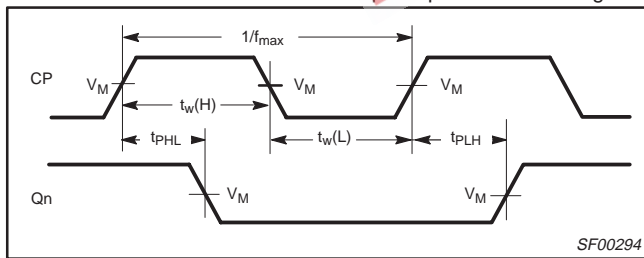
AC SETUP REQUIREMENTS

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | UNIT |
|----------------------------|--------------------------------------|----------------|---|-----|------|
| | | | $T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}, R_L = 500\Omega$ | | |
| | | | MIN | MAX | |
| $t_{su(H)}$ $t_{su(L)}$ | Setup time, High or Low Dn to CP | Waveform 3 | 6.0 5.0 | | ns |
| $t_h(H)$ $t_h(L)$ | Hold time, High or Low Dn to CP | Waveform 3 | 0 0 | | ns |
| $t_w(H)$ $t_w(L)$ | Clock pulse width, High or Low | Waveform 1 | 10.0 7.0 | | ns |
| $t_w(L)$ | \overline{MR} pulse width, Low | Waveform 2 | 6.0 | | ns |
| t_{REC} | Recovery time, \overline{MR} to CP | Waveform 2 | 6.0 | | ns |

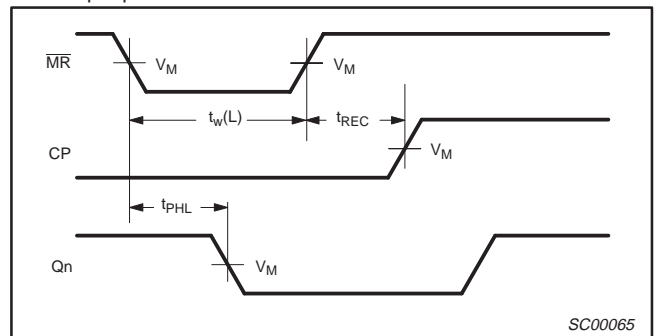
AC WAVEFORMS

For all waveforms, $V_M = 1.3\text{V}$.

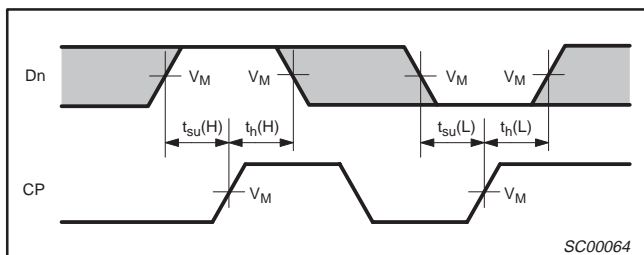
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay for Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Clock Recovery Time

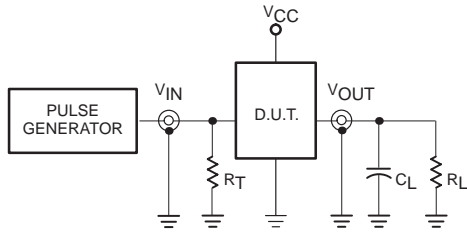


Waveform 3. Data Setup and Hold Times

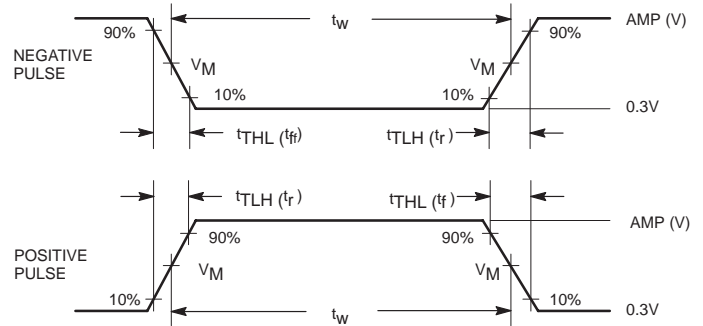
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TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-pole Outputs



Input Pulse Definition

DEFINITIONS:

- R_L = Load resistor; see AC electrical characteristics for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

| Family | INPUT PULSE REQUIREMENTS | | | | | |
|--------|--------------------------|-------|----------|-------|-----------|-----------|
| | Amplitude | V_M | Rep.Rate | t_w | t_{TLH} | t_{THL} |
| 74ALS | 3.5V | 1.3V | 1MHz | 500ns | 2.0ns | 2.0ns |

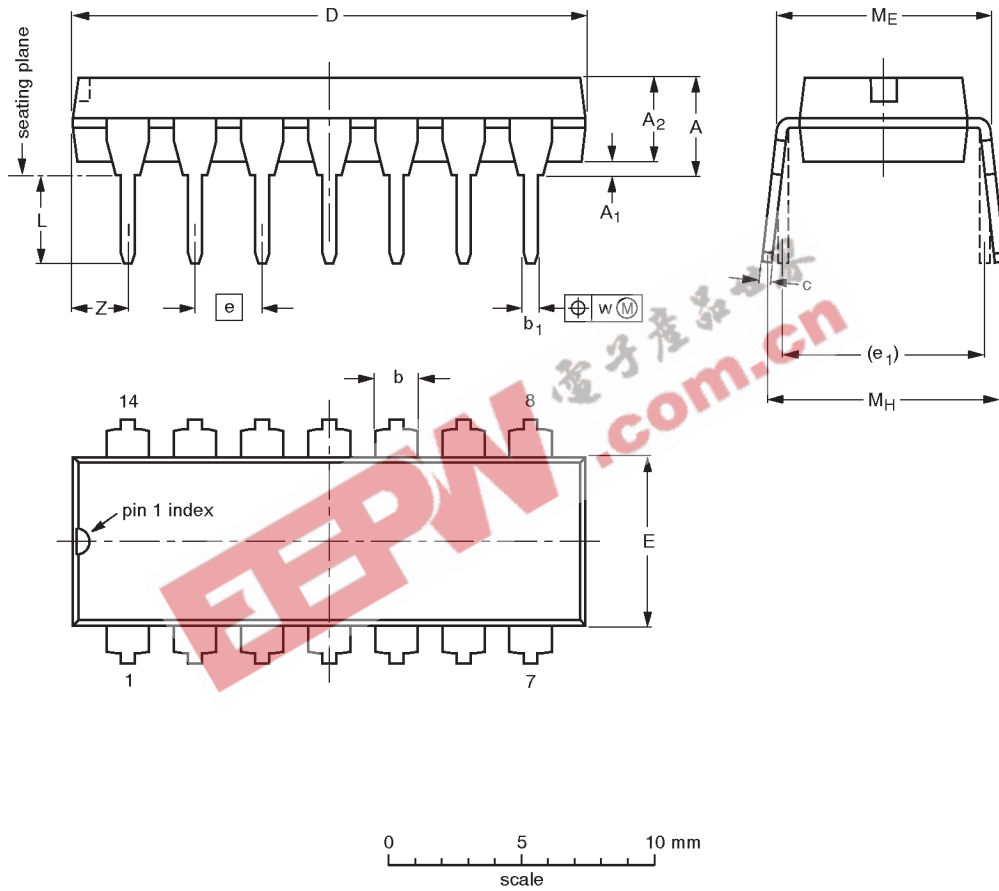
SC00005

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DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ min. | A ₂ max. | b | b ₁ | c | D ⁽¹⁾ | E ⁽¹⁾ | e | e ₁ | L | M _E | M _H | w | Z ⁽¹⁾ max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|-----------------------|
| mm | 4.2 | 0.51 | 3.2 | 1.73 1.13 | 0.53 0.38 | 0.36 0.23 | 19.50 18.55 | 6.48 6.20 | 2.54 | 7.62 | 3.60 3.05 | 8.25 7.80 | 10.0 8.3 | 0.254 | 2.2 |
| inches | 0.17 | 0.020 | 0.13 | 0.068 0.044 | 0.021 0.015 | 0.014 0.009 | 0.77 0.73 | 0.26 0.24 | 0.10 | 0.30 | 0.14 0.12 | 0.32 0.31 | 0.39 0.33 | 0.01 | 0.087 |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

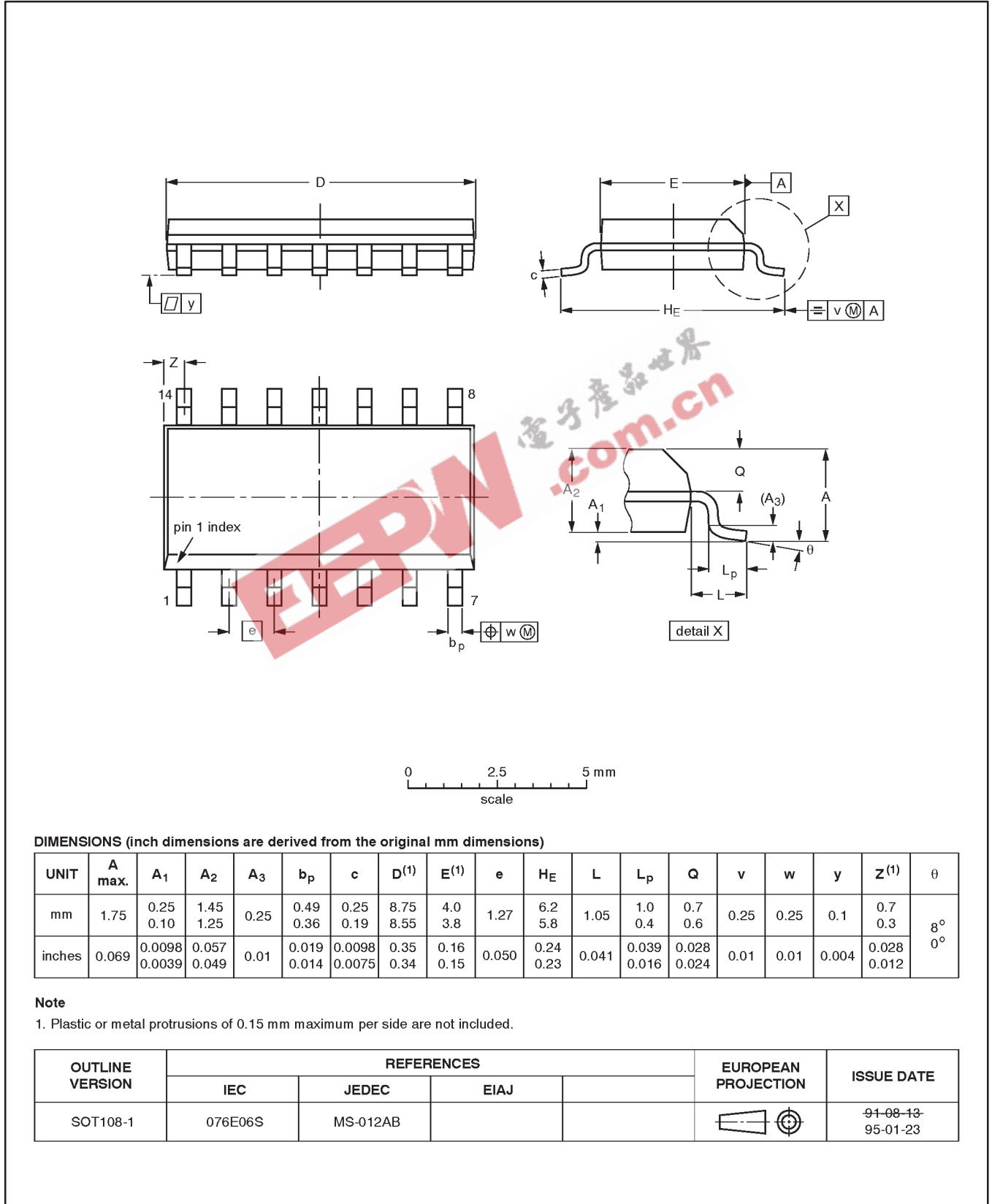
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT27-1 | 050G04 | MO-001AA | | | | 92-11-17 95-03-11 |

8-bit serial-in parallel-out shift register

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | z ⁽¹⁾ | θ |
|--------|--------|------------------|----------------|----------------|----------------|------------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm | 1.75 | 0.25 0.10 | 1.45 1.25 | 0.25 | 0.49 0.36 | 0.25 0.19 | 8.75 8.55 | 4.0 3.8 | 1.27 | 6.2 5.8 | 1.05 | 1.0 0.4 | 0.7 0.6 | 0.25 | 0.25 | 0.1 | 0.7 0.3 | 8° 0° |
| inches | 0.069 | 0.0098 0.0039 | 0.057 0.049 | 0.01 | 0.019 0.014 | 0.0098 0.0075 | 0.35 0.34 | 0.16 0.15 | 0.050 | 0.24 0.23 | 0.041 | 0.039 0.016 | 0.028 0.024 | 0.01 | 0.01 | 0.004 | 0.028 0.012 | |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT108-1 | 076E06S | MS-012AB | | | | 91-08-13 95-01-23 |

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DEFINITIONS

| Data Sheet Identification | Product Status | Definition |
|----------------------------------|-------------------------------|--|
| <i>Objective Specification</i> | Formative or in Design | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice. |
| <i>Preliminary Specification</i> | Preproduction Product | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
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