

## 9-Bit address/data Futurebus transceiver, ADT

## 74F8965/74F8966

## FEATURES

- 9-bit transceiver (both directions)
- Drives heavily loaded backplanes with equivalent load impedances down to 10 ohms
- High drive (100mA) open collector drivers on B port
- Reduced voltage swing (1V to 2V) produces less noise and reduces power consumption
- High speed operation enhances performance of backplane buses and facilitates incident wave switching
- Compatible with IEEE 896 futurebus standards and IEEE 1194 BTL standard
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Controlled output ramp and multiple GND pins minimize ground bounce
- Glitch-free power up/power down operation

- Guaranteed skew of less than 2ns

## DESCRIPTION

The 74F8965 and 74F8966 are 9-bit bidirectional latchable transceivers and are intended to provide the electrical interface to a high performance wired-OR bus. The B port inverting drivers are low-capacitance open collector with controlled ramp and are designed to sink 100mA from 2 volts. The B port inverting receivers have a precision band gap references for improved noise margins.

The B port interfaces to 'Backplane Transceiver Logic' (BTL). BTL features a reduced (1V to 2V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading.

Incident wave switching is employed, therefore BTL propagation delays are short. Although the voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.

BTL offers low power consumption, low ground bounce, EMI and crosstalk, low capacitive loading, superior noise margin and low propagation delays. This results in a high bandwidth, reliable backplane.

The 74F8965 and 74F8966 A ports have TTL 3-state drivers and TTL receivers. The B ports have standard BTL I/O with 100mA current sink capability. The B-to-A path is a simple inverted buffered path. When going from A-to-B the user may choose between a buffered path or a latching function.

The 74F8966 also has an idle arbitrator/multiple competitors output. The  $\overline{\text{IAMC}}$  output compares, using a wired-OR configuration, the data on the bus to the latched data presented to the bus. If the bus data matches the data presented by the 74F8966 then  $\overline{\text{IAMC}}$  is high. If the data doesn't match then  $\overline{\text{IAMC}}$  goes low.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT( TOTAL)
74F8965	3.5ns	80mA
74F8966	3.5ns	80mA

## ORDERING INFORMATION

DESCRIPTION	ORDER CODE
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$
44-pin PLCC	N74F8965A, N74F8966A

## INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A8	TTL data inputs	1.0/0.033	20 $\mu$ A/20 $\mu$ A
$\overline{B0}$ – $\overline{B8}$	Data inputs with threshold circuitry	5.0/0.167	100 $\mu$ A/100 $\mu$ A
OEA, OEB0, $\overline{OEB1}$	Output enable inputs	1.0/0.167	20 $\mu$ A/100 $\mu$ A
$\overline{\text{LS}}$	Latch select (active low) ('F8965)	1.0/0.167	20 $\mu$ A/100 $\mu$ A
$\overline{\text{IAREQ}}$	Idle arbitration request (active low) ('F8965)	1.0/0.167	20 $\mu$ A/100 $\mu$ A
$\overline{\text{LE}}$	Latch enable input (active low)	1.0/0.167	20 $\mu$ A/100 $\mu$ A
A0 – A8	3-state TTL outputs	150/40	3mA/24mA
$\overline{B0}$ – $\overline{B8}$	Open collector BTL outputs	OC/166.7	OC/100mA
$\overline{\text{IAMC}}$	Idle arbitration/multiple competitors output ('F8966)	OC/80	OC/48mA

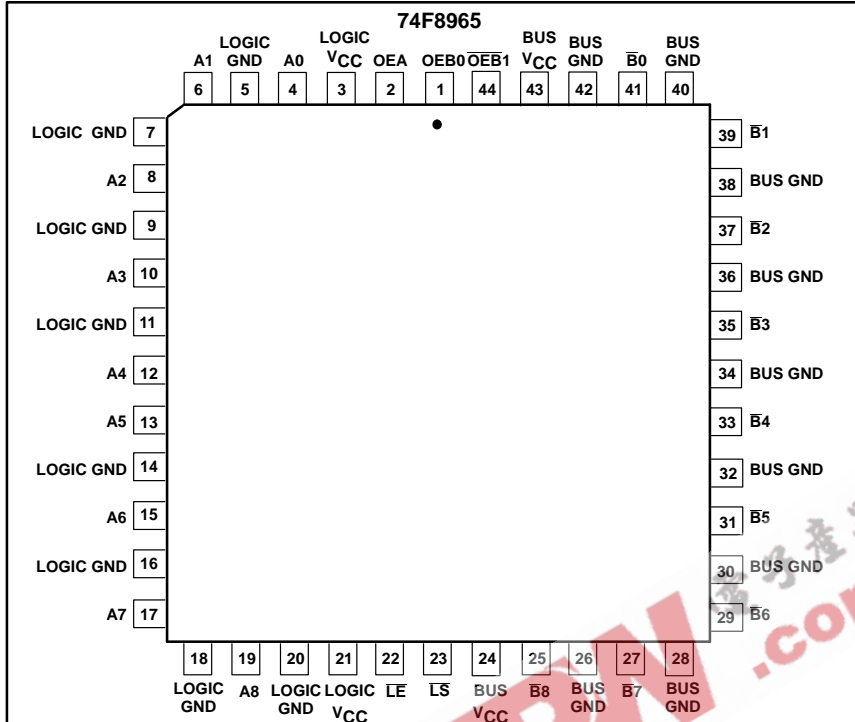
## Notes to input and output loading and fan out table

1. One (1.0) FAST unit load is defined as: 20 $\mu$ A in the high state and 0.6mA in the low state.
2. OC = Open collector.

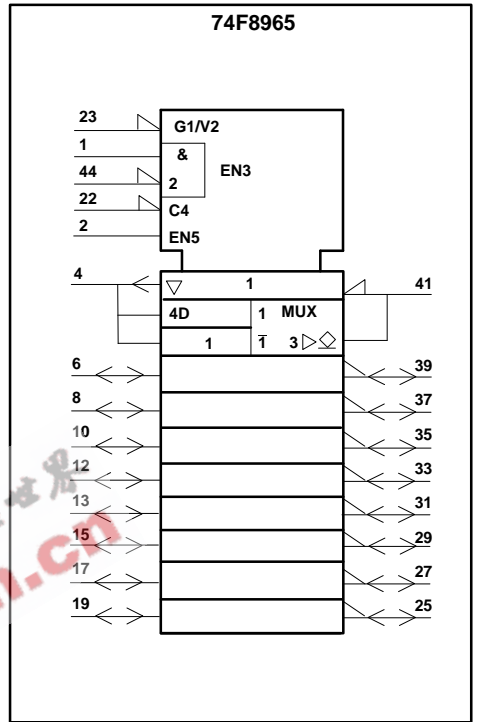
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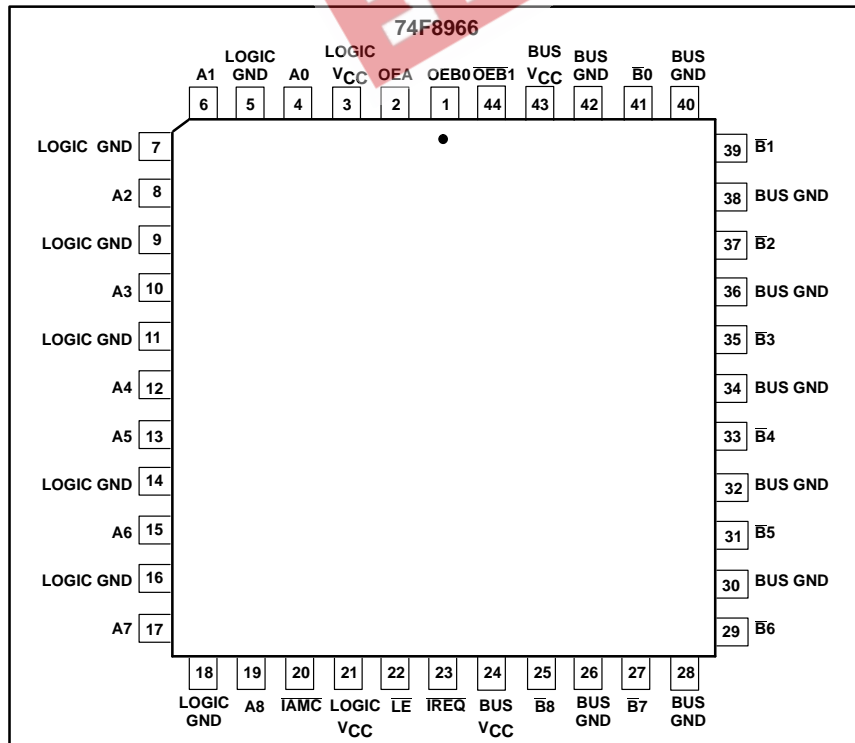
### PIN CONFIGURATION PLCC



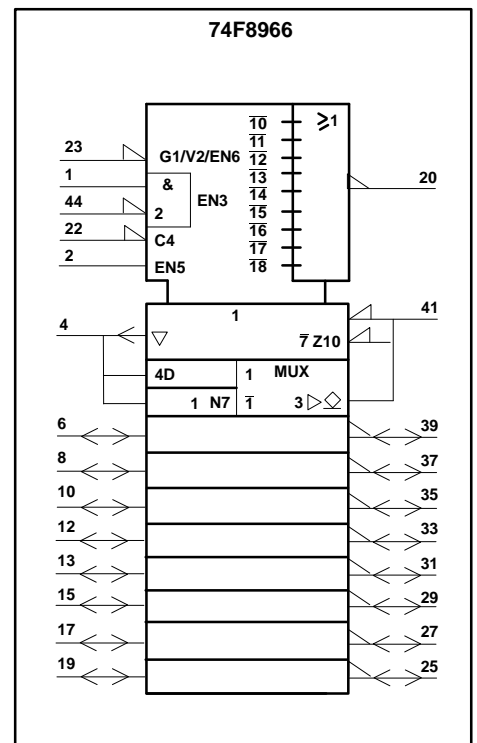
### IEC/IEEE SYMBOL



### PIN CONFIGURATION PLCC



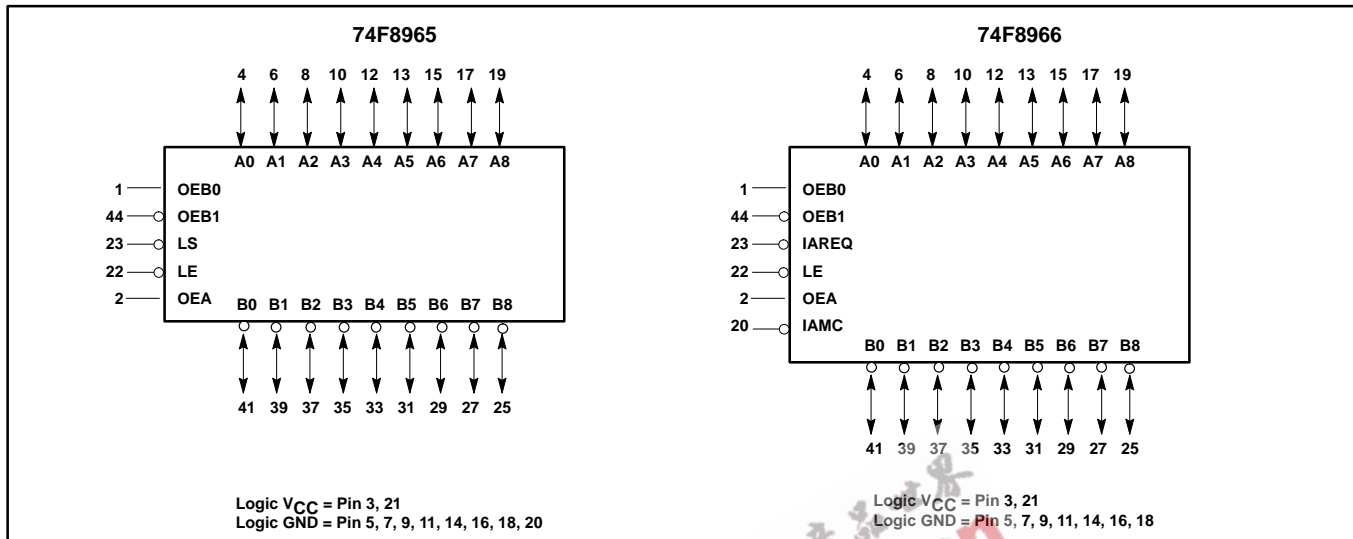
### IEC/IEEE SYMBOL



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LOGIC SYMBOL



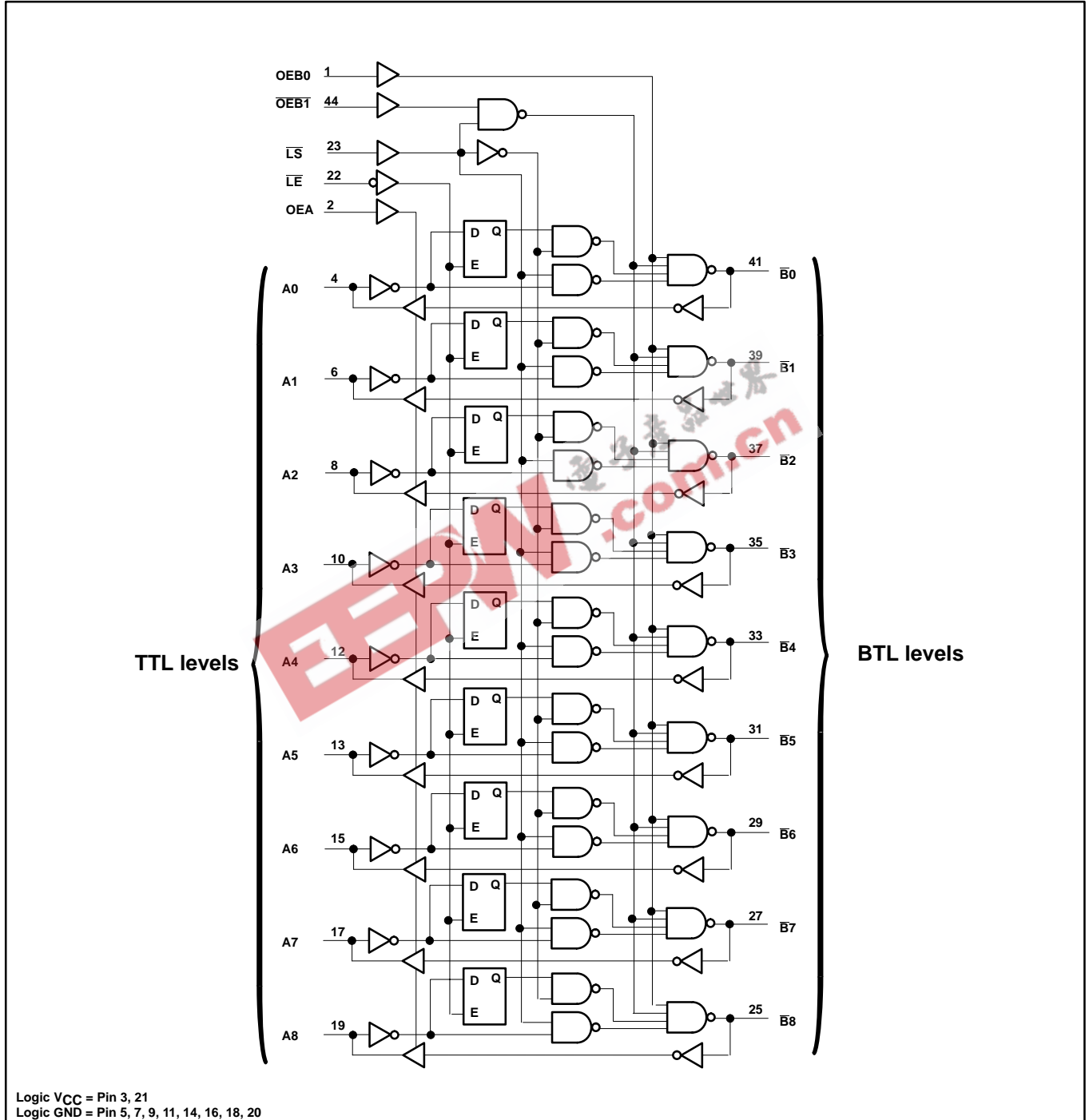
PIN DESCRIPTION

SYMBOL	PINS	TYPE	NAME AND FUNCTION
A0 – A8	4, 6, 8, 10, 12, 13, 15, 17, 19	I/O	Data inputs/TTL 3–state outputs
$\overline{B0} - \overline{B8}$	41, 39, 37, 35, 33, 31, 29, 27, 25	I/O	Data inputs / open collector outputs, high current drives.
OEBO	1	Input	Output enable input. Enables the B outputs when high.
$\overline{OEB1}$	44	Input	Output enable input. Enables the B outputs when low.
OEA	2	Input	Output enable input. Enables the A outputs when high.
$\overline{LE}$	22	Input	Latch enable input. Enables latch when low.
$\overline{LS}$	23	Input	Latch select input. Selects latch when low (74F8965).
$\overline{IAREQ}$	23	Input	Idle arbitration request input (74F8966).
$\overline{IAMC}$	20	Output	Idle arbitration/multiple competitors output (open collector output) (74F8966).
Bus GND	26, 28, 30, 32, 34, 36, 38, 40, 42	Ground	Bus ground (0V)
Logic GND	5, 7, 9, 11, 14, 16, 18, 20 (74F8965)	Ground	Logic ground (0V)
Bus V <sub>CC</sub>	24, 43	Power	Positive supply voltages
Logic V <sub>CC</sub>	3, 21	Power	Positive supply voltages

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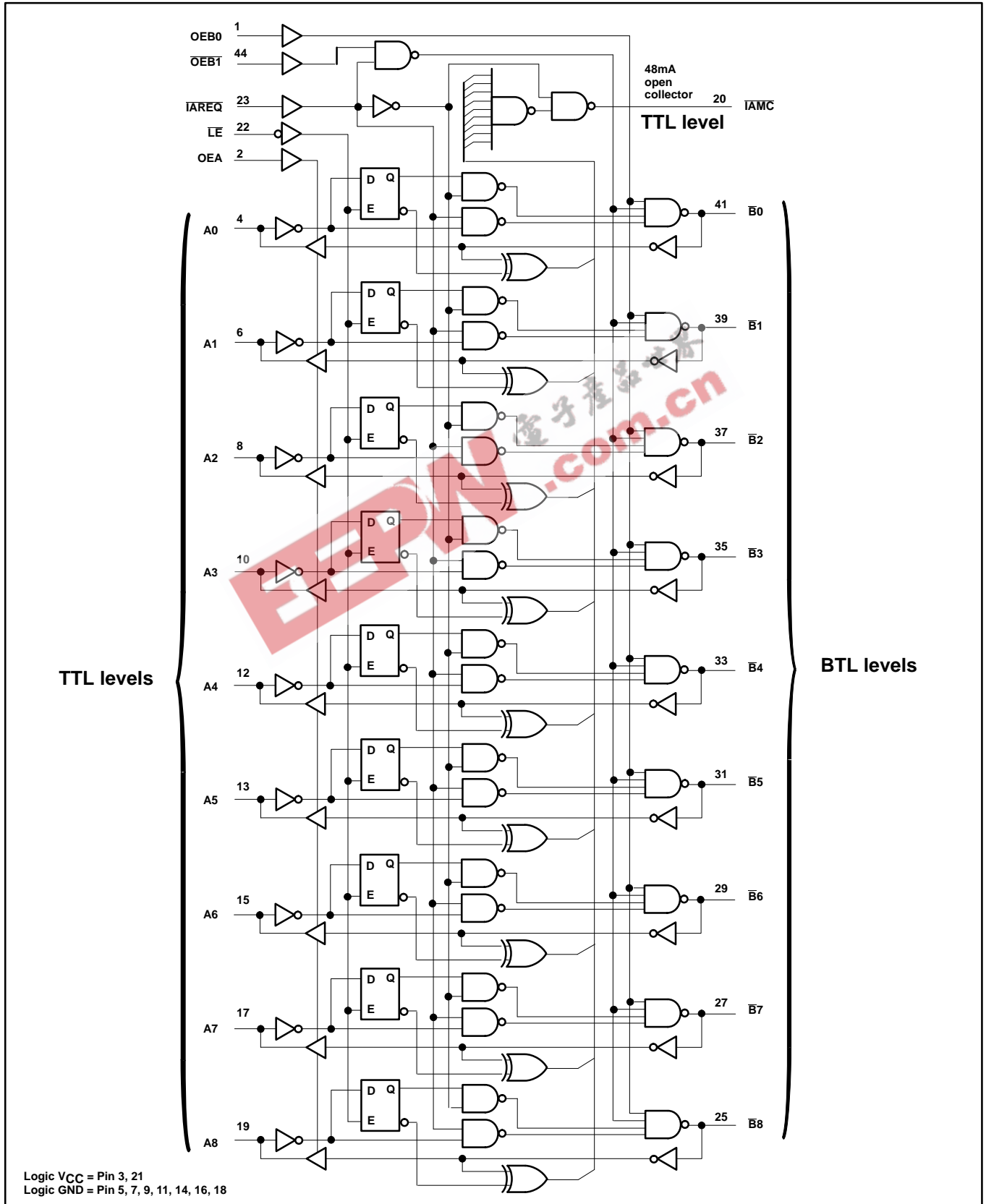
LOGIC DIAGRAM FOR 74F8965



# 9-Bit address/data Futurebus transceiver, ADT

## 74F8965/74F8966

### LOGIC DIAGRAM FOR 74F8966



## 9-Bit address/data Futurebus transceiver, ADT

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FUNCTION TABLE FOR 74F8965

INPUTS							LATCH STATE	OUTPUTS		OPERATING MODE
AIn	Bn*	OEB0	OEB1	LS	OEA	LE		An	Bn	
L	–	H	L	H	L	X	X	input	H**	An to Bn bypass latch
H	–	H	L	H	L	X	X	input	L	
L	–	H	L	L	L	L	H	input	H**	An to Bn transparent latch
H	–	H	L	L	L	L	L	input	L	
l	–	H	L	L	L	↑	H	input	H**	An to Bn latch and read
h	–	H	L	L	L	↑	L	input	L	
–	–	H	L	L	H	H	H	L	H**	An to Bn outputs latched and read (preconditioned latch)
–	–	H	L	L	H	H	L	H	L	
X	–	H	L	L	L	H	NC	input	L	An to Bn hold
X	X	L	X	X	X	X	X	X	H**	Disable Bn outputs
X	X	X	H	H	X	X	X	X	H**	
–	L	L	H	H	H	X	X	H	input	Bn to An
–	H	L	H	H	H	X	X	L	input	
–	X	X	X	X	L	X	X	X	X	Disable An outputs

## Notes to function table for 74F8965

1. H = High voltage level
2. h = High voltage level one setup time prior to the low-to-high LE transition
3. L = Low voltage level
4. l = Low voltage level one setup time prior to the low-to-high LE transition
5. NC= No change
6. X = Don't care
7. Z = High impedance "off" state
8. – = Input not externally driven
9. ↑ = Low-to-high transition
10. H\*\*= Goes to level of pullup voltage.
11. B\* = Precaution should be taken to insure B inputs do not float. If they do they are equal to low state.

FUNCTION TABLE FOR 74F8966

INPUTS								LATCH STATE	OUTPUTS			OPERATING MODE
AIn	Bn*	OEB0	OEB1	IAREQ	LS	OEA	LE		An	Bn	IAMC	
L	–	H	L	L	H	L	X	X	input	H**	H**	An to Bn bypass latch
H	–	H	L	L	H	L	X	X	input	L	H**	
L	–	H	L	L	L	L	L	H	input	H**	H**	An to Bn transparent latch
H	–	H	L	L	L	L	L	L	input	L	H**	
l	–	H	L	L	L	L	↑	H	input	H**	H**	An to Bn latch and read
h	–	H	L	L	L	L	↑	L	input	L	H**	
–	–	H	L	L	L	H	H	H	L	H**	H**	An to Bn outputs latched and read (preconditioned latch)
–	–	H	L	L	L	H	H	L	H	L	H**	
X	–	H	L	L	L	L	H	NC	input	NC	H**	An to Bn hold
X	X	L	X	X	X	X	X	X	X	H**	H**	Disable Bn outputs
X	X	X	H	H	H	X	X	X	X	H**	H**	
–	L	L	H	H	H	H	X	X	H	input	H**	Bn to An
–	H	L	H	H	H	H	X	X	L	input	H**	
–	Bn	L	H	H	↓*	H	H	Bn	Z	Bn	L	Latch Bn data idle arbitration request (preconditioned latch)
–	Bn	L	H	H	↓*	H	H	Bn	Z	Bn	H**	
–	X	X	X	X	X	L	X	X	Z	X	X	Disable An outputs

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**Notes to function table for 74F8966**

1. H = High voltage level
2. h = High voltage level one setup time prior to the low-to-high  $\overline{LE}$  transition
3. L = Low voltage level
4. l = Low voltage level one setup time prior to the low-to-high  $\overline{LE}$  transition
5. NC= No change
6. X = Don't care
7. Z = High impedance "off" state
8. – = Input not externally driven
9.  $\uparrow$  = Low-to-high transition
10.  $\downarrow^*$  = High-to-low transition, latch must be preconditioned before  $\overline{IAREQ}$
11. H\*\*= Goes to level of pullup voltage.
12. B\* = Precaution should be taken to insure B inputs do not float. If they do they are equal to low state.

**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V <sub>CC</sub>	Supply voltage		-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	OE $\overline{B}$ 0, OE $\overline{B}$ 1, LEA, $\overline{LE}$	-0.5 to +7.0	V
		A0 – A8, $\overline{B}$ 0 – $\overline{B}$ 8	-0.5 to +5.5	V
I <sub>IN</sub>	Input current		-40 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in high output state		-0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in low output state	A0 – A8	48	mA
		I $\overline{AMC}$ (74F8966 only)	96	mA
		$\overline{B}$ 0 – $\overline{B}$ 8	200	mA
T <sub>amb</sub>	Operating free air temperature range		0 to +70	°C
T <sub>stg</sub>	Storage temperature range		-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	Except $\overline{B}$ 0 – $\overline{B}$ 8	2.0		V
		$\overline{B}$ 0 – $\overline{B}$ 8	1.625	1.55	V
V <sub>IL</sub>	Low-level input voltage	Except $\overline{B}$ 0 – $\overline{B}$ 8		0.8	V
		$\overline{B}$ 0 – $\overline{B}$ 8		1.475	V
I <sub>Ik</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current	A0 – A8		-3	mA
V <sub>OH</sub>	High-level output voltage	I $\overline{AMC}$ (74F8966 only)	4.5		V
I <sub>OL</sub>	Low-level output current	A0 – A8		24	mA
		I $\overline{AMC}$ (74F8966 only)		48	mA
		$\overline{B}$ 0 – $\overline{B}$ 8		100	mA
T <sub>amb</sub>	Operating free air temperature	0		+70	°C

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## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT
				MIN	TYP <sup>2</sup>	MAX	
I <sub>OH</sub>	High-level output current	$\bar{B}0 - \bar{B}8$	$V_{CC} = \text{MAX}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, V_{OH} = 2.1\text{V}$			100	$\mu\text{A}$
		I $\bar{A}M\bar{C}$ (74F8966)	$V_{CC} = \text{MAX}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, V_{OH} = 4.5\text{V}$			100	$\mu\text{A}$
I <sub>OFF</sub>	Power-off output current	$\bar{B}0 - \bar{B}8$	$V_{CC} = 0.0\text{V}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, V_{OH} = 2.1\text{V}$			100	$\mu\text{A}$
		I $\bar{A}M\bar{C}$ (74F8966)	$V_{CC} = 0.0\text{V}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, V_{OH} = 4.5\text{V}$			100	$\mu\text{A}$
V <sub>OH</sub>	High-level output voltage	A0 – A8 <sup>4</sup>	$V_{CC} = \text{MAX}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, I_{OH} = -3\text{mA}$	2.4		V <sub>CC</sub>	V
V <sub>OL</sub>	Low-level output voltage	A0 – A8 <sup>4</sup>	$V_{CC} = \text{MIN},$ $I_{OL} = 24\text{mA}$			0.50	V
		I $\bar{A}M\bar{C}$ (74F8966)	$V_{IL} = \text{MAX},$ $I_{OL} = 48\text{mA}$			0.50	V
		$\bar{B}0 - \bar{B}8$	$V_{IH} = \text{MIN},$ $I_{OL} = 100\text{mA}$	0.75	1.0	1.10	V
V <sub>IK</sub>	Input clamp voltage		$V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.2	V
I <sub>I</sub>	Input current at maximum input voltage	OEB0, OEB1, OEA, LE, LS, IAREQ	$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$			100	$\mu\text{A}$
		A0 – A8, $\bar{B}0 - \bar{B}8$	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1	mA
I <sub>IH</sub>	High-level input current	OEB0, OEB1, OEA, LE, LS, IAREQ	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$			20	$\mu\text{A}$
		$\bar{B}0 - \bar{B}8$	$V_{CC} = \text{MAX}, V_I = 2.1\text{V}$			100	$\mu\text{A}$
I <sub>IL</sub>	Low-level input current	OEB0, OEB1, OEA, LE, LS, IAREQ	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$			-100	$\mu\text{A}$
		$\bar{B}0 - \bar{B}8$	$V_{CC} = \text{MAX}, V_I = 0.3\text{V}$			-100	$\mu\text{A}$
I <sub>IH</sub> + I <sub>OZH</sub>	Off-state output current, high-level voltage applied	A0 – A8	$V_{CC} = \text{MAX}, V_O = 2.7\text{V}$			50	$\mu\text{A}$
I <sub>IL</sub> + I <sub>OZL</sub>	Off-state output current, low-level voltage applied		$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$			-50	$\mu\text{A}$
I <sub>OS</sub>	Short circuit output current <sup>3</sup>	A0 – A8 only AO8	$V_{CC} = \text{MAX}$	-60		-150	mA
I <sub>CC</sub>	Supply current (total)	I <sub>CC</sub> H	$V_{CC} = \text{MAX}$		80	140	mA
		I <sub>CC</sub> L	$V_{CC} = \text{MAX}, V_{IL} = 0.5\text{V}$		85	145	mA
		I <sub>CC</sub> Z			75	100	mA

## Notes to DC electrical characteristics

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at  $V_{CC} = 5\text{V}, T_{\text{amb}} = 25^\circ\text{C}$ .
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.
- Due to test equipment limitations, actual test conditions are for  $V_{IH} = 1.8\text{V}$  and  $V_{IL} = 1.3\text{V}$ .



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## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay B <sub>n</sub> to A <sub>n</sub>	Waveform 2	3.0 2.5	5.0 4.5	8.0 7.5	2.5 2.5	8.5 8.0	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time to high or low, OEA to A <sub>n</sub>	Waveform 5, 6	7.5 9.0	9.0 11.0	12.0 13.5	6.0 7.5	14.0 16.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable from high or low, OEA to A <sub>n</sub>	Waveform 5, 6	3.0 4.0	5.0 6.0	8.0 9.0	2.5 4.0	9.0 10.0	ns
t <sub>sk(o)</sub>	Skew between receivers in same package	Waveform 4		0.5	1.0		1.0	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>D</sub> = 30pF, R <sub>U</sub> = 9Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>D</sub> = 30pF, R <sub>U</sub> = 9Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay A <sub>n</sub> to B <sub>n</sub> (transparent latch)	Waveform 2	2.5 3.0	4.0 5.0	7.0 7.5	2.0 2.5	8.0 9.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay A <sub>n</sub> to B <sub>n</sub> (bypass latch)	Waveform 2	1.0 1.5	3.0 3.0	5.5 5.5	1.0 1.0	6.0 6.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay LE to B <sub>n</sub>	Waveform 1, 2	3.0 4.0	5.0 5.5	8.0 8.5	3.0 3.5	8.5 9.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Output enable/disable time, OEB0 to B <sub>n</sub>	Waveform 2	4.0 5.0	6.0 6.5	8.5 9.5	3.5 3.5	10.0 11.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Output enable/disable time, OEB1 to B <sub>n</sub>	Waveform 1	5.5 3.0	7.5 5.0	10.0 8.0	5.0 2.5	11.0 8.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay IAREQ or LS to B <sub>n</sub>	Waveform 1, 2	4.5 2.0	7.5 6.5	10.0 9.5	4.0 2.0	11.0 11.0	ns
t <sub>TLH</sub> t <sub>THL</sub>	Transition time, B <sub>n</sub> port 10% to 90%, 90% to 10%	Test circuit and waveforms		2.0 2.0		1.0 1.0	3.0 3.0	ns
t <sub>sk(o)</sub>	Skew between drivers in same package	Waveform 4		1.0	2.0		2.0	ns
SYMBOL	PARAMETER	TEST CONDITION	IAMC PORT LIMITS (74F8966 only)					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay A <sub>n</sub> to IAMC (latches preset)	Waveform 2	10.5 7.0	14.5 12.0	18.0 15.0	9.5 6.0	20.0 17.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay IAREQ to IAMC	Waveform 2	6.5 2.5	8.0 4.5	11.0 7.0	6.0 2.0	11.5 8.0	ns

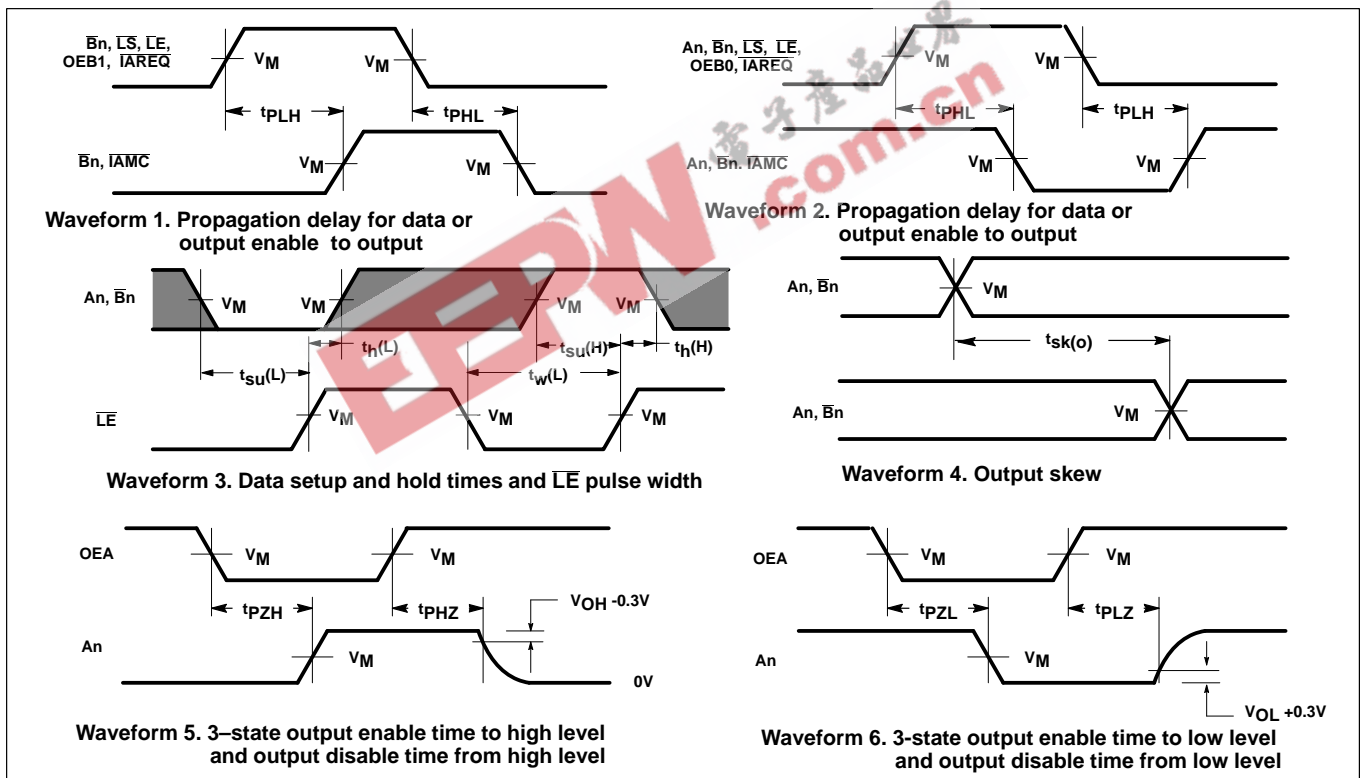
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AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>su</sub> (H) t <sub>su</sub> (L)	Setup time, high or low An to $\overline{LE}$	Waveform 3	2.5 0.0			3.0 0.0		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, high or low An to $\overline{LE}$	Waveform 3	4.0 2.5			5.0 3.0		ns
t <sub>w</sub> (L)	$\overline{LE}$ pulse width, low	Waveform 3	4.0			4.5		ns

AC WAVEFORMS



Notes to AC waveforms

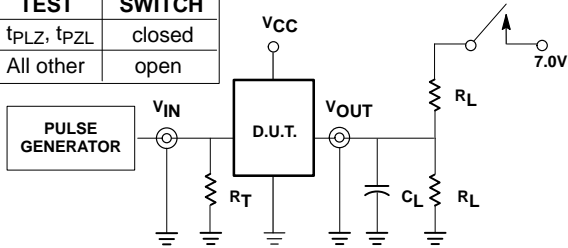
1. For all waveforms,  $V_M = 1.5V$ .
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

9-Bit address/data Futurebus transceiver, ADT

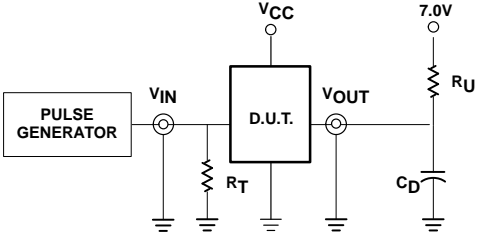
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TEST CIRCUITS AND WAVEFORMS

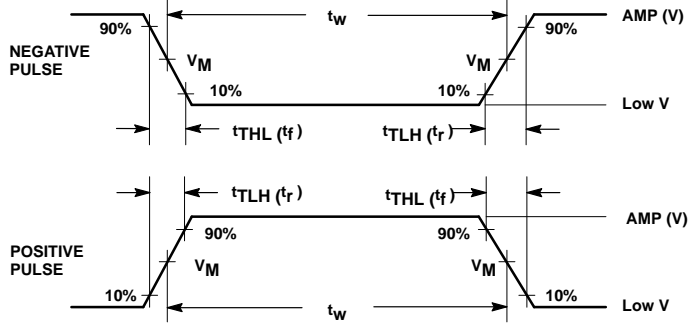
SWITCH POSITION	
TEST	SWITCH
$t_{PLZ}$ , $t_{PZL}$	closed
All other	open



Test circuit for 3-state outputs on A port



Test circuit for outputs on B port



Input pulse definition

family	INPUT PULSE REQUIREMENTS						
	amplitude	Low V	V <sub>M</sub>	rep. rate	t <sub>w</sub>	t <sub>TLH</sub>	t <sub>THL</sub>
A port	3.0V	0.0V	1.5V	1MHz	500ns	2.5ns	2.5ns
B port	3.0V	1.0V	1.5V	1MHz	500ns	4.0ns	4.0ns

**DEFINITIONS:**

$R_L$  = Load resistor; see AC electrical characteristics for value.  
 $C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.  
 $R_U$  = Pull up resistor; see AC electrical characteristics for value.  
 $C_D$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.