DATA SHEET

74F198
8-bit bidirectional universal shift register

Product specification

1987 Oct 02

IC15 Data Handbook

Philips
Semiconductors

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8-bit bidirectional universal shift register 74F198

FEATURES

- Buffered clock and control inputs
- Shift right, shift left, and parallel load capability
- Asynchronous Master Reset

DESCRIPTION

The 74F198 Bidirectional Universal Shift Register is designed to incorporate virtually all of the features a system designer may want in a shift register. This circuit features parallel inputs and outputs, shift right and shift left serial inputs, operating mode select inputs, and direct overriding master reset input. The register has four distinct modes of operation:

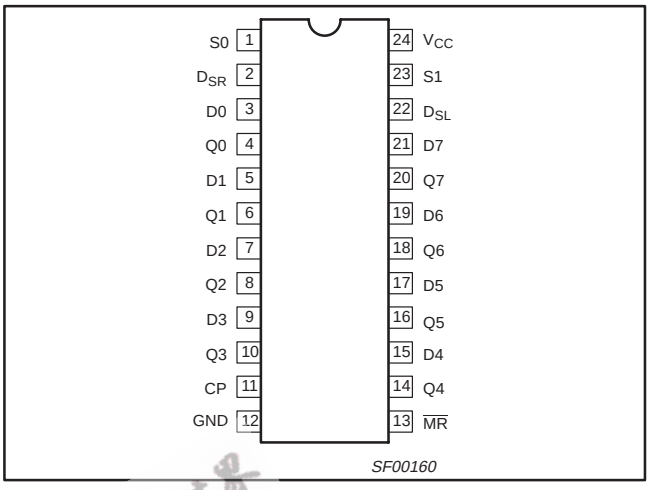
– Parallel (broadside) load
– Shift right (in the direction Q0 toward Q7)
– Shift left (in the direction Q7 toward Q0)
– Inhibit clock (do nothing).

Synchronous parallel loading is accomplished by applying the 8 bits of data and taking both mode control inputs, S0 and S1, High. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock inputs. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously, with the rising edge of the clock pulse when S0 is High and S1 is Low. Serial data for this mode is entered at the right data input (D_{SR}). When S0 is Low and S1 is High, data shifts left synchronously and new data is entered at the shift-left serial input (D_{SL}).

Clocking of the flip-flops is inhibited when both mode control inputs are Low.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F198	95MHz	73mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
24-pin Plastic Slim DIP (300mil)	N74F198N	SOT222-1
24-pin Plastic SOL	N74F198D	SOT137-1

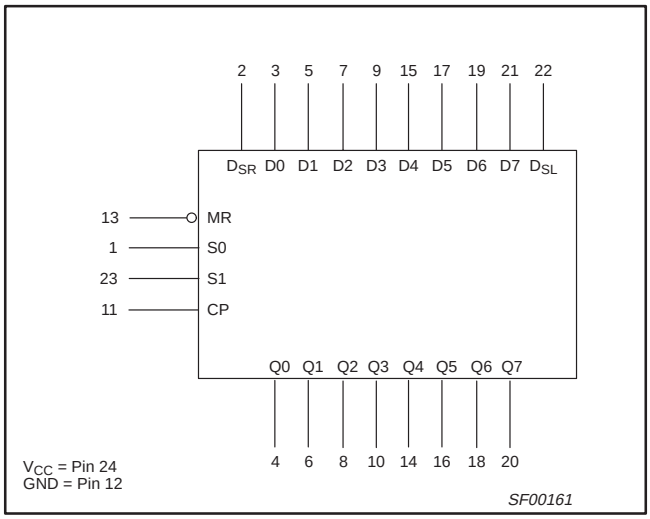
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0–D7	Parallel data inputs	1.0/1.0	20µA/0.6mA
D_{SR}	Serial data input (Shift Right)	1.0/1.0	20µA/0.6mA
D_{SL}	Serial data input (Shift Left)	1.0/1.0	20µA/0.6mA
S0–S1	Mode Select inputs	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (Active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (Active Low)	1.0/1.0	20µA/0.6mA
Q0–Q7	Data outputs	50/33	1.0mA/20mA

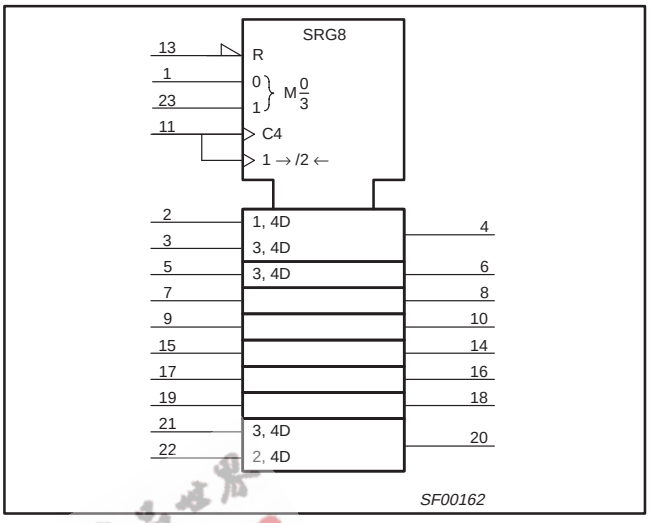
NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

8-bit bidirectional universal shift register 74F198

LOGIC SYMBOL



IEC/IEEE SYMBOL

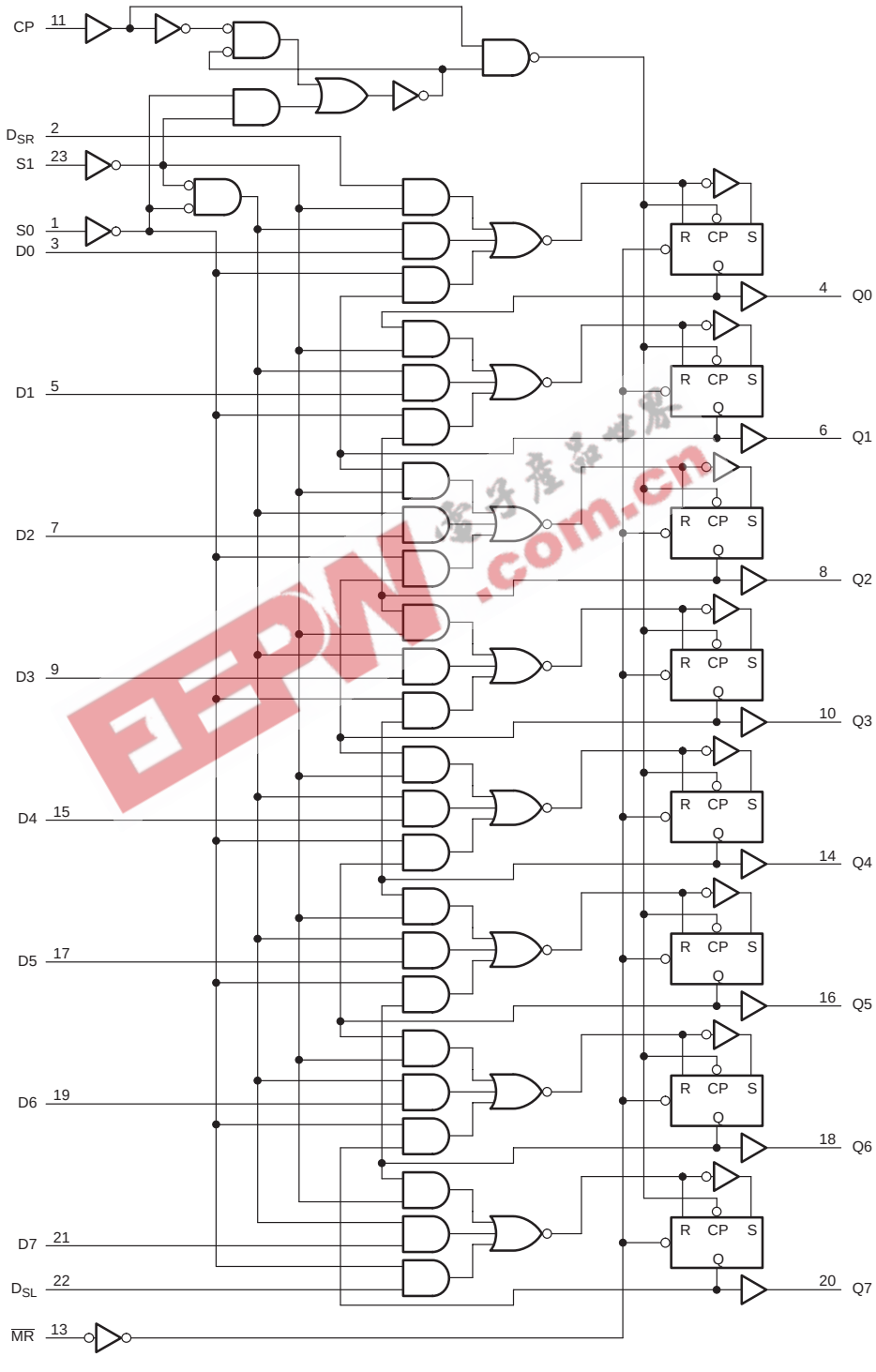


FUNCTION TABLE

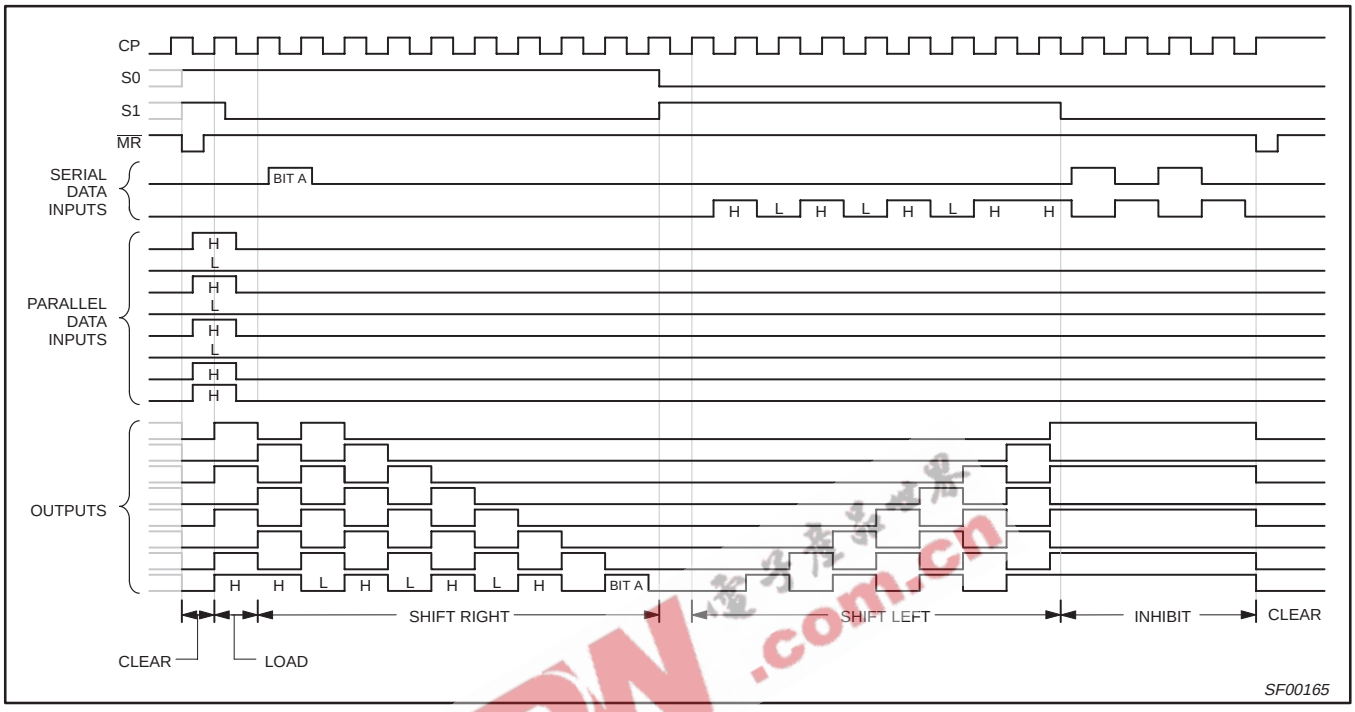
INPUTS							OUTPUTS				
$\overline{MR}$	MODE		CP	SERIAL		PARALLEL	Q0	Q1	…	Q6	Q7
	S0	S1		LEFT	RIGHT	0…7					
L	X	X	X	X	X	X	L	L		L	L
H	X	X	L	X	X	X	Q00	Q10		Q60	Q70
H	H	H	↑	X	X	0…7	0	1		6	7
H	H	L	↑	X	H	X	H	Q0n		Q5n	Q6n
H	H	L	↑	X	L	X	L	Q0n		Q5n	Q6n
H	L	H	↑	H	X	X	Q1n	Q2n		Q7n	H
H	L	H	↑	L	X	X	Q1n	Q2n		Q7n	L
H	L	L	X	X	X	X	Q00	Q10		Q60	Q70

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High transition of designated input
0…7 = The level of steady input at inputs 0 through 7, respectively.
Q00, Q10, Q60, Q70 = The level of Q0, Q1, Q6, Q7, respectively, before the indicated steady state input conditions were established.
Q0n, Q1n, Q6n, Q7n = The level of Q0, Q1, Q6, Q7, respectively, before the most recent Low-to-High clock transition.

LOGIC DIAGRAM



TYPCIAL TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			70	100	mA
		I_{CCL}				75	110	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

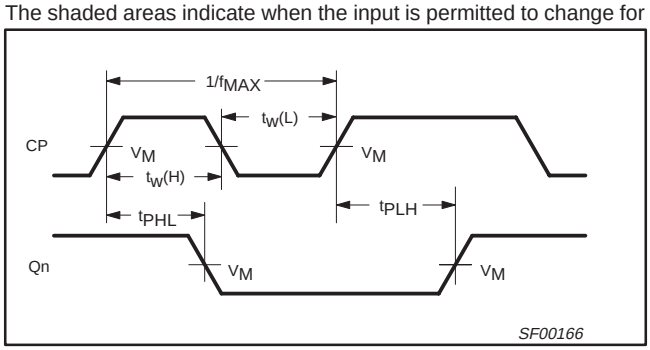
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	80	95		70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	Waveform 1	5.0 6.0	7.5 8.5	10.0 11.0	4.5 5.5	11.0 12.0	ns
t_{PHL}	Propagation delay	Waveform 3	5.0	7.5	10.0	4.5	11.0	ns

AC SETUP REQUIREMENTS

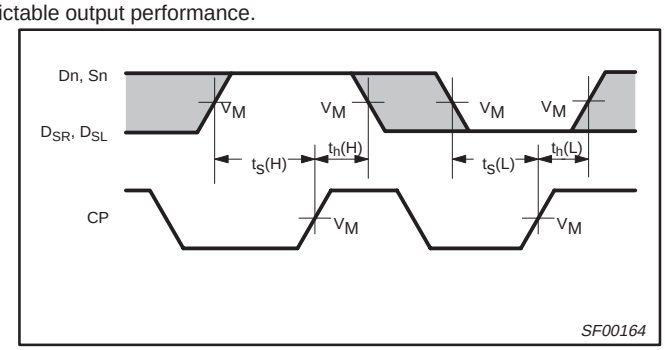
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V_{CC} = +5.0V T_{amb} = +25°C C_L = 50pF, R_L = 500Ω			V_{CC} = +5.0V ± 10% T_{amb} = 0°C to +70°C C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_S(H) t_S((L)	Setup time, High or Low Dn to CP	Waveform 2	0.0 3.0			0.0 3.0		ns
t_h(H) t_h(L)	Hold time, High or Low Dn to CP	Waveform 2	0.0 3.5			1.0 4.0		ns
t_S(H) t_S(L)	Setup time, High or Low D_{SR}, D_{SL} to CP	Waveform 2	0.0 3.0			0.0 3.0		ns
t_h(H) t_h(L)	Hold time, High or Low D_{SR}, D_{SL} to CP	Waveform 2	0.0 2.5			0.0 3.0		ns
t_S(H) t_S(L)	Setup time, High or Low Sn to CP	Waveform 2	9.0 6.0			10.0 7.0		ns
t_h(H) t_h(L)	Hold time, High or Low Sn to CP	Waveform 2	0.0 0.0			0.0 0.0		ns
t_w(H) t_w(L)	CP Pulse width, High or Low	Waveform 1	5.0 5.0			6.0 6.0		ns
t_w(L)	$\overline{MR}$ Pulse width, Low	Waveform 3	5.0			5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 3	5.0			6.0		ns

AC WAVEFORMS

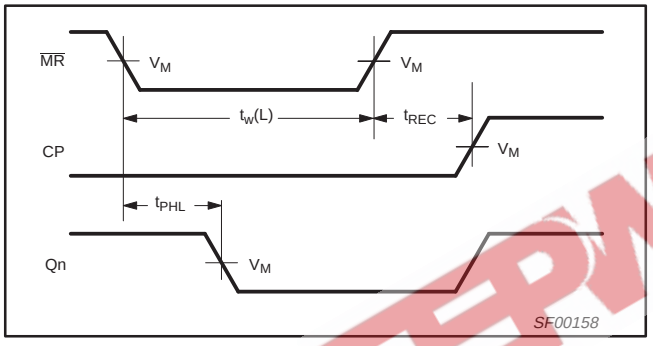
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation 'Delay, Clock Input to Output, Clock Widths, and Maximum Clock Frequency

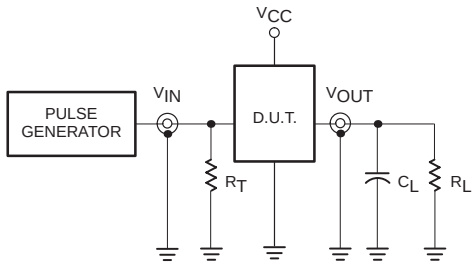


Waveform 2. Setup Time and Hold Time

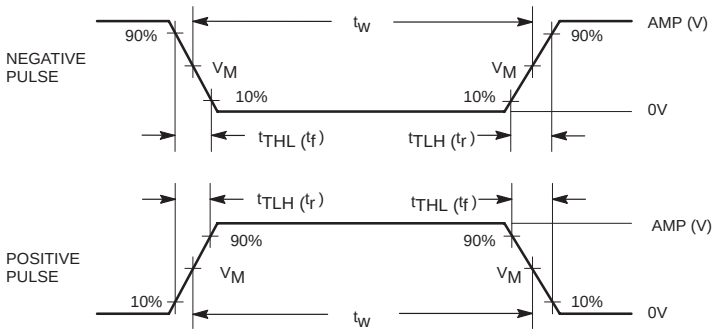


Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

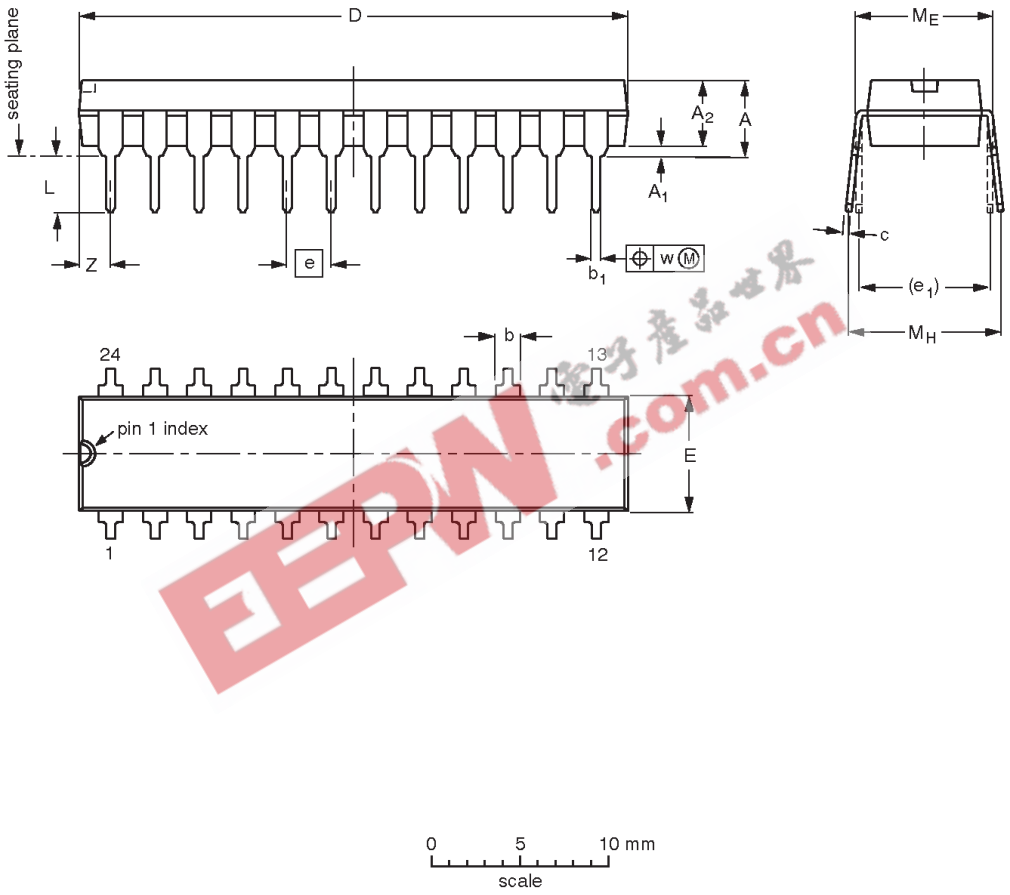
R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

DIP24: plastic dual in-line package; 24 leads (300 mil) SOT222-1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

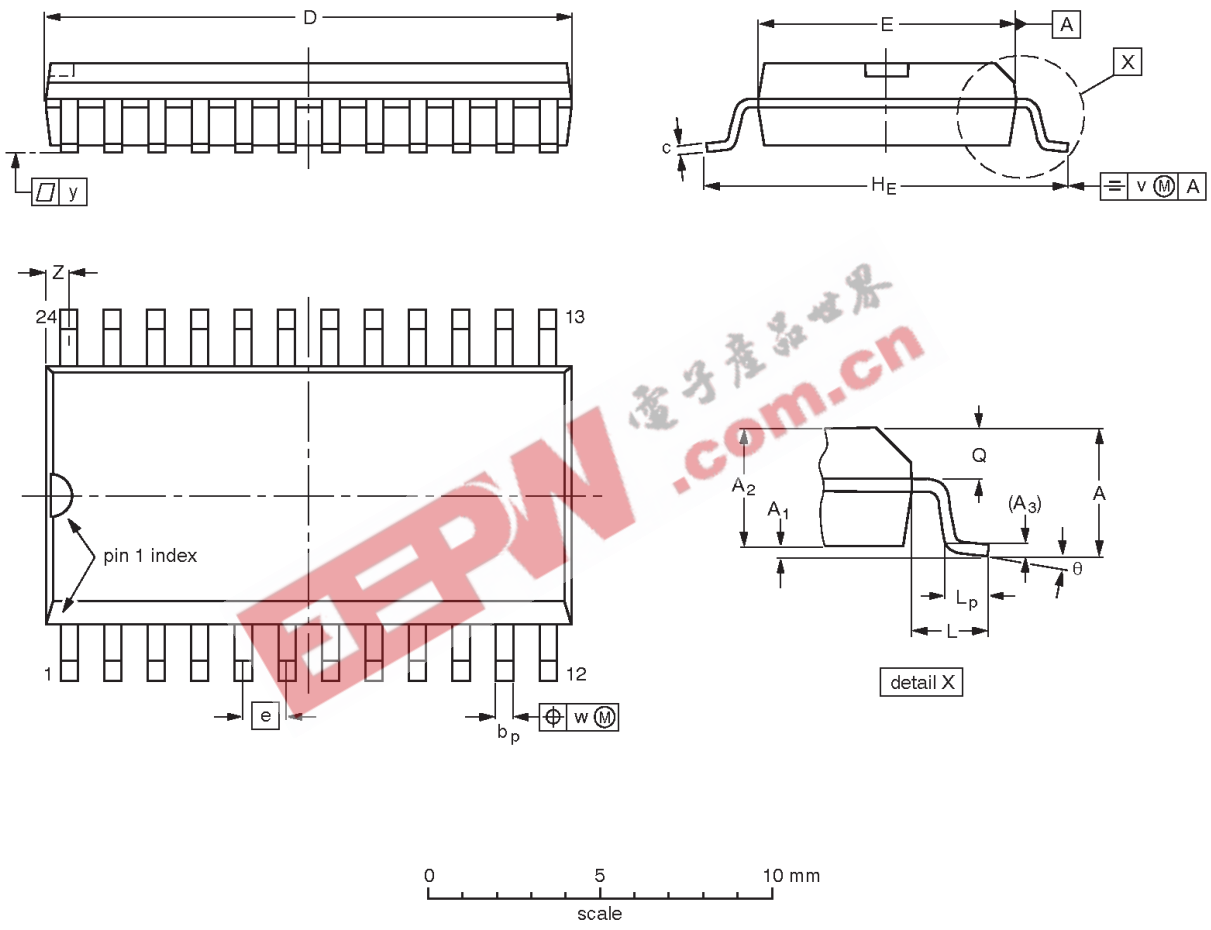
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

NOTES

8-bit bidirectional universal shift register 74F198

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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