FAIRCHILD SEMICONDUCTOR™

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74VHC595
8-Bit Shift Register with Output Latches

General Description

The VHC595 is an advanced high-speed CMOS Shift Register fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has eight 3-STATE outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive-edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register.

An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

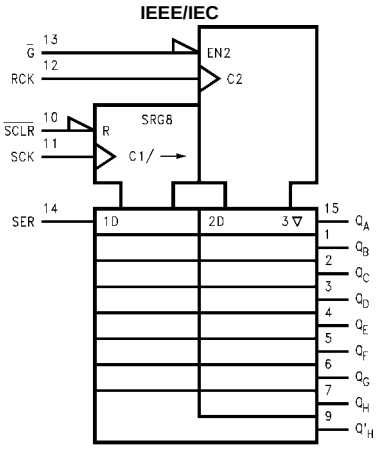
- High Speed: t_{PD} = 5.4 ns (typ) at V_{CC} = 5V
- Low power dissipation: I_{CC} = 4 μA (max) at T_A = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Power down protection is provided on all inputs
- Low noise: V_{OLP} = 0.9V (typ)
- Pin and function compatible with 74HC595

Ordering Code:

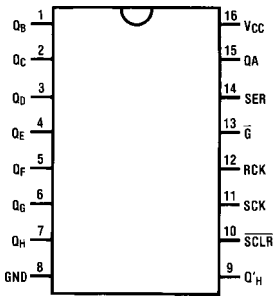
Order Number	Package Number	Package Description
74VHC595M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74VHC595SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC595MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC595N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



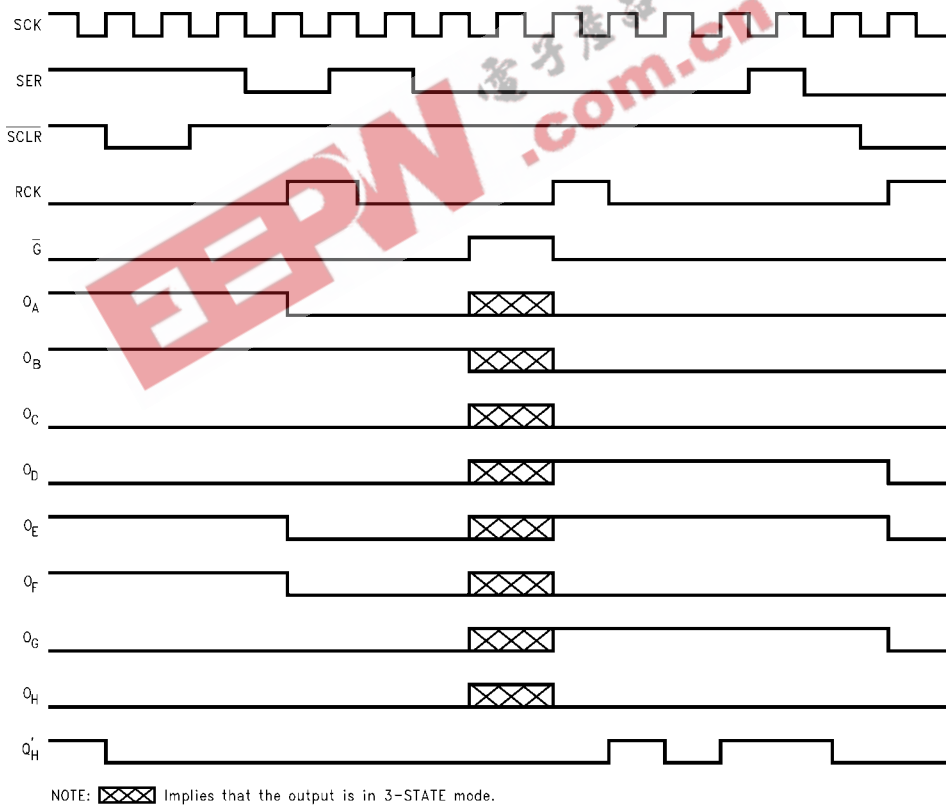
Pin Descriptions

Pin Names	Description
SER	Serial Data Input
SCK	Shift Register Clock Input (Active rising edge)
RCK	Storage Register Clock Input (Active rising edge)
$\overline{SCLR}$	Reset Input
$\overline{G}$	3-STATE Output Enable Input (Active LOW)
Q_A - Q_H	Parallel Data Outputs
Q'_H	Serial Data Output

Truth Table

Inputs					Function
SER	RCK	SCK	$\overline{SCLR}$	$\overline{G}$	
X	X	X	X	H	Q_A thru Q_H 3-STATE
X	X	X	X	L	Q_A thru Q_H outputs enabled
X	X	X	L	L	Shift Register cleared $Q'_H = 0$
L	X	↑	H	L	Shift Register clocked $Q_N = Q_{n-1}$, Q_0 = SER = L
H	X	↑	H	L	Shift Register clocked $Q_N = Q_{n-1}$, Q_0 = SER = H
X	↑	X	H	L	Contents of Shift Register transferred to output latches

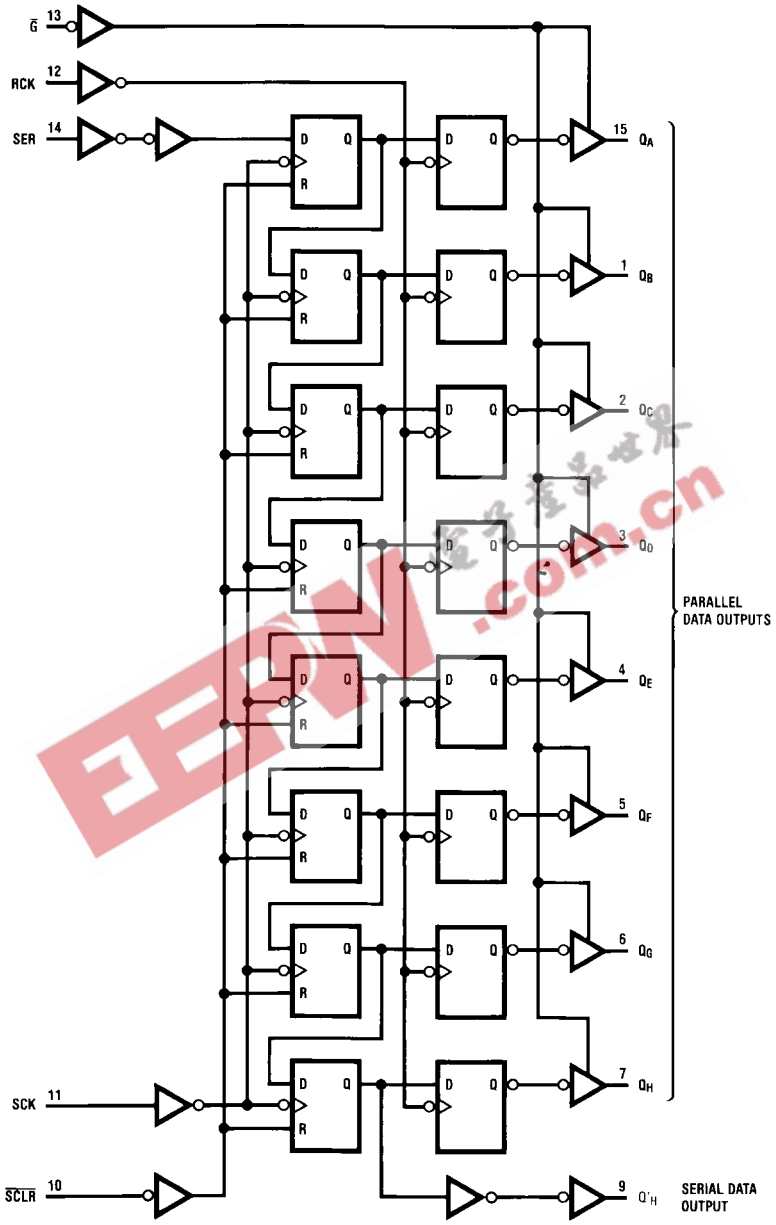
Timing Diagram



NOTE: ⊠ Implies that the output is in 3-STATE mode.

Logic Diagram

(positive logic)



Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC})	2.0V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ±0.3V	0 ~ 100 ns/V
V_{CC} = 5.0V ±0.5V	0 ~ 20 ns/V

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level Input Voltage	2.0	1.50			1.50		V		
		3.0 – 5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	LOW Level Input Voltage	2.0			0.50		0.50	V		
		3.0 – 5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	HIGH Level Output Voltage	2.0	1.9	2.0		1.9		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 µA
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		3.0	2.58			2.48		V		I_{OH} = −4 mA
		4.5	3.94			3.80				I_{OH} = −8 mA
V_{OL}	LOW Level Output Voltage	2.0		0.0	0.1		0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 µA
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44	V		I_{OL} = 4 mA
		4.5			0.36		0.44			I_{OL} = 8 mA
I_{OZ}	3-STATE Output Off-State Current	5.5			±0.25		±2.5	µA	V_{IN} = V_{CC} or GND; V_{OUT} = V_{CC} or GND; $V_{IN}\overline{G}$ = V_{IH} or V_{IL}	
I_{IN}	Input Leakage Current	0 – 5.5			±0.1		±1.0	µA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	µA	V_{IN} = V_{CC} or GND	

Noise Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = 25°C		Units	Conditions
			Typ	Limits		
V_{OLP} (Note 3)	Quiet Output Maximum Dynamic V_{OL}	5.0	0.9	1.2	V	C_L = 50 pF
V_{OLV} (Note 3)	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.9	−1.2	V	C_L = 50 pF
V_{IHD} (Note 3)	Minimum HIGH Level Dynamic Input Voltage	5.0		3.5	V	C_L = 50 pF
V_{ILD} (Note 3)	Maximum LOW Level Dynamic Input Voltage	5.0		1.5	V	C_L = 50 pF

Note 3: Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions	
			Min	Typ	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay Time RCK to Q_A–Q_H	3.3 ± 0.3		7.7	11.9	1.0	13.5	ns		C_L = 15 pF
				10.2	15.4	1.0	17.0			C_L = 50 pF
		5.0 ± 0.5		5.4	7.4	1.0	8.5	ns		C_L = 15 pF
				6.9	9.4	1.0	10.5			C_L = 50 pF
t_{PLH} t_{PHL}	Propagation Delay Time SCK–Q'H	3.3 ± 0.3		8.8	13.0	1.0	15.0	ns		C_L = 15 pF
				11.3	16.5	1.0	18.5			C_L = 50 pF
		5.0 ± 0.5		6.2	8.2	1.0	9.4	ns		C_L = 15 pF
				7.7	10.2	1.0	11.4			C_L = 50 pF
t_{PHL}	Propagation Delay Time $\overline{SCLR}$ –Q'H	3.3 ± 0.3		8.4	12.8	1.0	13.7	ns		C_L = 15 pF
				10.9	16.3	1.0	17.2			C_L = 50 pF
		5.0 ± 0.5		5.9	8.0	1.0	9.1	ns		C_L = 15 pF
				7.4	10.0	1.0	11.1			C_L = 50 pF
t_{PZL} t_{PZH}	Output Enable Time $\overline{G}$ to Q_A–Q_H	3.3 ± 0.3		7.5	11.5	1.0	13.5	ns	R_L = 1 kΩ	C_L = 15 pF
				9.0	15.0	1.0	17.0			C_L = 50 pF
		5.0 ± 0.5		4.8	8.6	1.0	10.0	ns		C_L = 15 pF
				8.3	10.6	1.0	12.0			C_L = 50 pF
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{G}$ to Q_A–Q_H	3.3 ± 0.3		12.1	15.7	1.0	16.2	ns	R_L = 1 kΩ	C_L = 50 pF
		5.0 ± 0.5		7.6	10.3	1.0	11.0			C_L = 50 pF
f_{MAX}	Maximum Clock Frequency	3.3 ± 0.3	80	150		70		MHz		C_L = 15 pF
			55	130		50				C_L = 50 pF
		5.0 ± 0.5	135	185		115		MHz		C_L = 15 pF
			95	155		85				C_L = 50 pF
t_{OSLH} t_{OSHL}	Output to Output Skew	3.3 ± 0.3			1.5		1.5	ns	(Note 4)	C_L = 50 pF
		5.0 ± 0.5			1.0		1.0			C_L = 50 pF
C_{IN}	Input Capacitance			5.0	10		10	pF	V_{CC} = Open	
C_{OUT}	Output Capacitance			6.0				pF	V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance			87				pF	(Note 5)	

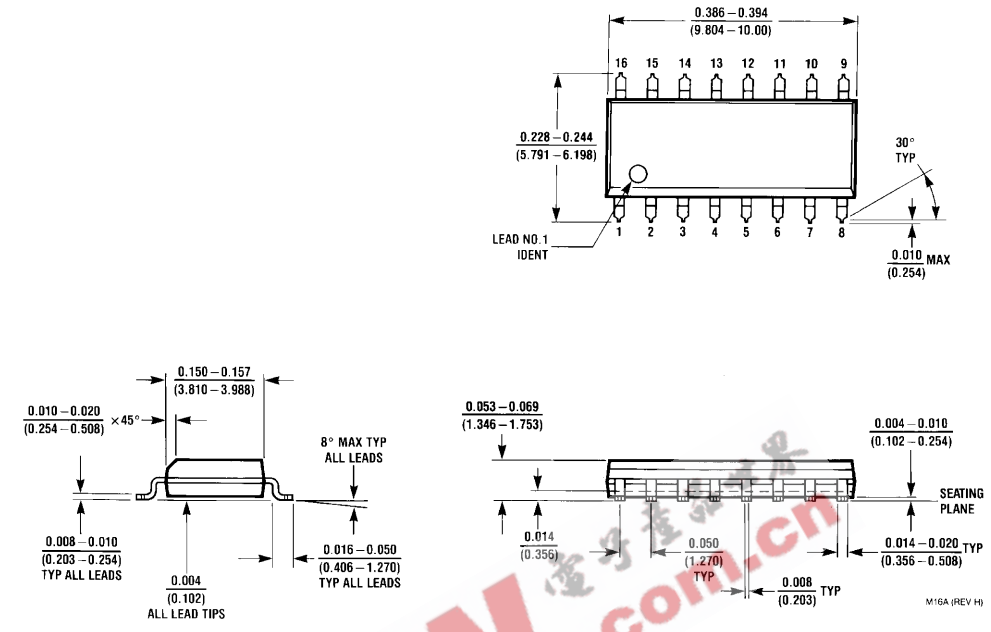
Note 4: Parameter guaranteed by design. $t_{OSLH} = |t_{PLH}$ max – t_{PLH} min|; $t_{OSHL} = |t_{PHL}$ max – t_{PHL} min|.

Note 5: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = C_{PD} * V_{CC} * f_{IN} + I_{CC}.

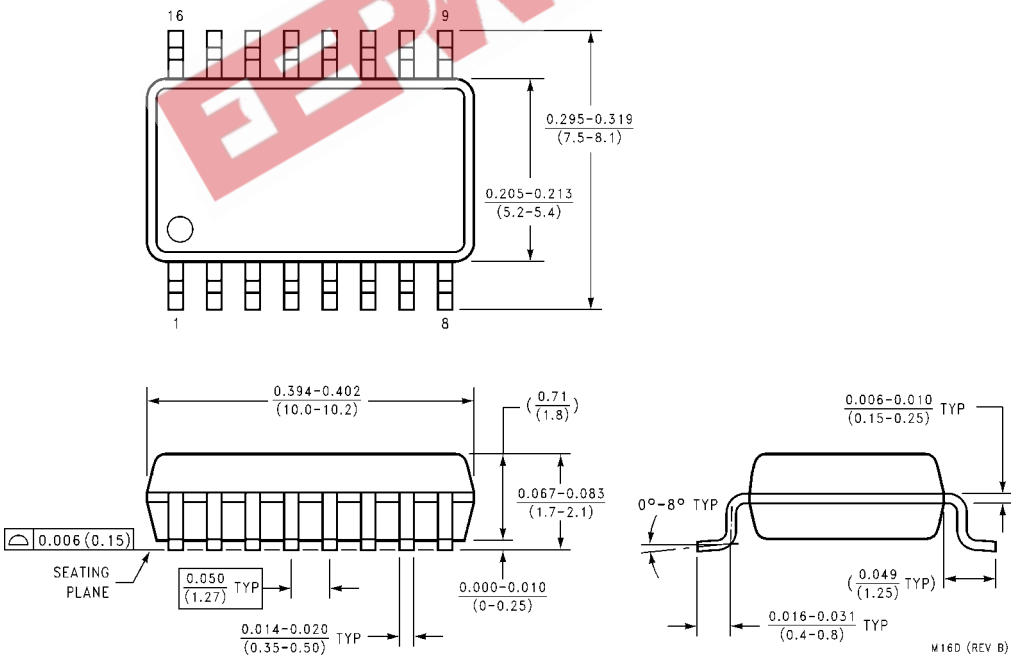
AC Operating Requirements

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$		$T_A = -40°C$ to $+85°C$	Units
			Typ	Guaranteed Minimum		
t_S	Minimum Setup Time	3.3 ± 0.3		3.5	3.5	ns
	(SER–SCK)	5.0 ± 0.5		3.0	3.0	
t_S	Minimum Setup Time	3.3 ± 0.3		8.0	8.5	ns
	(SCK–RCK)	5.0 ± 0.5		5.0	5.0	
t_S	Minimum Setup Time	3.3 ± 0.3		8.0	9.0	ns
	($\overline{SCLR}$ –RCK)	5.0 ± 0.5		5.0	5.0	
t_H	Minimum Hold Time	3.3 ± 0.3		1.5	1.5	ns
	(SER–SCK)	5.0 ± 0.5		2.0	2.0	
t_H	Minimum Hold Time	3.3 ± 0.3		0.0	0.0	ns
	(SCK–RCK)	5.0 ± 0.5		0.0	0.0	
t_H	Minimum Hold Time	3.3 ± 0.3		0.0	0.0	ns
	($\overline{SCLR}$ –RCK)	5.0 ± 0.5		0.0	0.0	
$t_{W(L)}$	Minimum Pulse Width	3.3 ± 0.3		5.0	5.0	ns
	($\overline{SCLR}$)	5.0 ± 0.5		5.0	5.0	
$t_{W(L)}$	Minimum Pulse Width	3.3 ± 0.3		5.0	5.0	ns
$t_{W(H)}$	(SCK)	5.0 ± 0.5		5.0	5.0	
$t_{W(L)}$	Minimum Pulse Width	3.3 ± 0.3		5.0	5.0	ns
$t_W(H)$	(RCK)	5.0 ± 0.5		5.0	5.0	
t_{rem}	Minimum Removal Time	3.3 ± 0.3		3.0	3.0	ns
	($\overline{SCLR}$ –SCK)	5.0 ± 0.5		2.5	2.5	

Physical Dimensions inches (millimeters) unless otherwise noted

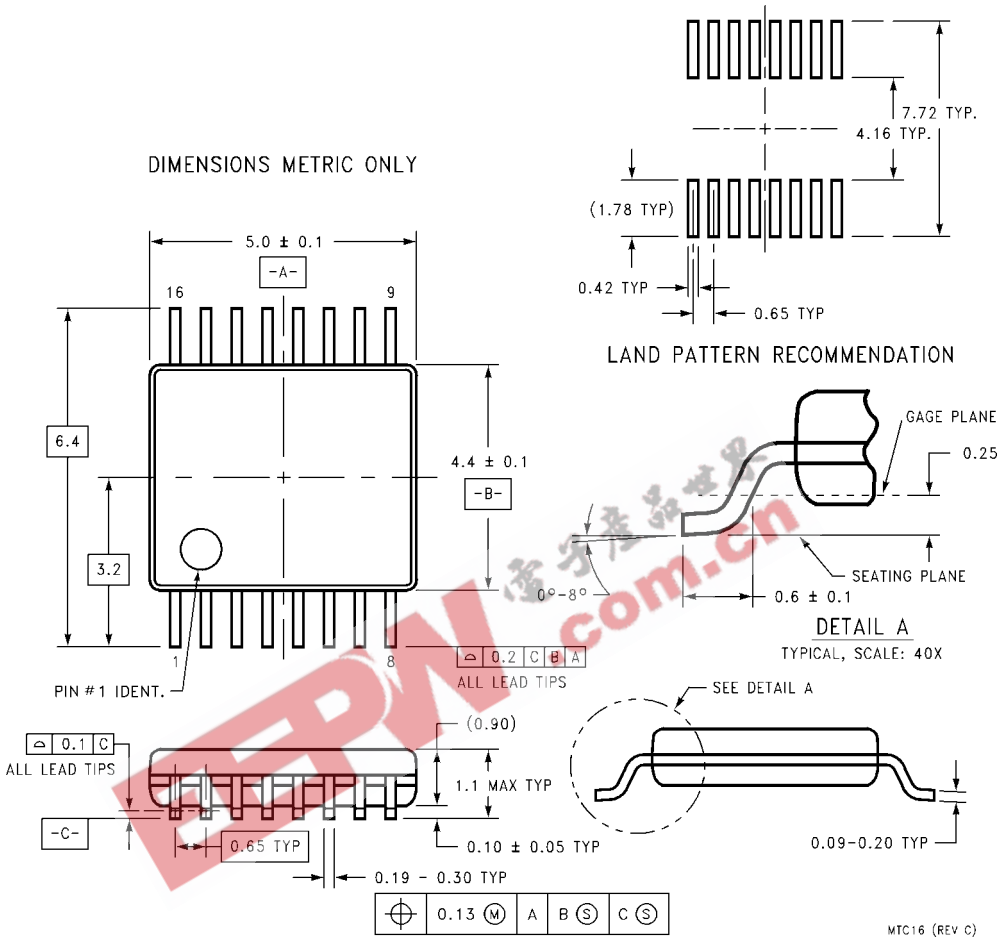


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A



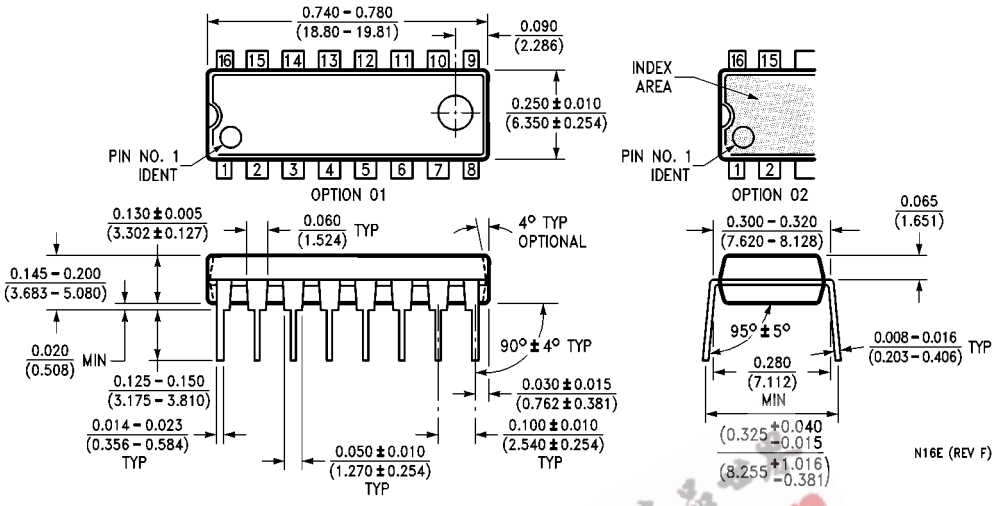
16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

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