

April 1988 Revised August 1999

74F5218-Bit Identity Comparator

General Description

The 74F521 is an expandable 8-bit comparator. It compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input $\overline{l}_{A=B}$ also serves as an active LOW enable input.

Features

- Compares two 8-bit words in 6.5 ns typ
- Expandable to any word length
- 20-pin package

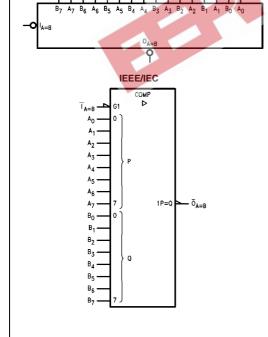
Ordering Code:

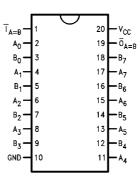
		4
Order Number	Package Number	Package Description
74F521SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F521SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F521MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74F521PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols

Connection Diagram





Unit Loading/Fan Out

Pin Names	December 1	U.L.	Input I _{IH} /I _{IL}	
	Description	HIGH/LOW	Output I _{OH} /I _{OL}	
A ₀ -A ₇	Word A Inputs	1.0/1.0	20 μA/-0.6 mA	
B ₀ -B ₇	Word B Inputs	1.0/1.0	20 μA/–0.6 mA	
$\bar{I}_{A=B}$	Expansion or Enable Input (Active LOW)	1.0/1.0	20 μA/-0.6 mA	
$\overline{O}_{A=B}$	Identity Output (Active LOW)	50/33.3	-1 mA/20 mA	

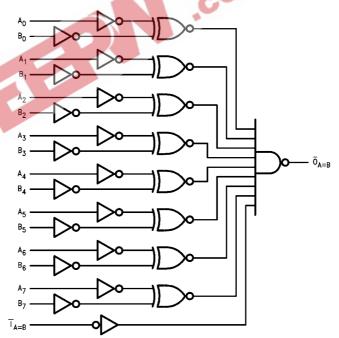
Truth Table

In	Output	
Ī _{A = B}	A, B	O _{A = B}
L	A = B (Note 1)	L
L	$A \neq B$	Н
Н	A = B (Note 1)	- H-
Н	$A \neq B$	3 35 H

H = HIGH Voltage Level L = LOW Voltage Level

Note 1: $A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 2)

Storage Temperature -65°C to +150°C

Ambient Temperature under Bias -55°C to +125°C Junction Temperature under Bias -55°C to +150°C V_{CC} Pin Potential to Ground Pin -0.5V to +7.0V Input Voltage (Note 3) -0.5V to +7.0V Input Current (Note 3) -30 mA to +5.0 mA

Voltage Applied to Output

in HIGH State (with V_{CC} = 0V)

Standard Output –0.5V to $V_{\mbox{\footnotesize CC}}$ 3-STATE Output -0.5V to +5.5V

Current Applied to Output

twice the rated I_{OL} (mA) in LOW State (Max)

Recommended Operating Conditions

Free Air Ambient Temperature 0°C to +70°C Supply Voltage +4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

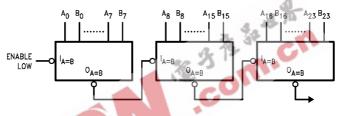
Symbol	Parameter	Min	Тур	Max	Units	Vcc	Conditions
V _{IH}	Input HIGH Voltage	2.0			V	18. M	Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V	p .	Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH 10% V _{CC}	2.5		20 1	V	Min	l _{OH} = −1 mA
	Voltage 5% V _{CC}	2.7		132			$I_{OH} = -1 \text{ mA}$
V _{OL}	Output LOW 10% V _{CC}			0.5	V	Min	I _{OL} = 20 mA
	Voltage						
I _{IH}	Input HIGH Current	1		5.0	μА	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current			7.0	μА	Max	V _{IN} = 7.0V
	Breakdown Test			7.0	μА	IVIAX	V _{IN} = 7.0V
I _{CEX} Output	Output HIGH			50	μА	Max	V -V
	Leakage Current						$V_{OUT} = V_{CC}$
V _{ID}	Input Leakage	4.75			V	0.0	$I_{ID} = 1.9 \mu A$
	4.75		V	0.0	All Other Pins Grounded		
I _{OD}	Output Leakage			3.75		0.0	V _{IOD} = 150 mV
	Circuit Current	Current		3.73	μΑ	0.0	All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6	mA	Max	$V_{IN} = 0.5V$
Ios	Output Short-Circuit Current	-60		-150	mA	Max	V _{OUT} = 0V
I _{CCH}	Power Supply Current		21	32	mA	Max	V _O = HIGH

AC Electrical Characteristics

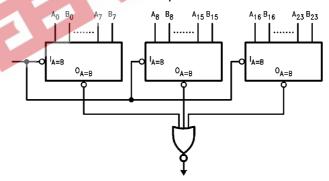
	Parameter	$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$			$T_{A} = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = +5.0V$ $C_{L} = 50 \text{ pF}$		$T_A = 0^{\circ}C \text{ to } +70^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$		Units
Symbol									
		Min	Тур	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	3.0	7.0	10.0	3.0	14.0	3.0	11.0	ns
t _{PHL}	A_n or B_n to $\overline{O}_{A=B}$	4.5	7.0	10.0	4.0	15.0	4.0	11.0	
t _{PLH}	Propagation Delay	3.0	5.0	6.5	3.0	8.5	3.0	7.5	ns
t _{PHL}	$\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	3.5	6.5	9.0	3.5	13.5	3.5	10.0	IIS

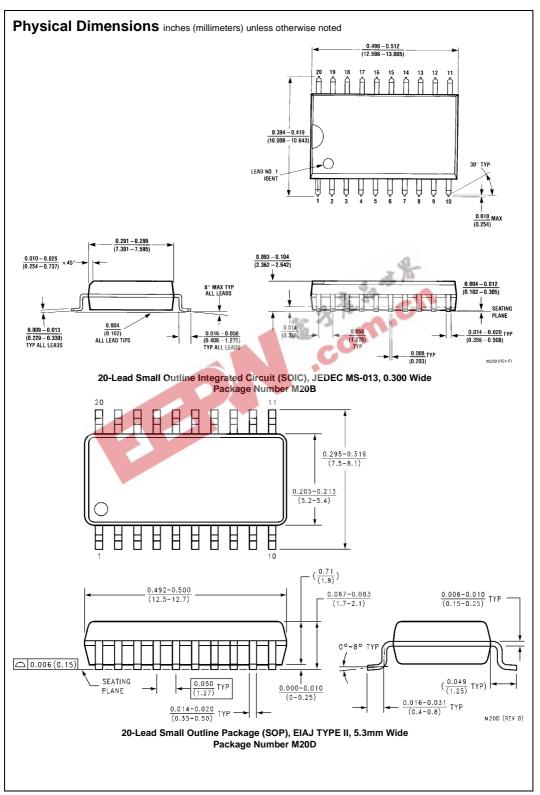
Applications

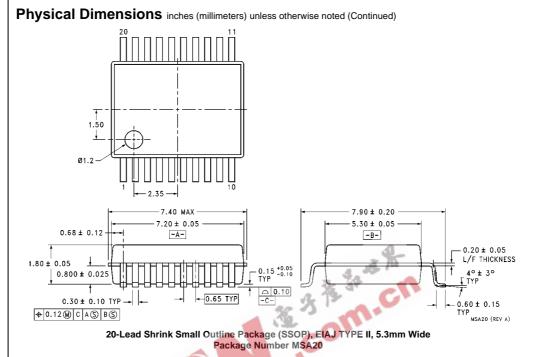
Ripple Expansion

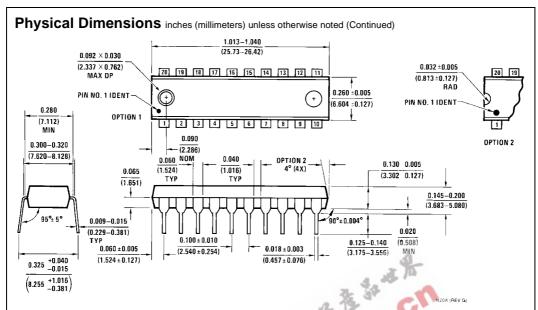


Parallel Expansion









20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N20A

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