

54/7476
54H/74H76
54LS/74LS76

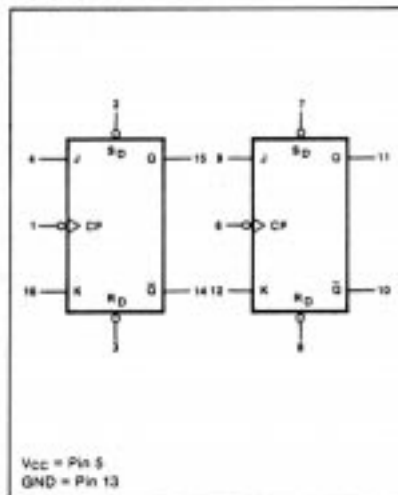
DESCRIPTION

The "76" is a Dual JK Flip-Flop with individual J, K, Clock, Set and Reset inputs. The 7476 and 74H76 are positive pulse triggered flip-flops. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW Clock transition. The J and K inputs must be stable while the Clock is HIGH for conventional operation.

The 74LS76 is a negative edge triggered flip-flop. The J and K inputs must be stable only one setup time prior to the HIGH-to-LOW Clock transition.

The Set (\bar{S}_D) and Reset (\bar{R}_D) are asynchronous active LOW inputs. When LOW, they override the Clock and data inputs forcing the outputs to the steady state levels as shown in the Truth Table.

LOGIC SYMBOL



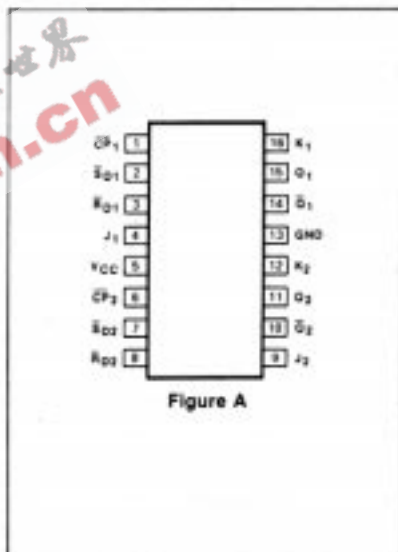
ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	Fig A Fig A	N7476N • N74H76N N74LS76N	
Ceramic DIP	Fig A Fig A	N7476F • N74H76F N74LS76F	S5476F • S54H76F S54LS76F
Flatpak	Fig A Fig A		S5476W • S54H76W S54LS76W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
$\bar{C}P$ Clock input	I_H (μA)	80	50		80
	I_L (mA)	-3.2	-2.0		-0.8
\bar{R}_D Reset input	I_H (μA)	80	100		80
	I_L (mA)	-3.2	-4.0		-0.8
\bar{S}_D Set input	I_H (μA)	80	100		80
	I_L (mA)	-3.2	-4.0		-0.8
JK Data inputs	I_H (μA)	40	50		20
	I_L (mA)	-1.6	-2.0		-0.4
Q & \bar{Q} Outputs	I_{OH} (μA)	-400	-500		-400
	I_{OL} (mA)	16	20		4/8 ^(a)

PIN CONFIGURATION



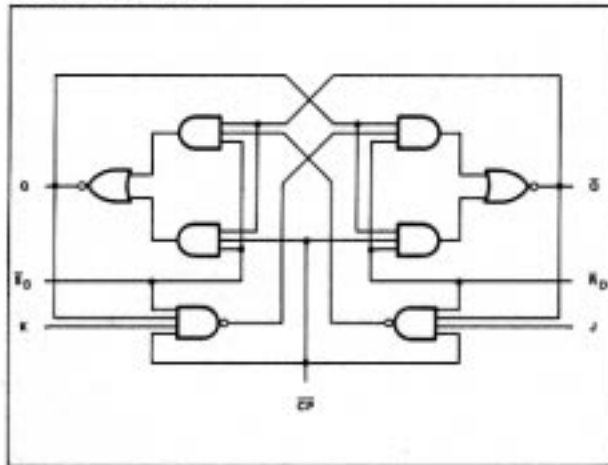
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
I_{CC} Supply current	$V_{CC} = \text{Max}$, $V_{CP} = 0V$		40		50				8.0	mA

NOTES

- The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.
- For family dc characteristics, see inside front cover for 54/74 and 54H/74H and see inside back cover for 54S/74S and 54LS/74LS specification.

LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS		
	\bar{S}_D	\bar{R}_D	\bar{CP} (d)	J	K	Q	\bar{Q}
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (c)	L	L	X	X	X	H	H
Toggle	H	H	\downarrow	h	h	\bar{q}	q
Load "0" (Reset)	H	H	\downarrow	l	h	L	H
Load "1" (Set)	H	H	\downarrow	h	l	H	L
Hold "no change"	H	H	\downarrow	l	l	q	\bar{q}

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.^(d)
 l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.^(d)
 X = Don't care.
 q = Lower case letters indicate the state of the referenced output prior to the HIGH to LOW Clock transition.
 \downarrow = Positive Clock pulse.

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		$C_L = 15\text{ pF}$ $R_L = 400\ \Omega$		$C_L = 25\text{ pF}$ $R_L = 280\ \Omega$				$C_L = 15\text{ pF}$ $R_L = 2\text{ k}\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	15		25				30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to Output	25 40		21 27				20 30		ns
t_{PLH} t_{PHL}	Propagation delay \bar{S}_D or \bar{R}_D to Output	25 40		13 24				20 30		ns

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$ (See Section 4 for Waveforms and Conditions)

PARAMETER	TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{w(H)}$	Clock pulse width (HIGH)	20		12				20		ns
$t_{w(L)}$	Clock pulse width (LOW)	47		28				13		ns
$t_{w(L)}$	Set or Reset pulse width (LOW)	25		16				25		ns
t_s	Setup time J or K to Clock	(e)		(e)				20		ns
t_h	Hold time J or K to Clock	0		0				0		ns

NOTES

- c. Both outputs will be HIGH while both \bar{S}_D and \bar{R}_D are LOW, but the output states are unpredictable if \bar{S}_D and \bar{R}_D go HIGH simultaneously.
- d. The 74LS76 is edge triggered. Data must be stable one setup time prior to the negative edge of the Clock for predictable operation.
- e. The J and K inputs of the 7476 and 74H76 must be stable while the Clock is HIGH for conventional operation.