

**Features**

- FCT-E speed at 3.2 ns
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Industrial temperature range of -40°C to +85°C
- V<sub>CC</sub> = 5V ± 10%

*CY74FCT16245T Features:*

- 64 mA sink current, 32 mA source current
- Typical V<sub>OLP</sub> (ground bounce) < 1.0V at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C

*CY74FCT162245T Features:*

- Balanced output drivers: 24 mA
- Reduced system switching noise
- Typical V<sub>OLP</sub> (ground bounce) < 0.6V at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C

*CY74FCT162H245T Features:*

- Bus hold on data inputs
- Eliminates the need for external pull-up or pull-down resistors

**Functional Description**

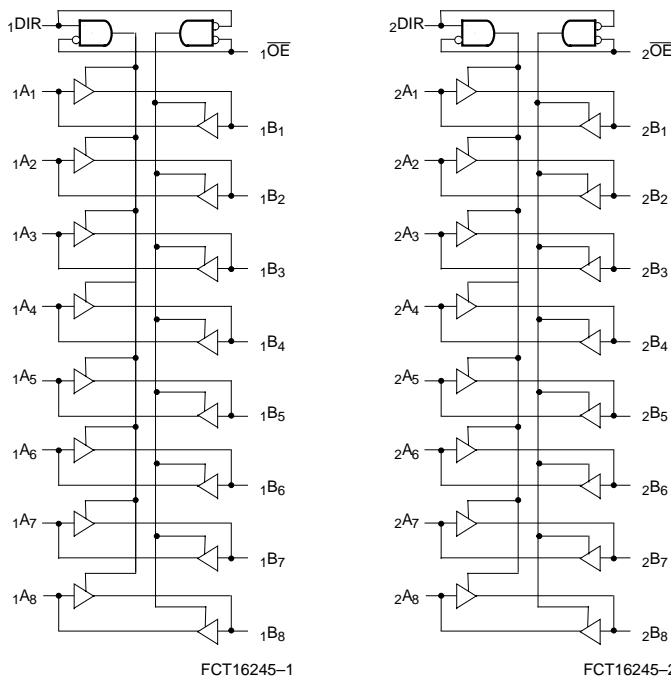
These 16-bit transceivers are designed for use in bidirectional synchronous communication between two buses, where high speed and low power are required. With the exception of the CY74FCT16245T, these devices can be operated either as two independent octals or a single 16-bit transceiver. Direction of data flow is controlled by (DIR), the Output Enable (OE) transfers data when LOW and isolates the buses when HIGH. The output buffers are designed with power off disable capability to allow for live insertion of boards.

The CY74FCT16245T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

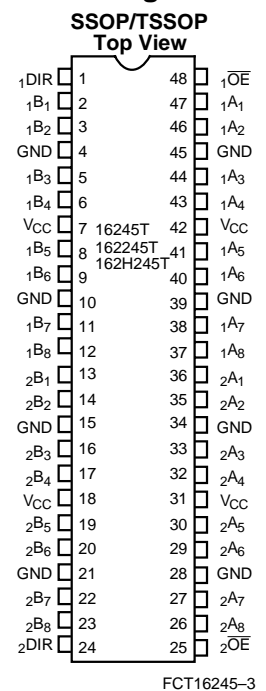
The CY74FCT162245T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162245T is ideal for driving transmission lines.

The CY74FCT162H245T is a 24-mA balanced output part that has bus hold on the data inputs. The device retains the input's last state whenever the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.

**Logic Block Diagrams CY74FCT16245T, CY74FCT162245T, CY74FCT162H245T**



**Pin Configuration**



**Pin Description**

Name	Description
OE	Three-State Output Enable Inputs (Active LOW)
DIR	Direction Control
A	Inputs or Three-State Outputs <sup>[1]</sup>
B	Inputs or Three-State Outputs <sup>[1]</sup>

**Function Table<sup>[2]</sup>**

Inputs		Outputs
OE	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

**Maximum Ratings<sup>[3, 4]</sup>**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... Com'l -55°C to +125°C

Ambient Temperature with Power Applied..... Com'l -55°C to +125°C

DC Input Voltage ..... -0.5V to +7.0V

DC Output Voltage..... -0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... -60 to +120 mA

Power Dissipation ..... 1.0W

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40°C to +85°C	5V ± 10%

**Notes:**

1. On CY74FCT162H245T these pins have bus hold.
2. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = High Impedance.
3. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.

**Electrical Characteristics Over the Operating Range**

Parameter	Description	Test Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage		2.0			V
V <sub>IL</sub>	Input LOW Voltage				0.8	V
V <sub>H</sub>	Input Hysteresis <sup>[6]</sup>			100		mV
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> =Min., I <sub>IN</sub> =-18 mA		-0.7	-1.2	V
I <sub>IH</sub>	Input HIGH Current	Standard	V <sub>CC</sub> =Max., V <sub>I</sub> =V <sub>CC</sub>		±1	µA
		Bus Hold			±100	
I <sub>IL</sub>	Input LOW Current	Standard	V <sub>CC</sub> =Max., V <sub>I</sub> =GND		±1	µA
		Bus Hold			±100	µA
I <sub>BBH</sub> I <sub>BBL</sub>	Bus Hold Sustain Current on Bus Hold Input <sup>[7]</sup>	V <sub>CC</sub> =Min., V <sub>I</sub> =2.0V	-50			µA
			V <sub>I</sub> =0.8V	+50		
I <sub>BHHO</sub> I <sub>BHLO</sub>	Bus Hold Overdrive Current on Bus Hold Input <sup>[7]</sup>	V <sub>CC</sub> =Max., V <sub>I</sub> =1.5V			TBD	mA
I <sub>OZH</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.7V			±1	µA
I <sub>OZL</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> =Max., V <sub>OUT</sub> =0.5V			±1	µA
I <sub>OS</sub>	Short Circuit Current <sup>[8]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =GND	-80	-140	-200	mA
I <sub>O</sub>	Output Drive Current <sup>[8]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.5V	-50		-180	mA
I <sub>OFF</sub>	Power-Off Disable	V <sub>CC</sub> =0V, V <sub>OUT</sub> ≤4.5V <sup>[9]</sup>			±1	µA

**Output Drive Characteristics for CY74FCT16245T**

Parameter	Description	Test Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-3 mA	2.5	3.5		V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-15 mA	2.4	3.5		V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-32 mA	2.0	3.0		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =64 mA		0.2	0.55	V

**Output Drive Characteristics for CY74FCT162245T, CY74FCT162H245T**

Parameter	Description	Test Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit
I <sub>ODL</sub>	Output LOW Current <sup>[8]</sup>	V <sub>CC</sub> =5V, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> =1.5V	60	115	150	mA
I <sub>ODH</sub>	Output HIGH Current <sup>[8]</sup>	V <sub>CC</sub> =5V, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> =1.5V	-60	-115	-150	mA
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-24 mA	2.4	3.3		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =24 mA		0.3	0.55	V

**Notes:**

5. Typical values are at V<sub>CC</sub>=5.0V, T<sub>A</sub>=+25°C ambient.
6. This parameter is specified but not tested.
7. Pins with bus hold are described in Pin Description.
8. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.
9. Tested at +25°C.

**Capacitance<sup>[6]</sup> (T<sub>A</sub> = +25°C, f = 1.0 MHz)**

Parameter	Description	Test Conditions	Typ. <sup>[5]</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6.0	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	5.5	8.0	pF

**Power Supply Characteristics**

Parameter	Description	Test Conditions		Typ. <sup>[5]</sup>	Max.	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC}=\text{Max.}$	$V_{IN}\leq 0.2V,$ $V_{IN}\geq V_{CC}-0.2V$	5	500	$\mu\text{A}$
$\Delta I_{CC}$	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC}=\text{Max.}$	$V_{IN}=3.4V^{[10]}$	0.5	1.5	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>[11]</sup>	$V_{CC}=\text{Max.}$ , One Input Toggling, 50% Duty Cycle, Outputs Open, $\text{OE}=\text{DIR}=\text{GND}$	$V_{IN}=V_{CC}$ or $V_{IN}=\text{GND}$	60	100	$\mu\text{A}/\text{MHz}$
$I_C$	Total Power Supply Current <sup>[12]</sup>	$V_{CC}=\text{Max.}$ , $f_1=10\text{ MHz}$ , 50% Duty Cycle, Outputs Open, One Bit Toggling, $\text{OE}=\text{DIR}=\text{GND}$	$V_{IN}=V_{CC}$ or $V_{IN}=\text{GND}$	0.6	1.5	mA
			$V_{IN}=3.4V$ or $V_{IN}=\text{GND}$	0.9	2.3	mA
		$V_{CC}=\text{Max.}$ , $f_1=2.5\text{ MHz}$ , 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\text{OE}=\text{DIR}=\text{GND}$	$V_{IN}=V_{CC}$ or $V_{IN}=\text{GND}$	2.4	4.5 <sup>[13]</sup>	mA
			$V_{IN}=3.4V$ or $V_{IN}=\text{GND}$	6.4	16.5 <sup>[13]</sup>	mA

**Notes:**

10. Per TTL driven input ( $V_{IN}=3.4V$ ); all other inputs at  $V_{CC}$  or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12.  $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$   
 $I_{CC}$  = Quiescent Current with CMOS input levels  
 $\Delta I_{CC}$  = Power Supply Current for a TTL HIGH input ( $V_{IN}=3.4V$ )  
 $D_H$  = Duty Cycle for TTL inputs HIGH  
 $N_T$  = Number of TTL inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current caused by an input transition pair (HLH or LHL)  
 $f_0$  = Clock frequency for registered devices, otherwise zero  
 $f_1$  = Input signal frequency  
 $N_1$  = Number of inputs changing at  $f_1$   
 All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are specified but not tested.

**Switching Characteristics** Over the Operating Range<sup>[14]</sup>

Parameter	Description	74FCT16245T 74FCT162245T		74FCT16245AT 74FCT162245AT 74FCT162H245AT		Unit	Fig. No. <sup>[15]</sup>
		Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Data to Output A to B, B to A	1.5	7.0	1.5	4.5	ns	1, 3
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time OE to A or B	1.5	9.5	1.5	6.2	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OE to A or B	1.5	7.5	1.5	5.0	ns	1, 7, 8
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time DIR to A or B	1.5	9.5	1.5	6.2	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time DIR to A or B	1.5	7.5	1.5	5.0	ns	1, 7, 8
t <sub>SK(O)</sub>	Output Skew <sup>[16]</sup>		0.5		0.5	ns	—

Parameter	Description	74FCT16245CT 74FCT162245CT 74FCT162H245CT		74FCT16245ET 74FCT162245ET 74FCT162H245ET		Unit	Fig. No. <sup>[15]</sup>
		Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Data to Output A to B, B to A	1.5	4.1	1.5	3.2	ns	1, 3
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time OE to A or B	1.5	5.8	1.5	4.4	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OE to A or B	1.5	4.8	1.5	4.0	ns	1, 7, 8
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time DIR to A or B	1.5	5.8	1.5	4.8	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time DIR to A or B	1.5	4.8	1.5	4.0	ns	1, 7, 8
t <sub>SK(O)</sub>	Output Skew <sup>[16]</sup>		0.5		0.5	ns	—

**Note:**

14. Minimum limits are specified but not tested on Propagation Delays.

15. See "Parameter Measurement Information" in the General Information section.

16. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

**Ordering Information CY74FCT16245**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.2	CY74FCT16245ETPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16245ETPVC/PVCT	O48	48-Lead (300-Mil) SSOP	
4.1	CY74FCT16245CTPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16245CTPVC/PVCT	O48	48-Lead (300-Mil) SSOP	
4.5	CY74FCT16245ATPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16245ATPVC/PVCT	O48	48-Lead (300-Mil) SSOP	
7.0	CY74FCT16245TPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16245TPVC/PVCT	O48	48-Lead (300-Mil) SSOP	

**Ordering Information CY74FCT162245**

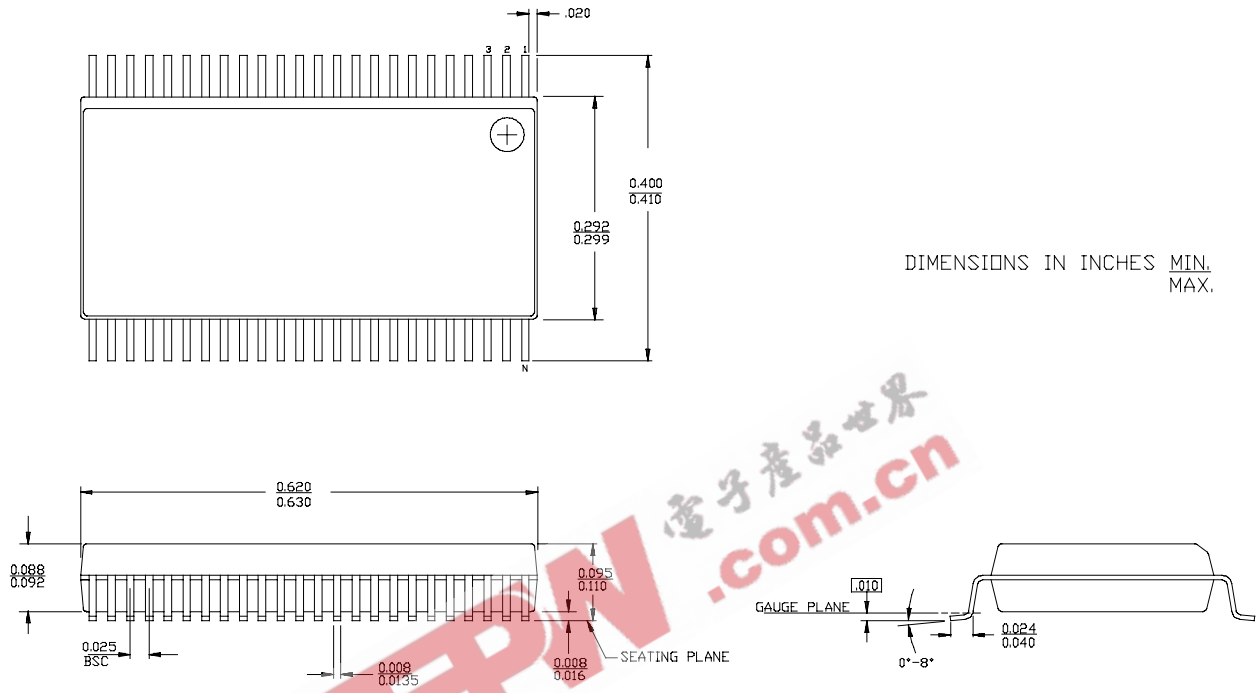
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.2	74FCT162245ETPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162245ETPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162245ETPVCT	O48	48-Lead (300-Mil) SSOP	
4.1	CY74FCT162245CTPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162245CTPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162245CTPVCT	O48	48-Lead (300-Mil) SSOP	
4.5	74FCT162245ATPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162245ATPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162245ATPVCT	O48	48-Lead (300-Mil) SSOP	
7.0	CY74FCT162245TPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162245TPVC/PVCT	O48	48-Lead (300-Mil) SSOP	

**Ordering Information CY74FCT162H245**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.2	74FCT162H245ETPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162H245ETPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162H245ETPVCT	O48	48-Lead (300-Mil) SSOP	
4.1	74FCT162H245CTPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162H245CTPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162H245CTPVCT	O48	48-Lead (300-Mil) SSOP	
4.5	74FCT162H245ATPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162H245ATPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162H245ATPVCT	O48	48-Lead (300-Mil) SSOP	

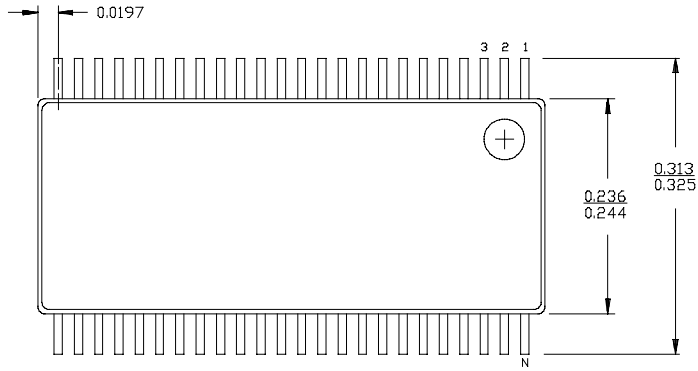
**Package Diagrams**

**48-Lead Shrunken Small Outline Package O48**

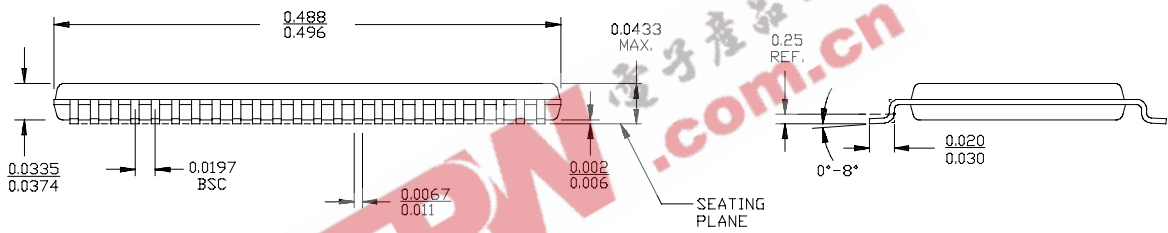


**Package Diagrams**

**48-Lead Thin Shrunken Small Outline Package Z48**



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