

54F/74F175 Quad D Flip-Flop

General Description

The 'F175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, LOW.

Features

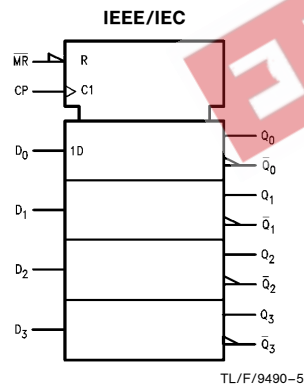
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Asynchronous common reset
- True and complement output
- Guaranteed 4000V minimum ESD protection

Commercial	Military	Package Number	Package Description
74F175PC		N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
	54F175DM (Note 2)	J16A	16-Lead Ceramic Dual-In-Line
74F175SC (Note 1)		M16A	16-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F175SJ (Note 1)		M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F175FM (Note 2)	W16A	16-Lead Cerpack
	54F175LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

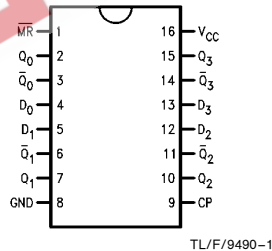
Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMOB and LMQB.

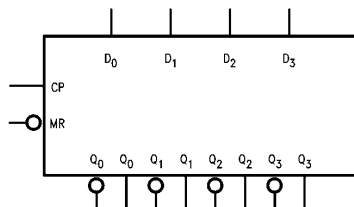
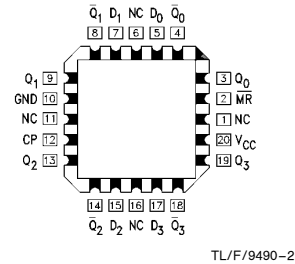
Logic Symbols



Pin Assignment for DIP, SOIC and Flatpak



Pin Assignment for LCC



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Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0-D_3	Data Inputs	1.0/1.0	20 μ A/ -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μ A/ -0.6 mA
\overline{MR}	Master Reset Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
Q_0-Q_3	True Outputs	50/33.3	-1 mA/20 mA
$\overline{Q}_0-\overline{Q}_3$	Complement Outputs	50/33.3	-1 mA/20 mA

Functional Description

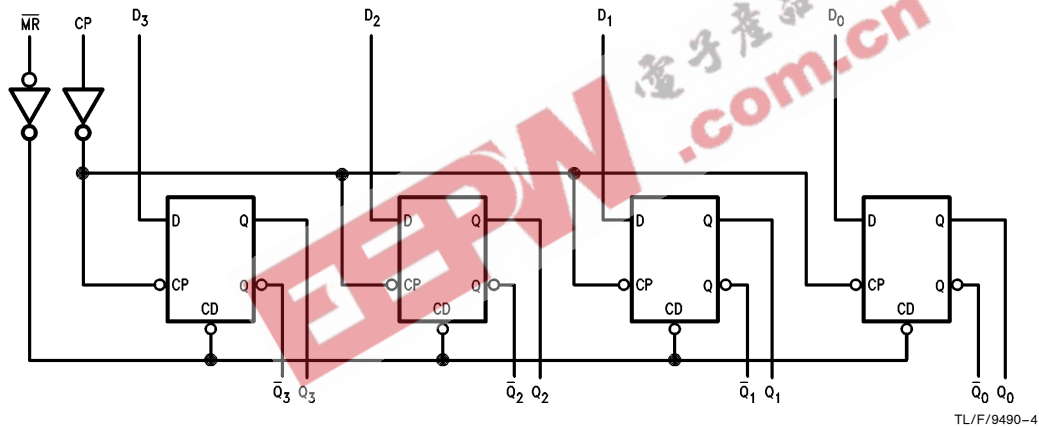
The 'F175 consists of four edge-triggered D flip-flops with individual D inputs and Q and \overline{Q} outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and \overline{Q} outputs to follow. A LOW input on the Master Reset (\overline{MR}) will force all Q outputs LOW and \overline{Q} outputs HIGH independent of Clock or Data inputs. The 'F175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

Truth Table

Inputs			Outputs	
\overline{MR}	CP	D_n	Q_n	\overline{Q}_n
L	X	X	L	H
H	\nearrow	H	H	L
H	\nearrow	L	L	H

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 \nearrow = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
TRI-STATE® Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)


Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC}	2.5		V	Min	I _{OH} = -1 mA I _{OH} = -1 mA I _{OH} = -1 mA
		74F 10% V _{CC}	2.5				
		74F 5% V _{CC}	2.7				
V _{OL}	Output LOW Voltage	54F 10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA I _{OL} = 20 mA
		74F 10% V _{CC}		0.5			
I _{IH}	Input HIGH Current	54F		20.0	μA	Max	V _{IN} = 2.7V
		74F		5.0			
I _{BVI}	Input HIGH Current Breakdown Test	54F		100	μA	Max	V _{IN} = 7.0V
		74F		7.0			
I _{CEX}	Output HIGH Leakage Current	54F		250	μA	Max	V _{OUT} = V _{CC}
		74F		50			
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V
I _{OS}	Output Short-Circuit Current			-60	mA	Max	V _{OUT} = 0V
I _{CC}	Power Supply Current		22.5	34.0	mA	Max	CP =  D _n = \overline{MR} = HIGH

AC Electrical Characteristics

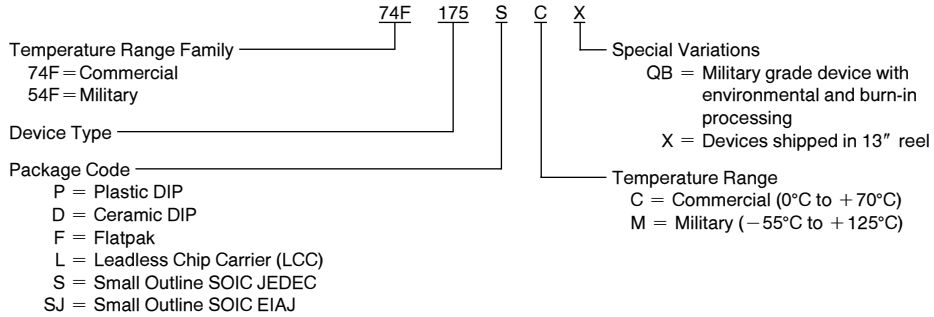
Symbol	Parameter	74F			54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Mil C _L = 50 pF		T _A , V _{CC} = Com C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	100	140		80		100		MHz
t _{PLH}	Propagation Delay CP to Q _n or \bar{Q}_n	4.0	5.0	6.5	3.5	8.5	4.0	7.5	ns
t _{PHL}	Propagation Delay CP to Q _n or \bar{Q}_n	4.0	6.5	8.5	4.0	10.5	4.0	9.5	
t _{PHL}	Propagation Delay \overline{MR} to Q _n	4.5	9.0	11.5	4.5	15.0	4.5	13.0	ns
t _{PLH}	Propagation Delay \overline{MR} to \bar{Q}_n	4.0	6.5	8.0	4.0	10.0	4.0	9.0	ns

AC Operating Requirements

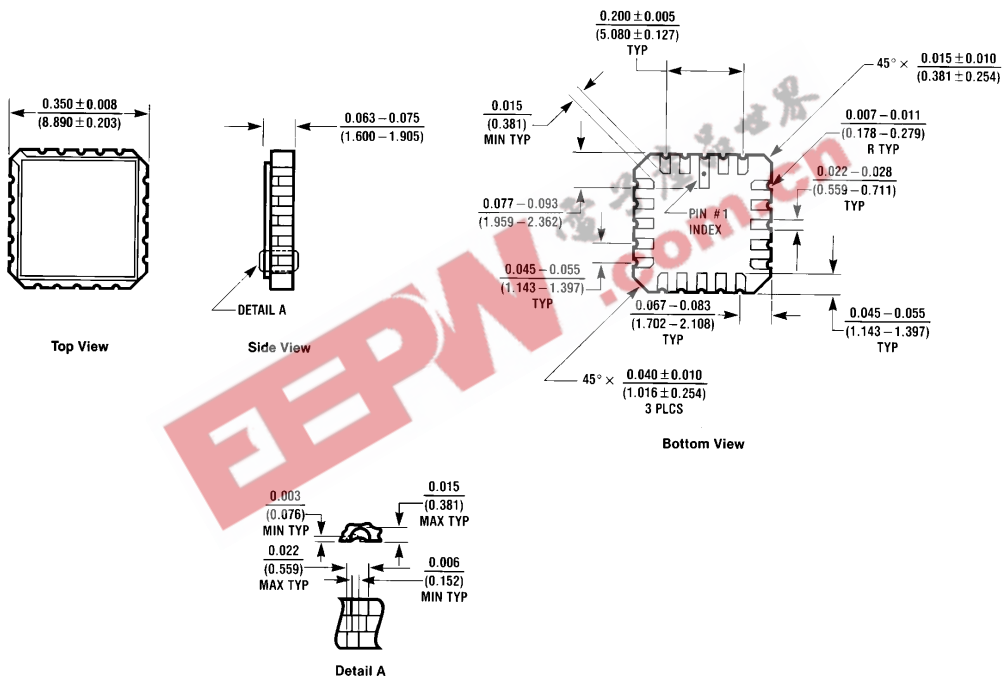
Symbol	Parameter	74F		54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V		T _A , V _{CC} = Mil		T _A , V _{CC} = Com		
		Min	Max	Min	Max	Min	Max	
t _s (H)	Setup Time, HIGH or LOW	3.0		3.0		3.0		ns
t _s (L)	D _n to CP	3.0		3.0		3.0		
t _h (H)	Hold Time, HIGH or LOW	1.0		1.0		1.0		ns
t _h (L)	D _n to CP	1.0		2.0		1.0		
t _w (H)	CP Pulse Width	4.0		4.0		4.0		ns
t _w (L)	HIGH or LOW	5.0		5.0		5.0		
t _w (L)	\overline{MR} Pulse Width, LOW	5.0		5.0		5.0		ns
t _{rec}	Recovery Time, \overline{MR} to CP	5.0		5.0		5.0		ns

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



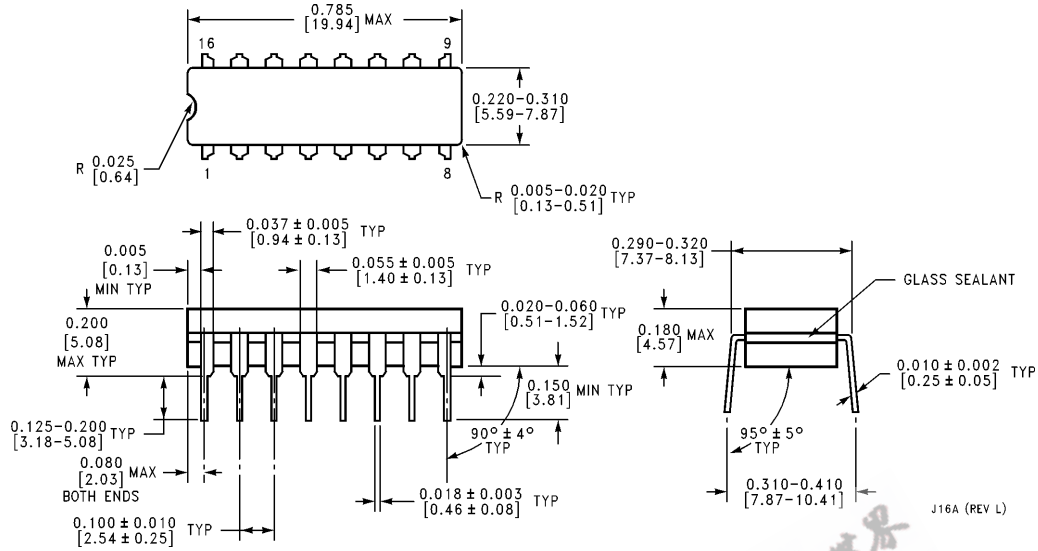
Physical Dimensions inches (millimeters)



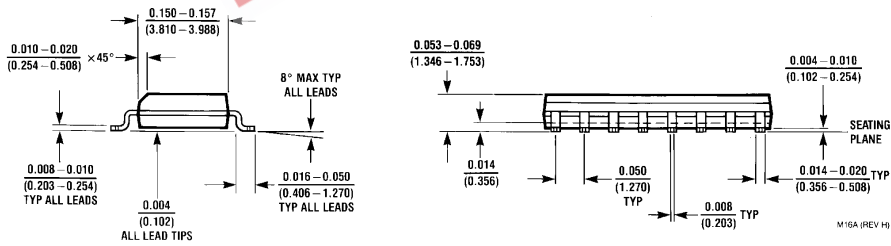
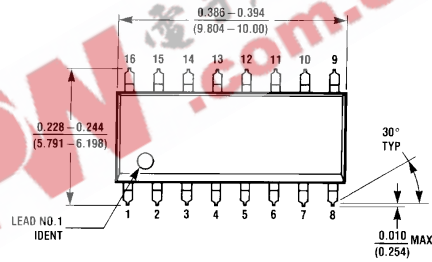
20-Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

E20A (REV D)

Physical Dimensions inches (millimeters) (Continued)

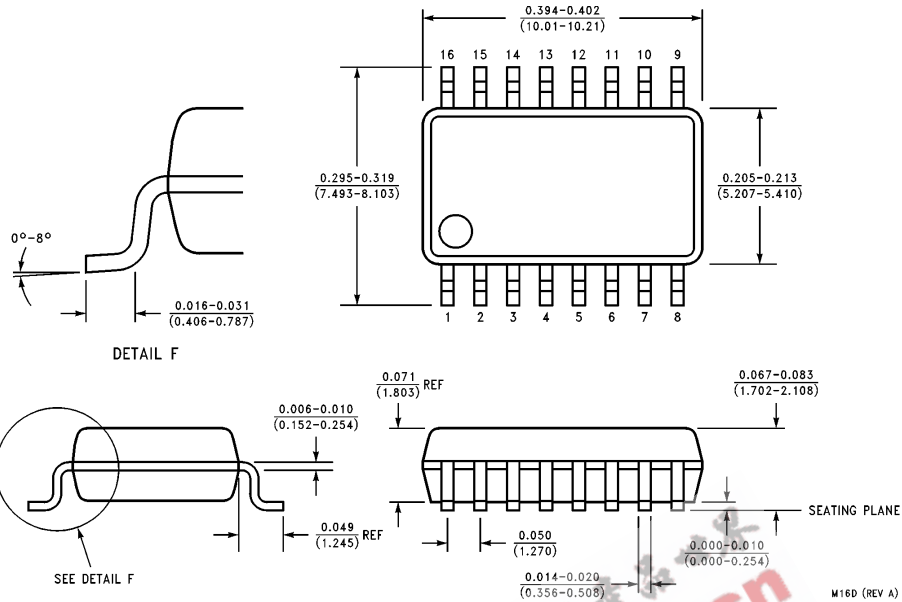


**16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A**



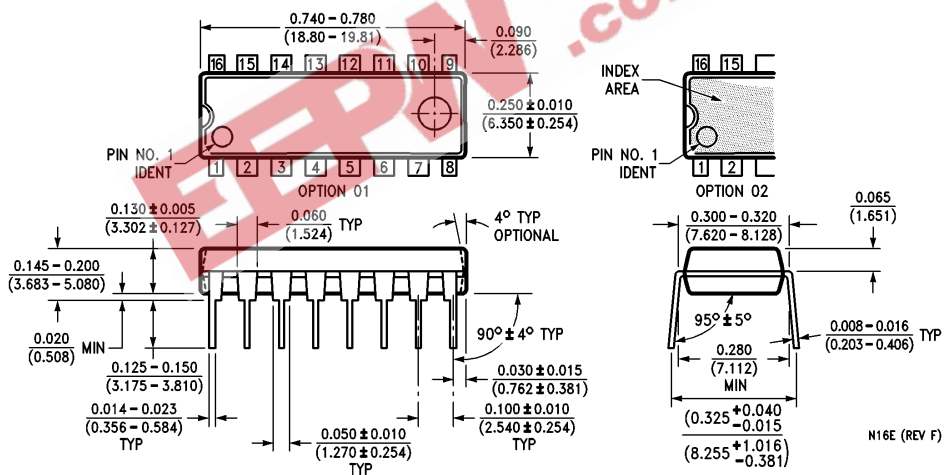
**16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M16A**

Physical Dimensions inches (millimeters) (Continued)



16-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M16D

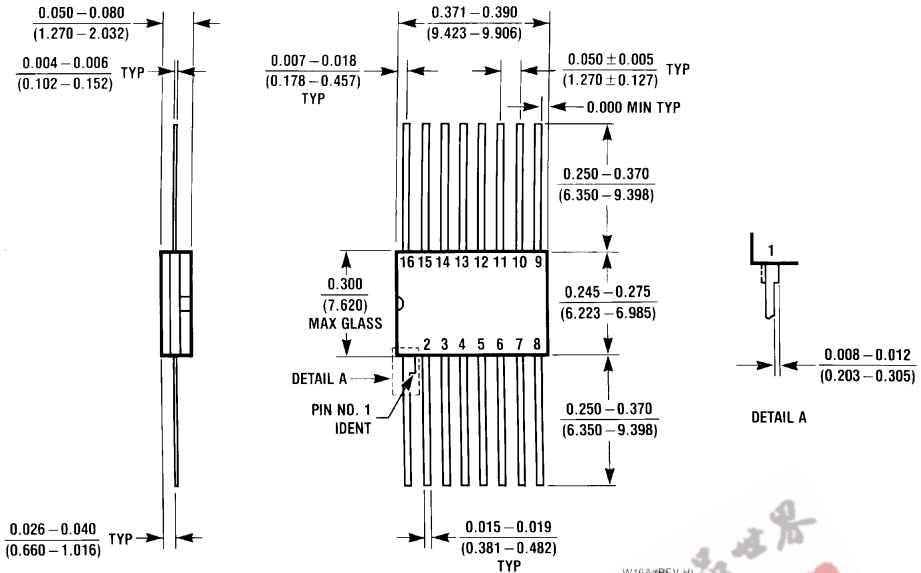
M16D (REV A)



16-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N16E

N16E (REV F)

Physical Dimensions inches (millimeters) (Continued)



**16 Lead Ceramic Flatpak (F)
NS Package Number W16A**

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