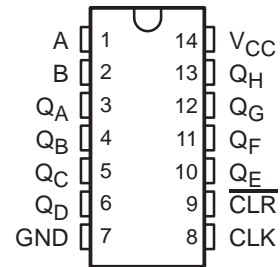


SN54HC164, SN74HC164 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

SCLS115D – DECEMBER 1982 – REVISED AUGUST 2003

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 20$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Direct Clear

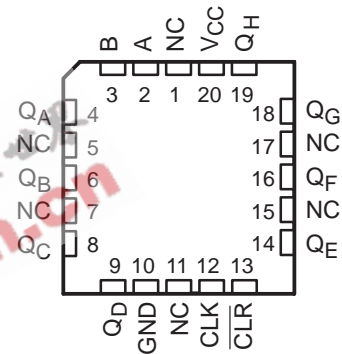
SN54HC164 . . . J OR W PACKAGE
SN74HC164 . . . D, N, NS, OR PW PACKAGE
(TOP VIEW)



description/ordering information

These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear (CLR) input. The gated serial (A and B) inputs permit complete control over incoming data; a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock (CLK) pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs can be changed while CLK is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of CLK.

SN54HC164 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HC164N	SN74HC164N
	SOIC – D	Tube of 50	SN74HC164D	HC164
		Reel of 2500	SN74HC164DR	
		Reel of 250	SN74HC164DT	
	SOP – NS	Reel of 2000	SN74HC164NSR	HC164
	TSSOP – PW	Tube of 90	SN74HC164PW	HC164
Reel of 2000		SN74HC164PWR		
Reel of 250		SN74HC164PWT		
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC164J	SNJ54HC164J
	CFP – W	Tube of 150	SNJ54HC164W	SNJ54HC164W
	LCCC – FK	Tube of 55	SNJ54HC164FK	SNJ54HC164FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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SN54HC164, SN74HC164

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

SCLS115D – DECEMBER 1982 – REVISED AUGUST 2003

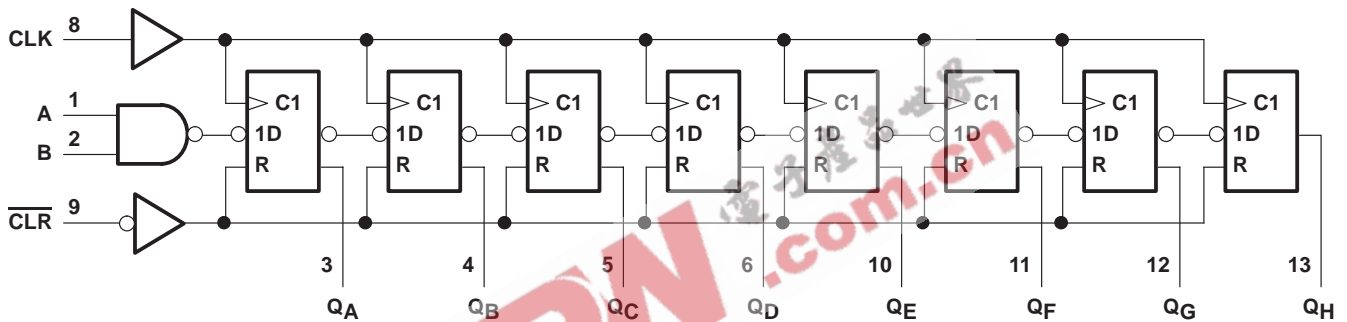
FUNCTION TABLE

INPUTS				OUTPUTS		
$\overline{\text{CLR}}$	CLK	A	B	Q _A	Q _B ... Q _H	
L	X	X	X	L	L	L
H	L	X	X	Q _{A0}	Q _{B0}	Q _{H0}
H	↑	H	H	H	Q _{An}	Q _{Gn}
H	↑	L	X	L	Q _{An}	Q _{Gn}
H	↑	X	L	L	Q _{An}	Q _{Gn}

Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established

Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of CLK: indicates a 1-bit shift

logic diagram (positive logic)



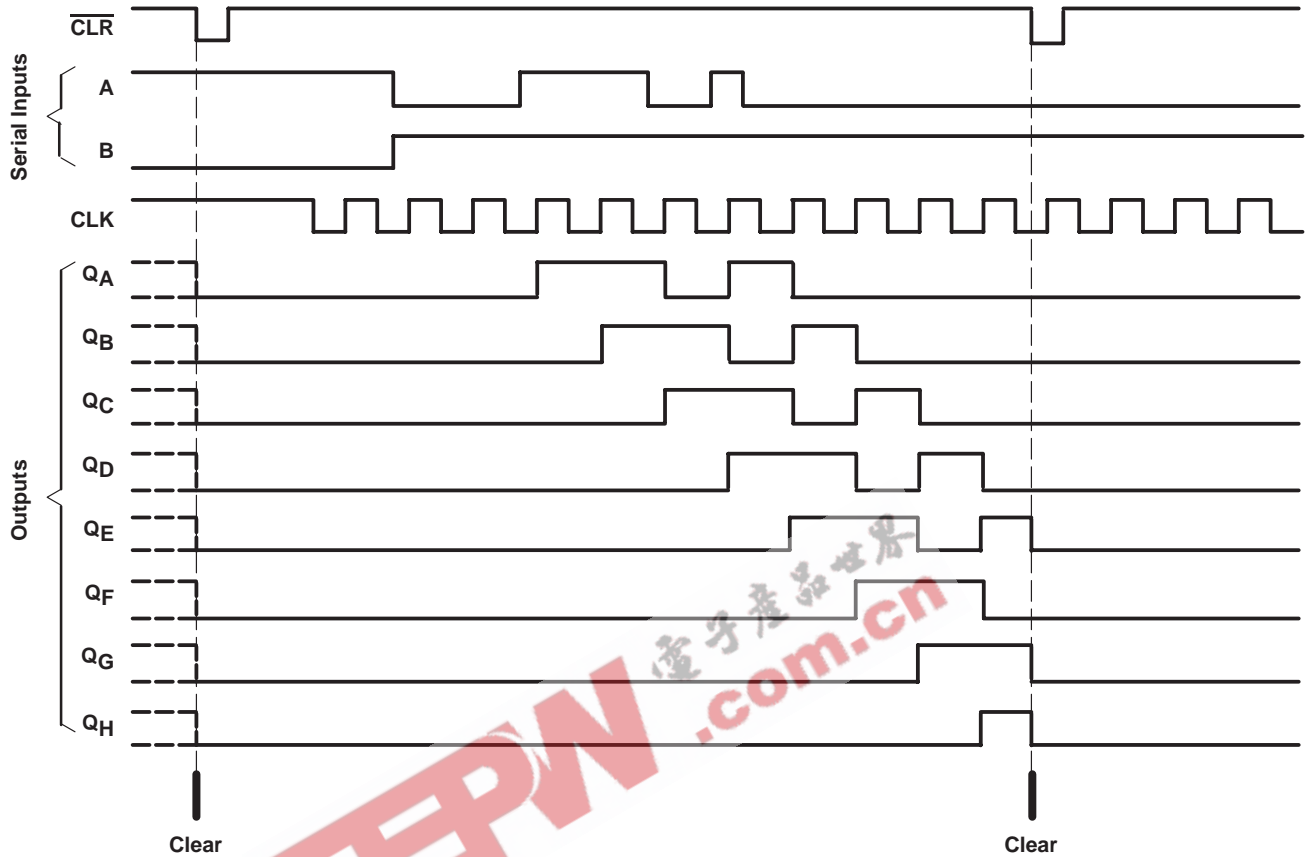
Pin numbers shown are for the D, J, N, NS, PW, and W packages.

SN54HC164, SN74HC164

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

SCLS115D – DECEMBER 1982 – REVISED AUGUST 2003

typical clear, shift, and clear sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
D package	86°C/W
N package	80°C/W
NS package	76°C/W
PW package	113°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54HC164, SN74HC164

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

SCLS115D – DECEMBER 1982 – REVISED AUGUST 2003

recommended operating conditions (see Note 3)

		SN54HC164			SN74HC164			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5		1.5		V	
		$V_{CC} = 4.5\text{ V}$	3.15		3.15			
		$V_{CC} = 6\text{ V}$	4.2		4.2			
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$	0.5		0.5		V	
		$V_{CC} = 4.5\text{ V}$	1.35		1.35			
		$V_{CC} = 6\text{ V}$	1.8		1.8			
V_I	Input voltage	0	V_{CC}		0	V_{CC}		V
V_O	Output voltage	0	V_{CC}		0	V_{CC}		V
$\Delta t/\Delta v^\dagger$	Input transition rise/fall time	$V_{CC} = 2\text{ V}$	1000		1000		ns	
		$V_{CC} = 4.5\text{ V}$	500		500			
		$V_{CC} = 6\text{ V}$	400		400			
T_A	Operating free-air temperature	-55	125		-40	85		°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

† If this device is used in the threshold region (from $V_{IL\text{max}} = 0.5\text{ V}$ to $V_{IH\text{min}} = 1.5\text{ V}$), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at $t_f = 1000\text{ ns}$ and $V_{CC} = 2\text{ V}$ does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC164		SN74HC164		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -20\ \mu\text{A}$	2 V	1.9	1.998	1.9	1.9	V		
			4.5 V	4.4	4.499	4.4	4.4			
			6 V	5.9	5.999	5.9	5.9			
		$I_{OH} = -4\text{ mA}$	4.5 V	3.98	4.3	3.7	3.84			
			6 V	5.48	5.8	5.2	5.34			
V_{OL}	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 20\ \mu\text{A}$	2 V	0.002	0.1	0.1	0.1	V		
			4.5 V	0.001	0.1	0.1	0.1			
			6 V	0.001	0.1	0.1	0.1			
		$I_{OL} = 4\text{ mA}$	4.5 V	0.17	0.26	0.4	0.33			
			6 V	0.15	0.26	0.4	0.33			
I_I	$V_I = V_{CC}$ or 0	6 V	± 0.1	± 100	± 1000	± 1000	nA			
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$	6 V		8	160	80	μA			
C_i		2 V to 6 V		3	10	10	10	pF		

SN54HC164, SN74HC164

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

SCLS115D – DECEMBER 1982 – REVISED AUGUST 2003

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V _{CC}	T _A = 25°C		SN54HC164		SN74HC164		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	2 V	6		4.2		5		MHz
		4.5 V	31		21		25		
		6 V	36		25		28		
t _w	Pulse duration	$\overline{\text{CLR}}$ low	2 V	100	150	125			ns
			4.5 V	20	30	25			
			6 V	17	25	21			
	CLK high or low	2 V	80	120	100				
		4.5 V	16	24	20				
		6 V	14	20	18				
t _{su}	Setup time before CLK↑	Data	2 V	100	150	125			ns
			4.5 V	20	30	25			
			6 V	17	25	21			
	$\overline{\text{CLR}}$ inactive	2 V	100	150	125				
		4.5 V	20	30	25				
		6 V	17	25	21				
t _h	Hold time, data after CLK↑		2 V	5	5	5			ns
			4.5 V	5	5	5			
			6 V	5	5	5			

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC164		SN74HC164		UNIT	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		
f _{max}			2 V	6	10		4.2	5			MHz	
			4.5 V	31	54		21	25				
			6 V	36	62		25	28				
t _{PHL}	$\overline{\text{CLR}}$	Any Q	2 V		140	205		295	255			ns
			4.5 V		28	41		59	51			
			6 V		24	35		51	46			
t _{pd}	CLK	Any Q	2 V		115	175		265	220			ns
			4.5 V		23	35		53	44			
			6 V		20	30		45	38			
t _t			2 V		38	75		110	95			ns
			4.5 V		8	15		22	19			
			6 V		6	13		19	16			

operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	No load	135	pF

SN54HC164, SN74HC164 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

SCLS115D – DECEMBER 1982 – REVISED AUGUST 2003

PARAMETER MEASUREMENT INFORMATION

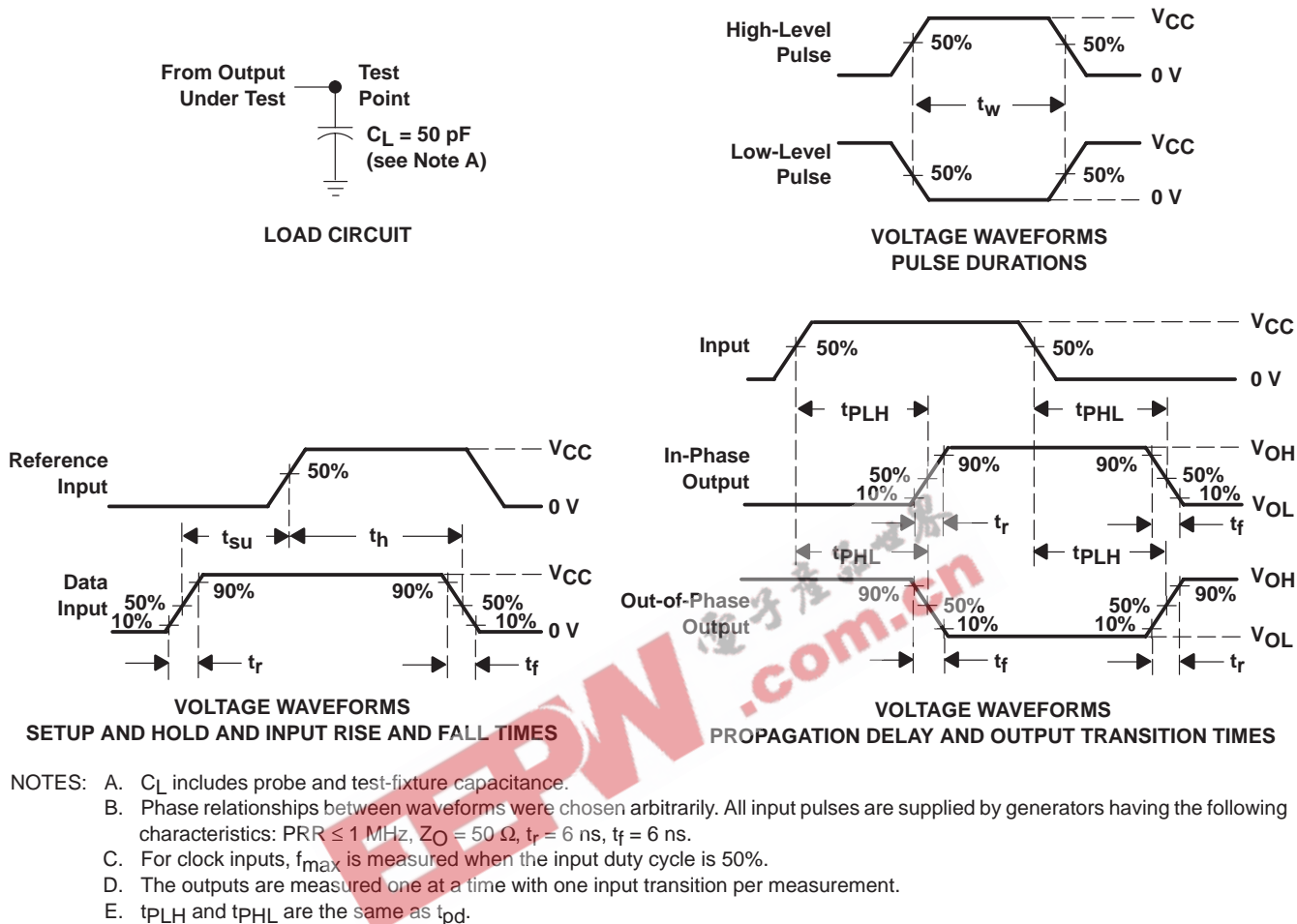
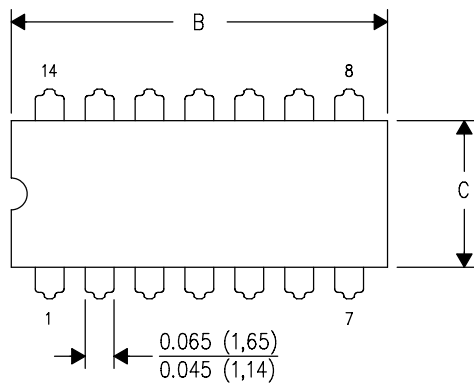


Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T**)
14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

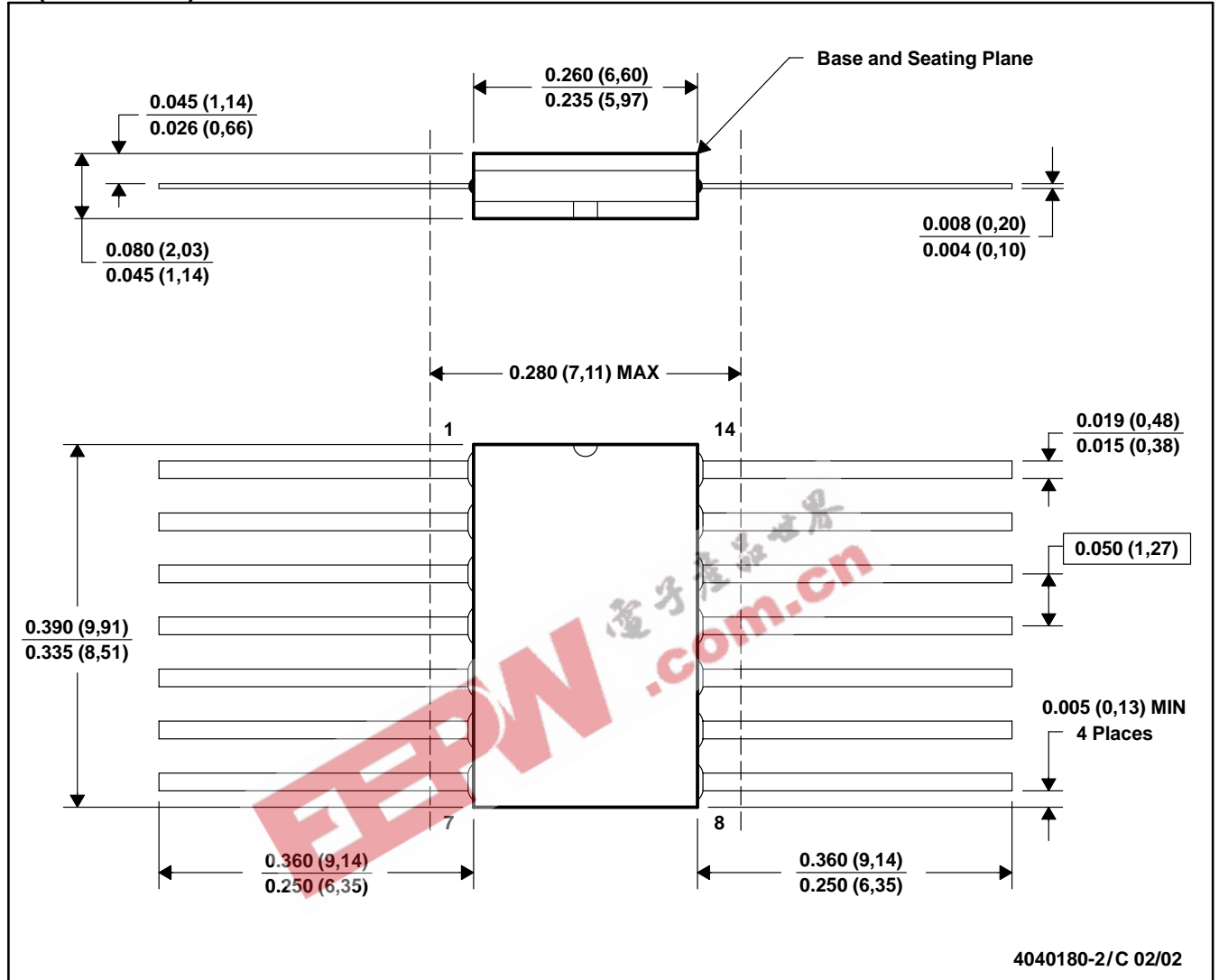
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

MCFP002A – JANUARY 1995 – REVISED FEBRUARY 2002

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK

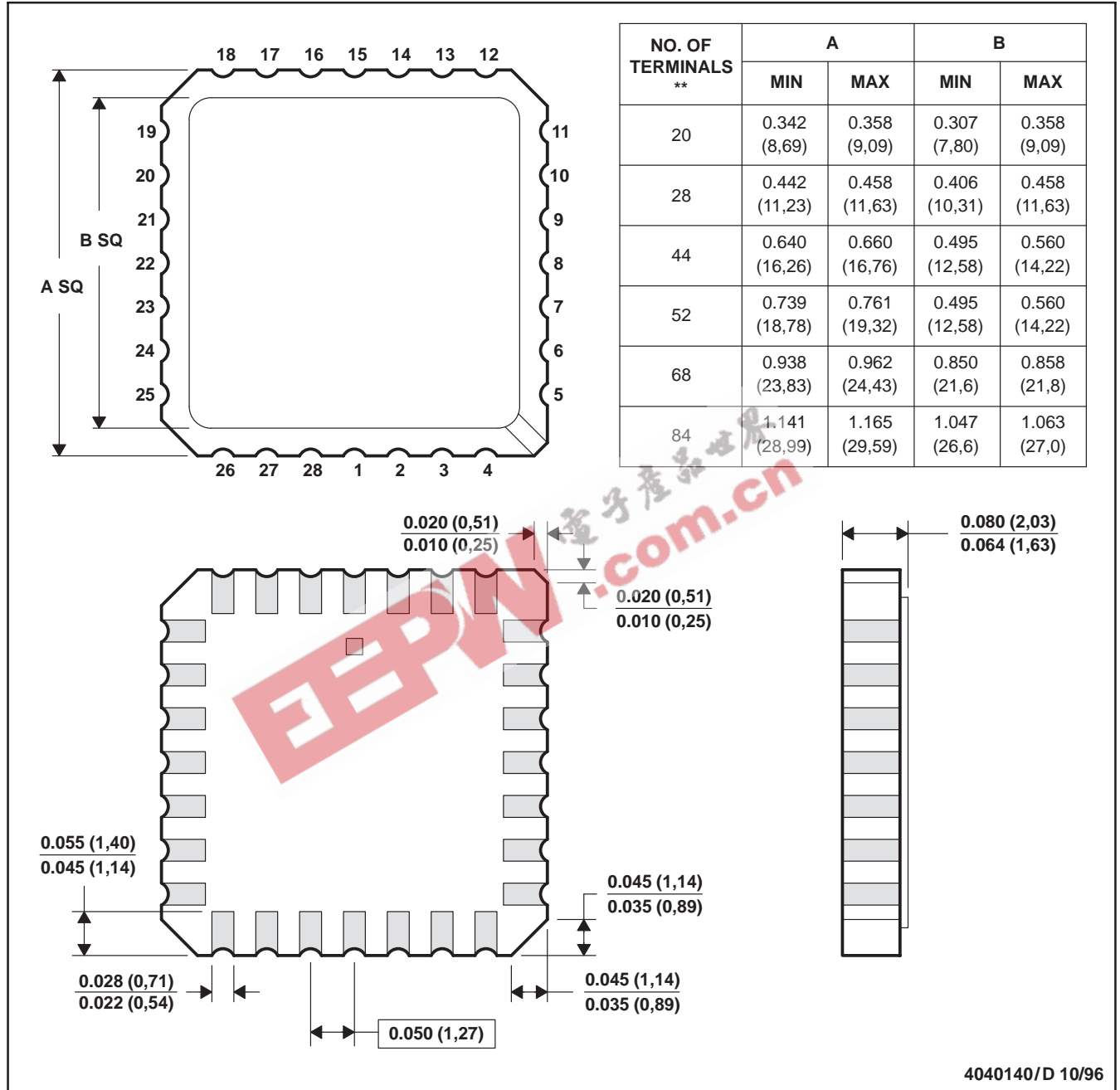


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

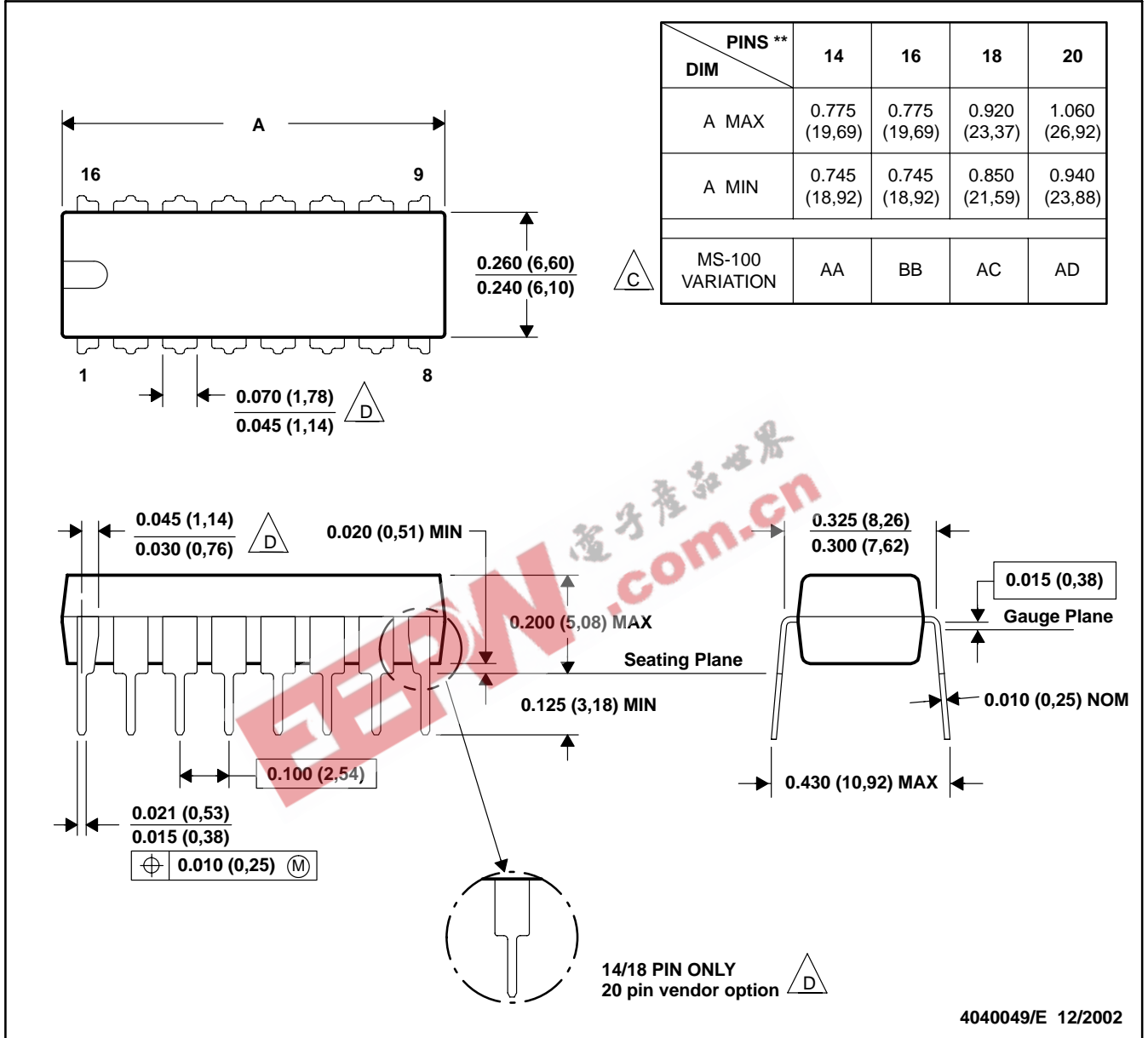
MECHANICAL

MPDI002C – JANUARY 1995 – REVISED DECEMBER 2002

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

The 20 pin end lead shoulder width is a vendor option, either half or full width.

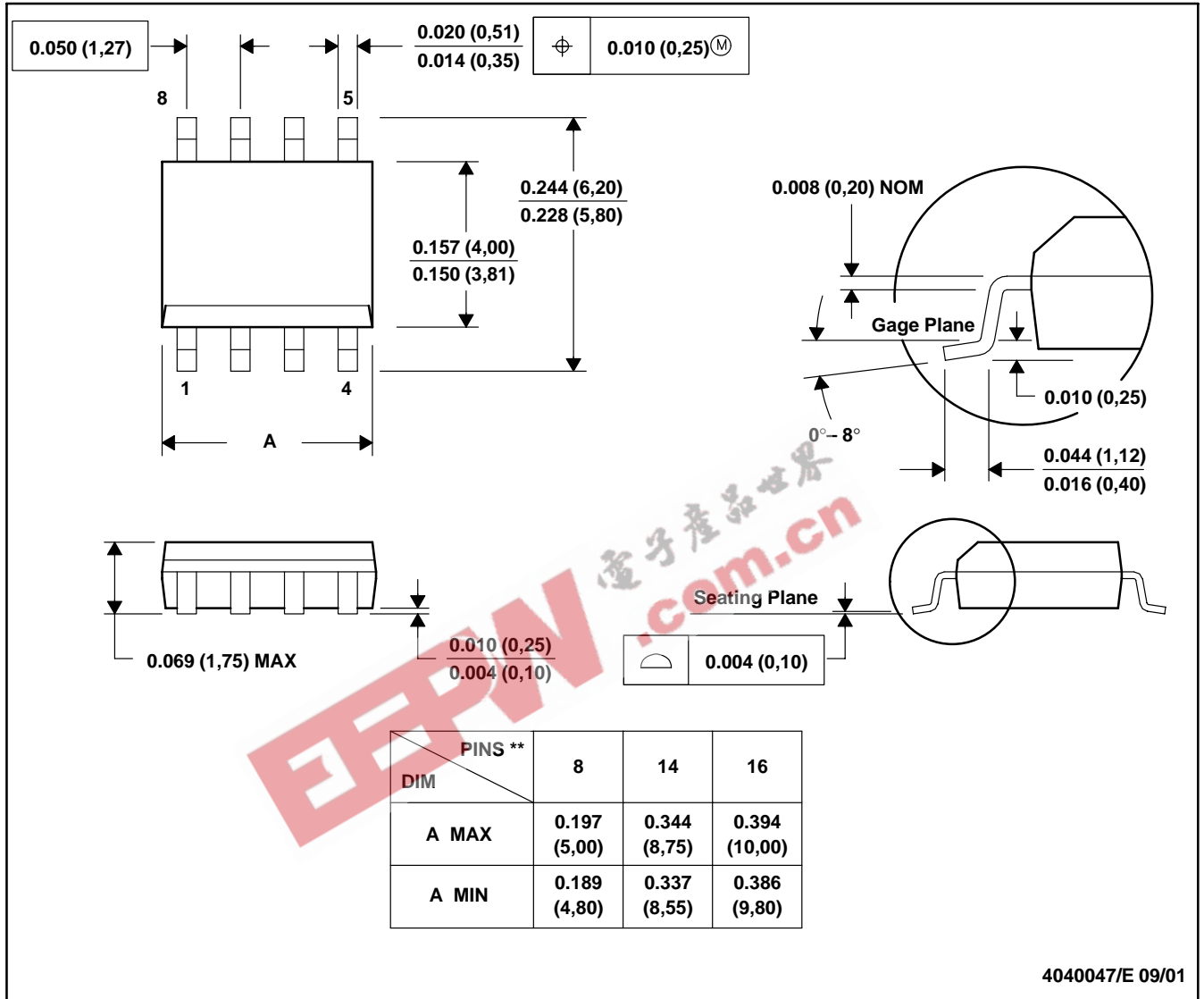
MECHANICAL DATA

MSOI002B – JANUARY 1995 – REVISED SEPTEMBER 2001

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



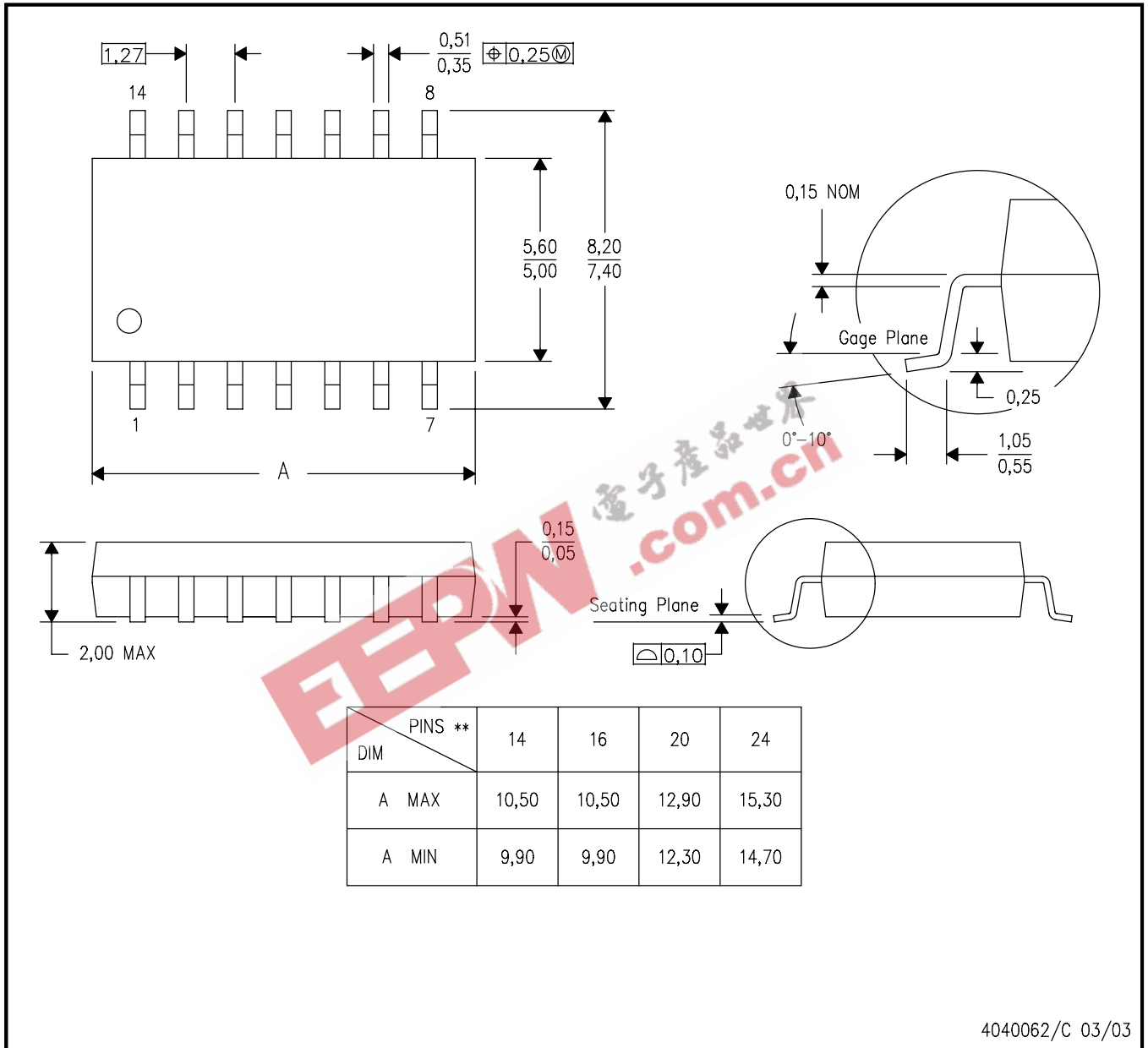
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

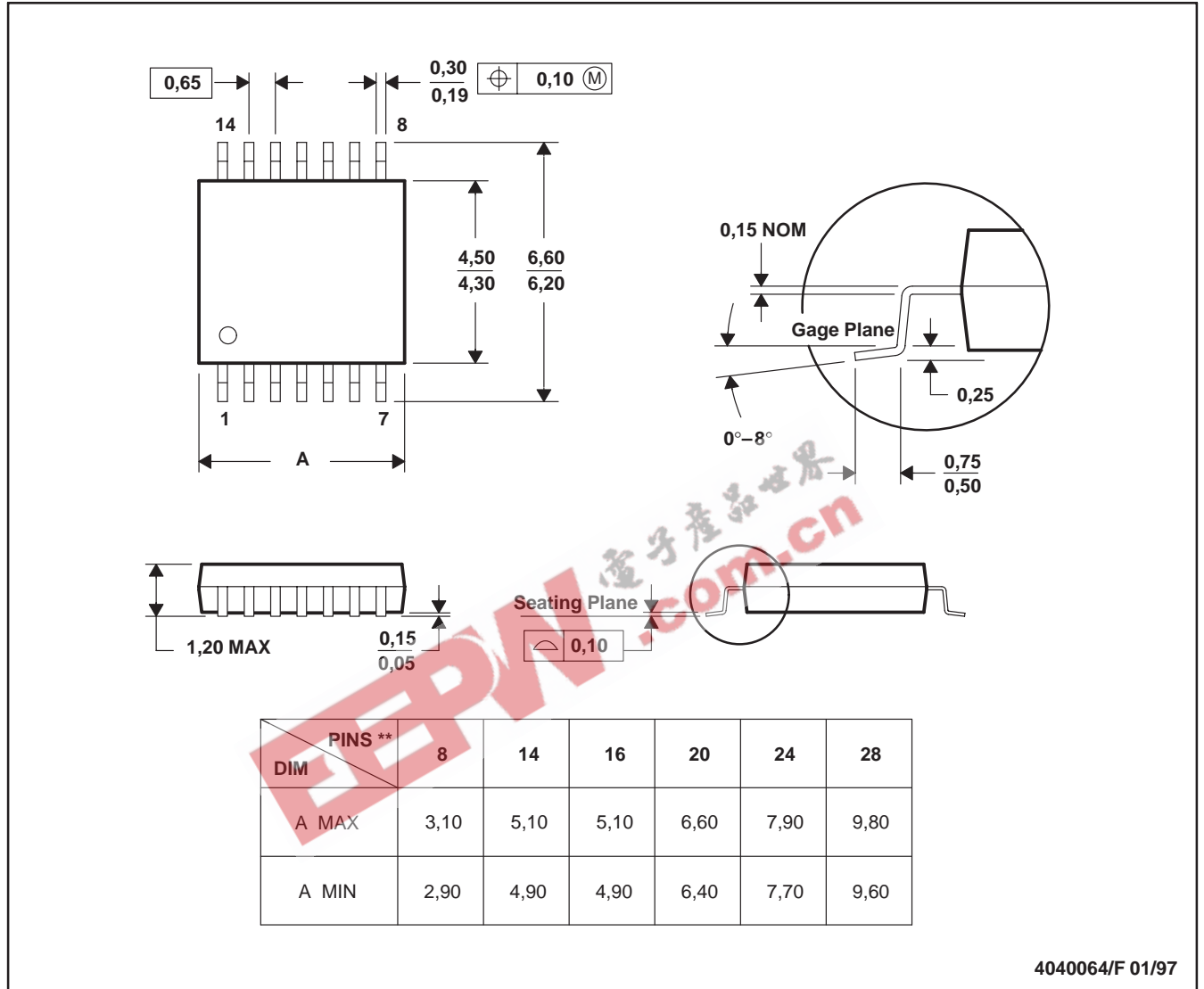
MECHANICAL DATA

MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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