

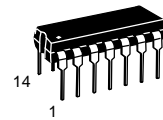
74HC164

Description

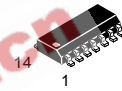
The 74HC164 is identical in pinout to the LS/ALS164. The Device inputs are compatible with standard CMOS outputs, with pullup resistors, they are compatible with LS/ALSTTL outputs. The 74HC164 is an 8-bit, serial-input parallel-output shift register. Two serial data inputs, A1 and A2, are provided so that one input may be used as a data enable. Data is entered on each rising edge of the clock. The active-low asynchronous Reset overrides the Clock and Serial Data inputs.

Features

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices



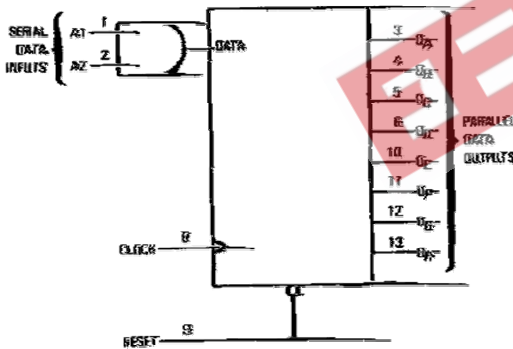
DIP - 14



SOP -14

Package

Logic Diagram



Pin Assignment

A1	1	14	V _{CC}
A2	2	13	QH
QA	3	12	QG
QB	4	11	QF
QC	5	10	QE
QD	6	9	RESET
GND	7	8	CLOCK

Function Table

Inputs			Outputs
RESET	CLOCK	A1	QA QB... QH
L	X	X	L L...
H		X X	L
H		X H D	no change
H			D QAn... QGn D

D = data input

X = don't care

Q_{An} - Q_{Gn} = data shifted from the previous stage on a rising edge at the clock input.

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±20	
I _{OUT}	DC Output Current, per Pin	±25	
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	
P _D	Power Dissipation in Still Air, Plastic DIP+	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/ °C from 65 ° to 125 °C
SOIC Package: - 7 mW/ °C from 65 ° to 125 °C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)			ns
	V _{CC} = 2.0	0	1000	
	V _{CC} = 4.5	0	500	
	V _{CC} = 6.0	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range

$$GND \leq (V_{IN \text{ or } V_{OUT}}) \leq V_{CC}$$

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

DC Electrical Characteristics

(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25 °C to -55 °C	≤ 85	≤ 125	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low - Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I _{IN}	Maximum Input Leakage Current	V _{IN} =V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
			4.5	0.26	0.33	0.4	
			6.0	0.26	0.33	0.4	
I _{CC} Quiescent	Maximum Supply Current	V _{IN} =V _{CC} or GND I _{OUT} =0μA	6.0	8.0	80	160	μA

AC Electrical Characteristics

($C_L = 50\text{pF}$, Input $t_r = t_f$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25 °C to -55 °C	≤85 °C	≤125 °C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t _{PLH} , t _{PHL} (Figures 1 and 4)	Maximum Propagation Delay, Clock to Q	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t _{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	2.0	205	255	310	ns
		4.5	41	51	62	
		6.0	35	43	53	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{IN}	Maximum Input Capacitance	-	10	10	10	pF
t _{SU}	Minimum Setup Time, A1 or A2 to Clock (Figure 3)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t _H	Minimum Hold Time, Clock to A1 or A2 (Figure 3)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t _{REC}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t _w	Minimum Pulse Width, Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	
C _{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $2f + I_{CC}V_{CC}C_{PD} = C_{PD}V$	Typical @25 °C, V _{CC} =5.0 V			pF	
		140				

74HC164

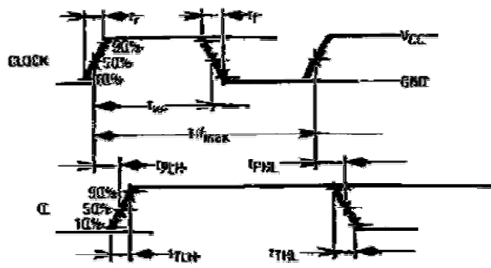


Figure 1. Switching Waveforms

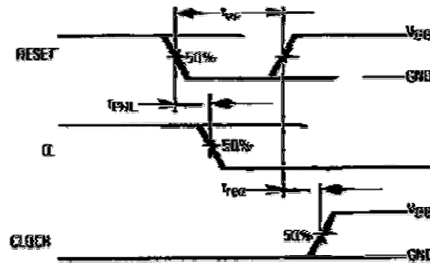


Figure 2. Switching Waveforms

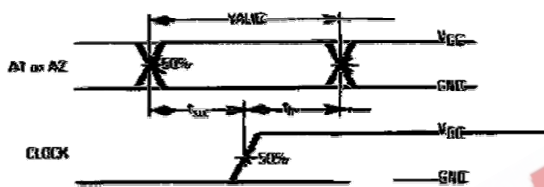


Figure 3. Switching Waveforms

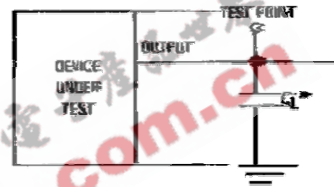
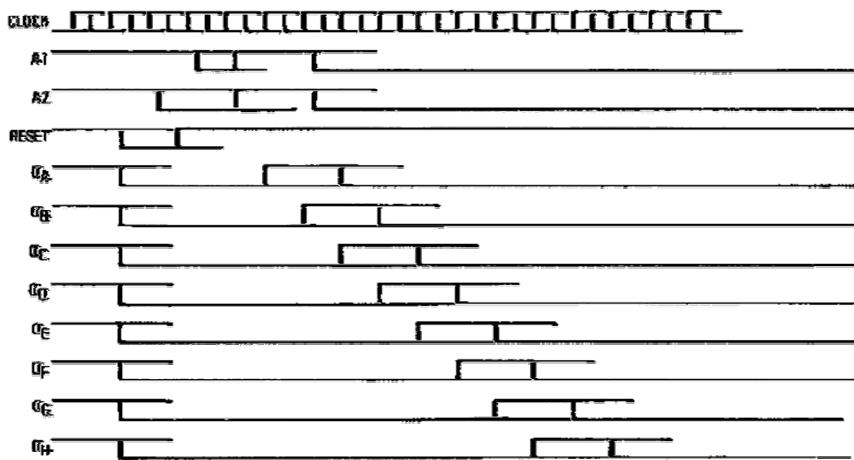


Figure 4. Test Circuit

Timing Diagram



74HC164

Expanded Logic Diagram

Ordering Information

ORDERING NUMBER	PACKAGE	MARKING
74HC164	DIP - 14 / SOP - 14	ESTEK74HC164

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