

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

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74HC/HCT280 9-bit odd/even parity generator/checker

Product specification
File under Integrated Circuits, IC06

December 1990

9-bit odd/even parity generator/checker

74HC/HCT280

FEATURES

- Word-length easily expanded by cascading
- Similar pin configuration to the "180" for easy system up-grading
- Generates either odd or even parity for nine data bits
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT280 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT280 are 9-bit parity generators or checkers commonly used to detect errors in high-speed data

transmission or data retrieval systems. Both even and odd parity outputs are available for generating or checking even or odd parity up to 9 bits.

The even parity output (Σ_E) is HIGH when an even number of data inputs (I_0 to I_8) are HIGH. The odd parity output (Σ_O) is HIGH when an odd number of data inputs are HIGH.

Expansion to larger word sizes is accomplished by tying the even outputs (Σ_E) of up to nine parallel devices to the data inputs of the final stage. For a single-chip 16-bit even/odd parity generator/checker, see PC74HC/HCT7080.

APPLICATIONS

- 25-line parity generator/checker
- 81-line parity generator/checker

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|-------------------------------------|---|---|---------|-----|------|
| | | | HC | HCT | |
| t _{PHL} / t _{PLH} | propagation delay | C _L = 15 pF; V _{CC} = 5 V | | | |
| | I _n to Σ_E | | 17 | 18 | ns |
| | I _n to Σ_O | | 20 | 22 | ns |
| C _I | input capacitance | | 3.5 | 3.5 | pF |
| C _{PD} | power dissipation capacitance per package | notes 1 and 2 | 65 | 65 | pF |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

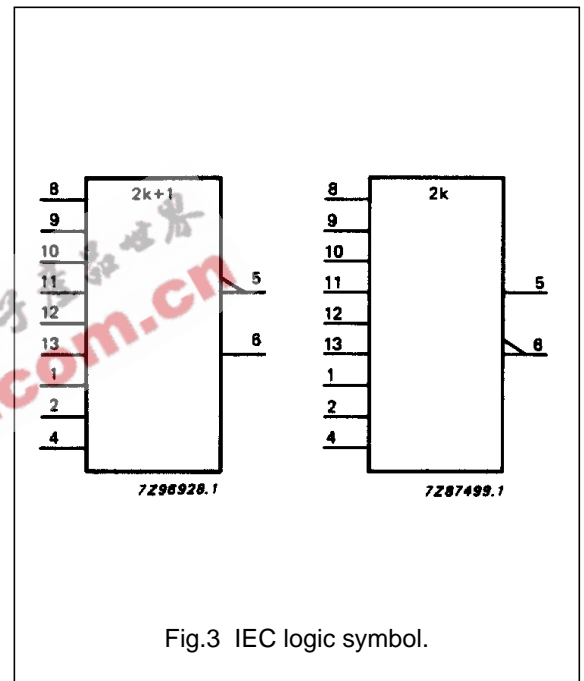
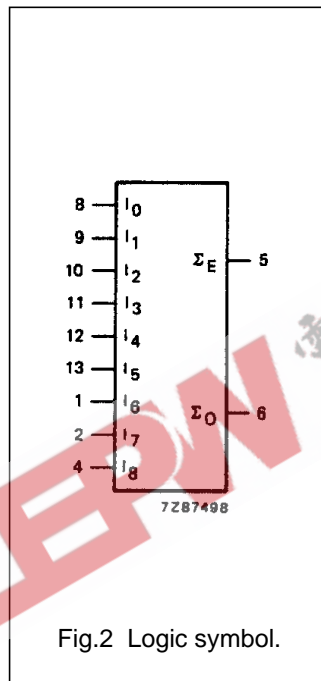
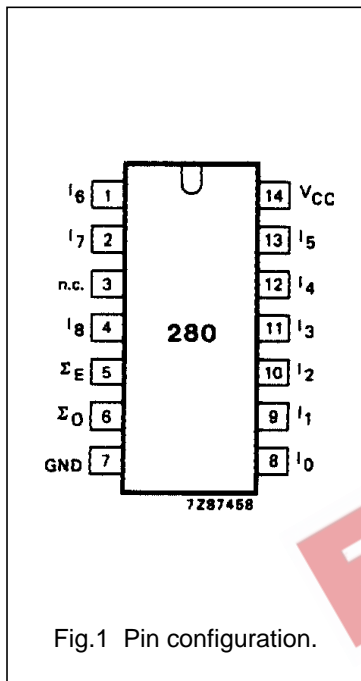
See "74HC/HCT/HCU/HCMOS Logic Package Information".

9-bit odd/even parity generator/checker

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PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|-------------------------------|-------------------------|-------------------------|
| 8, 9, 10, 11, 12, 13, 1, 2, 4 | I_0 to I_8 | data inputs |
| 5, 6 | ΣE , ΣO | parity outputs |
| 7 | GND | ground (0 V) |
| 14 | V_{CC} | positive supply voltage |



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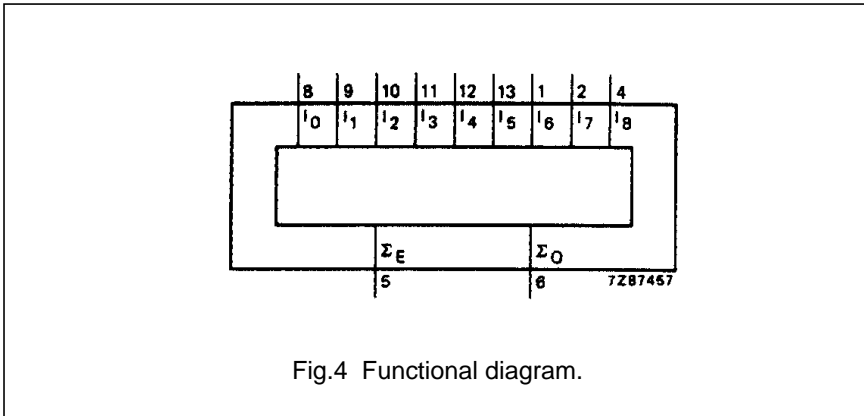


Fig.4 Functional diagram.

FUNCTION TABLE

| INPUTS | OUTPUTS | |
|--|----------------|----------------|
| | Σ _E | Σ _O |
| number of HIGH data inputs (I ₀ to I ₈) | | |
| even | H | L |
| odd | L | H |

Note

1. H = HIGH voltage level
L = LOW voltage level

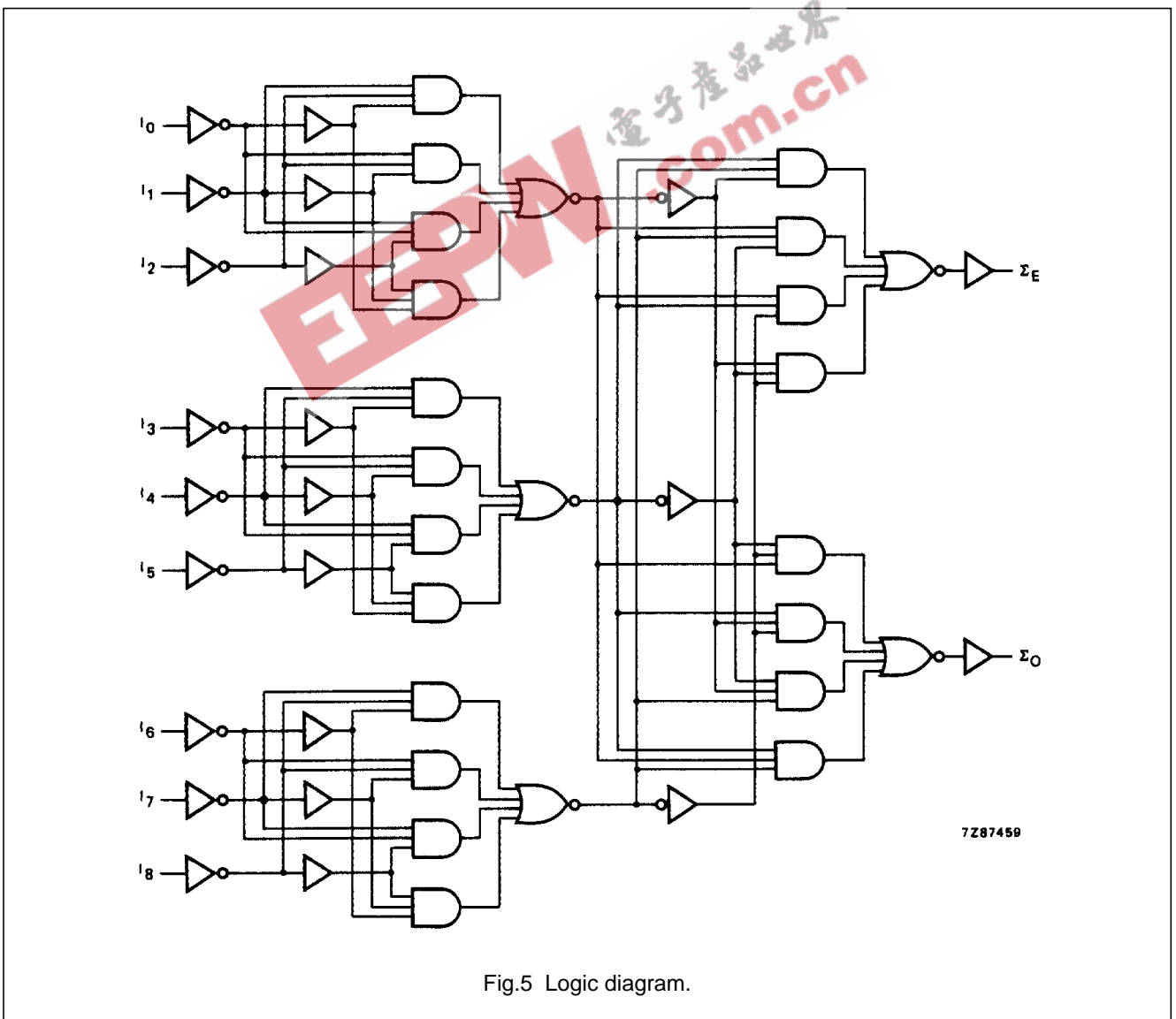


Fig.5 Logic diagram.

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Out put capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | UNIT | TEST CONDITIONS | | |
|-------------------------------------|---|-----------------------|----------------|-----------------|------------|-----------------|-------------|-----------------|------------------------|-------------------|-------|
| | | 74HC | | | | | | | V _{CC} (V) | WAVEFORMS | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | | | | max. |
| t _{PHL} / t _{PLH} | propagation delay I _n to Σ _E | | 55 20 16 | 200 40 34 | | 250 50 43 | | 300 60 51 | ns | 2.0 4.5 6.0 | Fig.6 |
| t _{PHL} / t _{PLH} | propagation delay I _n to Σ _O | | 63 23 18 | 200 40 34 | | 250 50 43 | | 300 60 51 | ns | 2.0 4.5 6.0 | Fig.6 |
| t _{THL} / t _{TLH} | output transition time | | 19 7 6 | 75 15 13 | | 95 19 16 | | 110 22 19 | ns | 2.0 4.5 6.0 | Fig.6 |

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|----------------|-----------------------|
| I _n | 1.0 |

AC CHARACTERISTICS FOR 74HCT

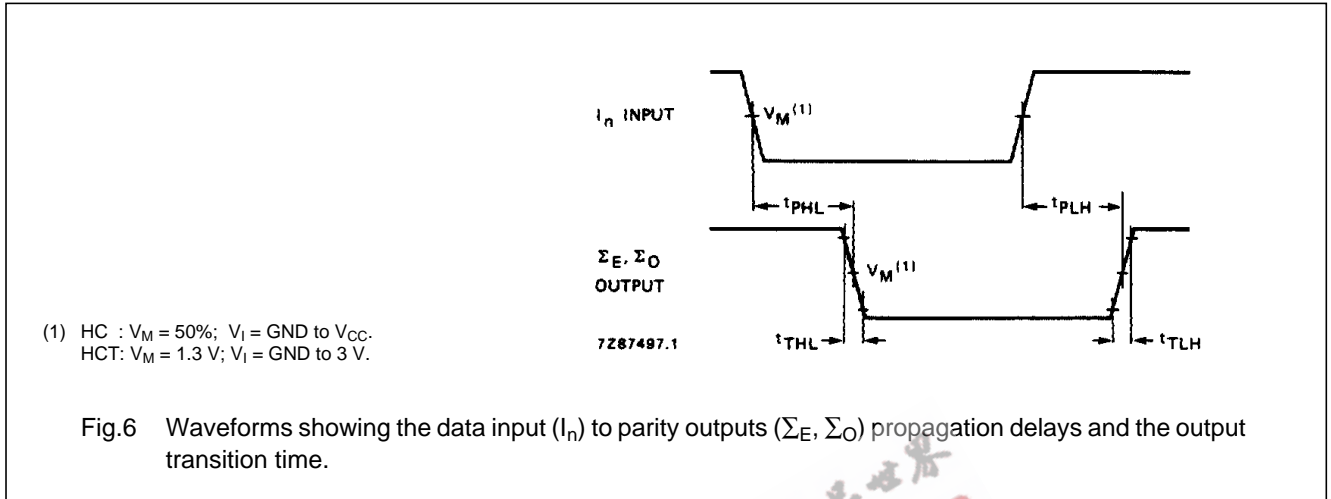
GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | | UNIT | TEST CONDITIONS | |
|-------------------------------------|---|-----------------------|------|------|------------|------|-------------|------|----|------|------------------------|-----------|
| | | 74HCT | | | | | | | | | V _{CC} (V) | WAVEFORMS |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | |
| t _{PHL} / t _{PLH} | propagation delay I _n to Σ_E | | 21 | 42 | | | 53 | | 63 | ns | 4.5 | Fig.6 |
| t _{PHL} / t _{PLH} | propagation delay I _n to Σ_O | | 26 | 45 | | | 56 | | 68 | ns | 4.5 | Fig.6 |
| t _{THL} / t _{TLH} | output transition time | | 7 | 15 | | | 19 | | 22 | ns | 4.5 | Fig.6 |

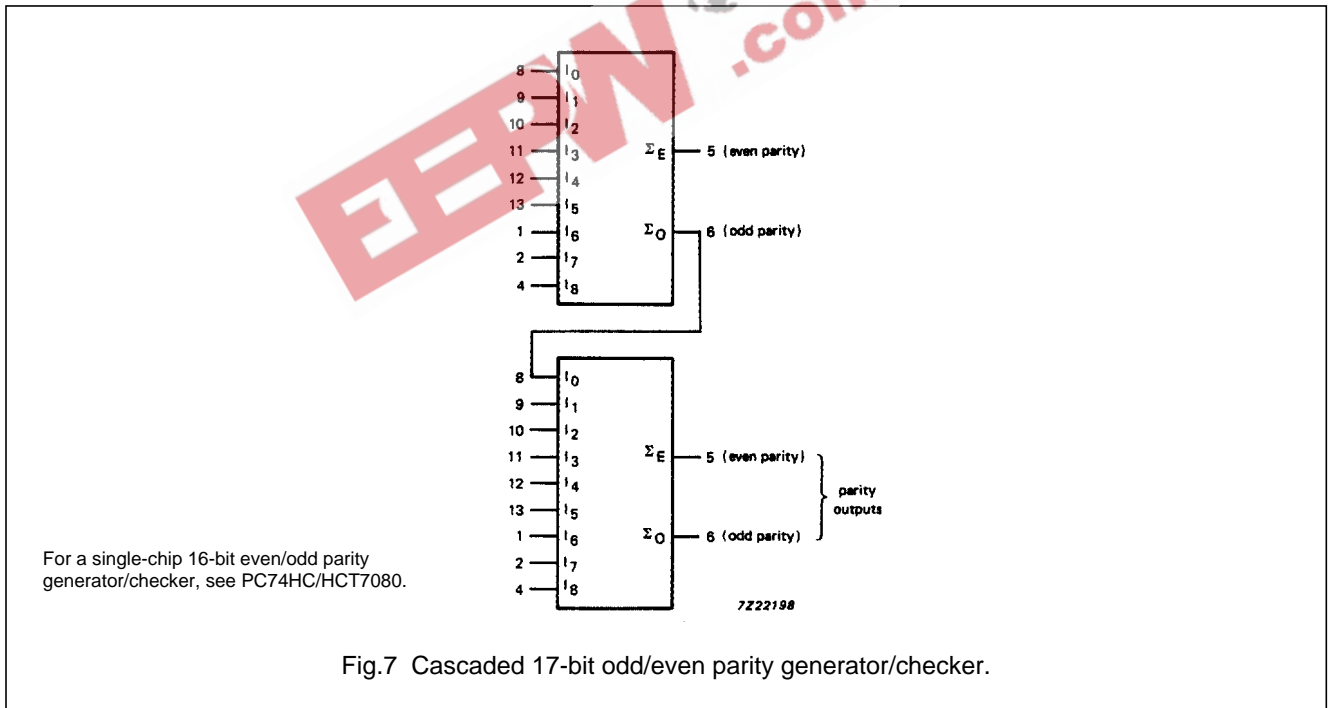
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AC WAVEFORMS



APPLICATION INFORMATION



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".