# 2.7 V, 800 μA, 80 MHz Rail-to-Rail I/O Amplifiers

# AD8031/AD8032

## FEATURES

**Low Power**
- Supply Current 800 μA/Amplifier
- Fully Specified at +2.7 V, +5 V and ±5 V Supplies

**High Speed and Fast Settling on +5 V**
- 80 MHz –3 dB Bandwidth (G = +1)
- 30 V/μs Slew Rate
- 125 ns Settling Time to 0.1%

**Rail-to-Rail Input and Output**
- No Phase Reversal with Input 0.5 V Beyond Supplies
- Input CMVR Extends Beyond Rails by 200 mV
- Output Swing to Within 20 mV of Either Rail

**Low Distortion**
- –62 dB @ 1 MHz, $V_O$ = 2 V p-p
- –86 dB @ 100 kHz, $V_O$ = 4.6 V p-p

**Output Current: 15 mA**

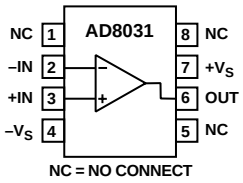
**High Grade Option**
- $V_{OS}$ (max) = 1.5 mV

## APPLICATIONS

**High-Speed Battery-Operated Systems**
**High Component Density Systems**
**Portable Test Instruments**
**A/D Buffer**
**Active Filters**
**High-Speed Set-and-Demand Amplifier**

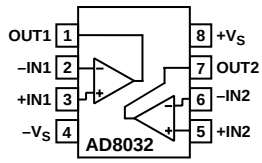
## CONNECTION DIAGRAMS

**8-Lead Plastic DIP (N) and SOIC (R) Packages**

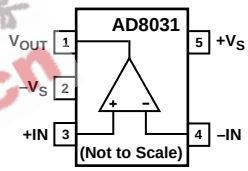



NC = NO CONNECT

**8-Lead Plastic DIP (N), SOIC (R) and μSOIC (RM) Packages**




**5-Lead Plastic Surface Mount Package SOT-23-5 (RT-5)**



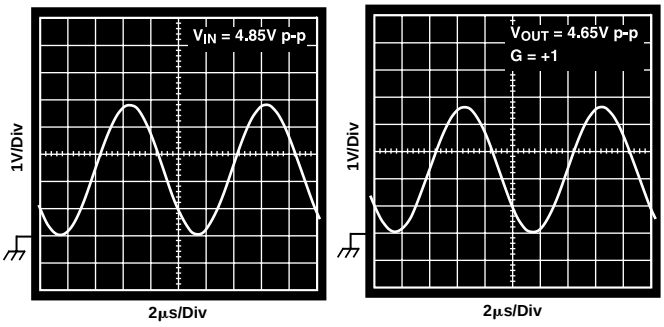

## GENERAL DESCRIPTION

The AD8031 (single) and AD8032 (dual) single supply voltage feedback amplifiers feature high-speed performance with 80 MHz of small signal bandwidth, 30 V/μs slew rate and 125 ns settling time. This performance is possible while consuming less than 4.0 mW of power from a single +5 V supply. These features increase the operation time of high speed battery-powered systems without compromising dynamic performance.

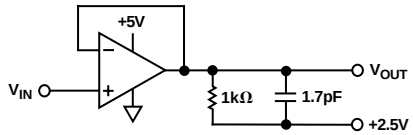
The products have true single supply capability with rail-to-rail input and output characteristics and are specified for +2.7 V, +5 V and ±5 V supplies. The input voltage range can extend to 500 mV beyond each rail. The output voltage swings to within 20 mV of each rail providing the maximum output dynamic range.

The AD8031/AD8032 also offer excellent signal quality for only 800 μA of supply current per amplifier; THD is –62 dBc with a 2 V p-p, 1 MHz output signal and –86 dBc for a 100 kHz, 4.6 V p-p signal on +5 V supply. The low distortion and fast settling time make them ideal as buffers to single supply, A-to-D converters.

Operating on supplies from +2.7 V to +12 V and dual supplies up to ±6 V, the AD8031/AD8032 are ideal for a wide range of applications, from battery-operated systems with large bandwidth requirements to high-speed systems where component density requires lower power dissipation. The AD8031/AD8032 are available in 8-lead plastic DIP and SOIC packages and will operate over the industrial temperature range of –40°C to +85°C. The AD8031A is also available in the space-saving 5-lead SOT-23-5 package and the AD8032A is available in AN 8-lead μSOIC package.




*Input $V_{IN}$* *Output $V_{OUT}$*




*Circuit Diagram*

*Figure 1. Rail-to-Rail Performance at 100 kHz*

REV. B



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# AD8031/AD8032–SPECIFICATIONS

## +2.7 V Supply (@ $T_A$ = +25°C, $V_S$ = +2.7 V, $R_L$ = 1 kΩ to +1.35 V, $R_F$ = 2.5 kΩ unless otherwise noted)

| Parameter | Conditions | AD8031A/AD8032A Min | AD8031A/AD8032A Typ | AD8031A/AD8032A Max | AD8031B/AD8032B Min | AD8031B/AD8032B Typ | AD8031B/AD8032B Max | Units |
|---|---|---|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | | | | |
| –3 dB Small Signal Bandwidth | G = +1, $V_O$ < 0.4 V p-p | 54 | 80 | | 54 | 80 | | MHz |
| Slew Rate | G = –1, $V_O$ = 2 V Step | 25 | 30 | | 25 | 30 | | V/μs |
| Settling Time to 0.1% | G = –1, $V_O$ = 2 V Step, $C_L$ = 10 pF | | 125 | | | 125 | | ns |
| DISTORTION/NOISE PERFORMANCE | | | | | | | | |
| Total Harmonic Distortion | $f_C$ = 1 MHz, $V_O$ = 2 V p-p, G = +2 | | –62 | | | –62 | | dBc |
| | $f_C$ = 100 kHz, $V_O$ = 2 V p-p, G = +2 | | –86 | | | –86 | | dBc |
| Input Voltage Noise | f = 1 kHz | | 15 | | | 15 | | nV/√Hz |
| Input Current Noise | f = 100 kHz | | 2.4 | | | 2.4 | | pA/√Hz |
| | f = 1 kHz | | 5 | | | 5 | | pA/√Hz |
| Crosstalk (AD8032 Only) | f = 5 MHz | | –60 | | | –60 | | dB |
| DC PERFORMANCE | | | | | | | | |
| Input Offset Voltage | $V_{CM} = \frac{V_{CC}}{2}$; $V_{OUT}$ = 1.35 V | | ±1 | ±6 | | ±0.5 | ±1.5 | mV |
| | $T_{MIN}$ to $T_{MAX}$ | | ±6 | ±10 | | ±1.6 | ±2.5 | mV |
| Offset Drift | $V_{CM} = \frac{V_{CC}}{2}$; $V_{OUT}$ = 1.35 V | | 10 | | | 10 | | μV/°C |
| Input Bias Current | $V_{CM} = \frac{V_{CC}}{2}$; $V_{OUT}$ = 1.35 V | | 0.45 | 2 | | 0.45 | 2 | μA |
| | $T_{MIN}$ to $T_{MAX}$ | | | 2.2 | | | 2.2 | μA |
| Input Offset Current | | | 50 | 500 | | 50 | 500 | nA |
| Open Loop Gain | $V_{CM} = \frac{V_{CC}}{2}$; $V_{OUT}$ = 0.35 V to 2.35 V | 76 | 80 | | 76 | 80 | | dB |
| | $T_{MIN}$ to $T_{MAX}$ | 74 | | | 74 | | | dB |
| INPUT CHARACTERISTICS | | | | | | | | |
| Common-Mode Input Resistance | | | 40 | | | 40 | | MΩ |
| Differential Input Resistance | | | 280 | | | 280 | | kΩ |
| Input Capacitance | | | 1.6 | | | 1.6 | | pF |
| Input Voltage Range | | | –0.5 to +3.2 | | | –0.5 to +3.2 | | V |
| Input Common-Mode Voltage Range | | | –0.2 to +2.9 | | | –0.2 to +2.9 | | V |
| Common-Mode Rejection Ratio | $V_{CM}$ = 0 V to 2.7 V | 46 | 64 | | 46 | 64 | | dB |
| | $V_{CM}$ = 0 V to 1.55 V | 58 | 74 | | 58 | 74 | | dB |
| Differential Input Voltage | | | | 3.4 | | | 3.4 | V |
| OUTPUT CHARACTERISTICS | | | | | | | | |
| Output Voltage Swing Low | $R_L$ = 10 kΩ | +0.05 | +0.02 | | +0.05 | +0.02 | | V |
| Output Voltage Swing High | | +2.6 | +2.68 | | +2.6 | +2.68 | | V |
| Output Voltage Swing Low | $R_L$ = 1 kΩ | +0.15 | +0.08 | | +0.15 | +0.08 | | V |
| Output Voltage Swing High | | +2.55 | +2.6 | | +2.55 | +2.6 | | V |
| Output Current | | | 15 | | | 15 | | mA |
| Short Circuit Current | Sourcing | | 21 | | | 21 | | mA |
| | Sinking | | –34 | | | –34 | | mA |
| Capacitive Load Drive | G = +2 (See Figure 41) | | 15 | | | 15 | | pF |
| POWER SUPPLY | | | | | | | | |
| Operating Range | | +2.7 | | +12 | +2.7 | | +12 | V |
| Quiescent Current per Amplifier | | | 750 | 1250 | | 750 | 1250 | μA |
| Power Supply Rejection Ratio | $V_S$– = 0 V to –1 V or | | | | | | | |
| | $V_S$+ = +2.7 V to +3.7 V | 75 | 86 | | 75 | 86 | | dB |

Specifications subject to change without notice.

# SPECIFICATIONS

## +5 V Supply (@ $T_A$ = +25°C, $V_S$ = +5 V, $R_L$ = 1 kΩ to +2.5 V, $R_F$ = 2.5 kΩ unless otherwise noted)

| Parameter | Conditions | AD8031A/AD8032A Min | AD8031A/AD8032A Typ | AD8031A/AD8032A Max | AD8031B/AD8032B Min | AD8031B/AD8032B Typ | AD8031B/AD8032B Max | Units |
|---|---|---|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | | | | |
| –3 dB Small Signal Bandwidth | G = +1, $V_O$ < 0.4 V p-p | 54 | 80 | | 54 | 80 | | MHz |
| Slew Rate | G = –1, $V_O$ = 2 V Step | 27 | 32 | | 27 | 32 | | V/µs |
| Settling Time to 0.1% | G = –1, $V_O$ = 2 V Step, $C_L$ = 10 pF | | 125 | | | 125 | | ns |
| DISTORTION/NOISE PERFORMANCE | | | | | | | | |
| Total Harmonic Distortion | $f_C$ = 1 MHz, $V_O$ = 2 V p-p, G = +2 | | –62 | | | –62 | | dBc |
| | $f_C$ = 100 kHz, $V_O$ = 2 V p-p, G = +2 | | –86 | | | –86 | | dBc |
| Input Voltage Noise | f = 1 kHz | | 15 | | | 15 | | nV/√Hz |
| Input Current Noise | f = 100 kHz | | 2.4 | | | 2.4 | | pA/√Hz |
| | f = 1 kHz | | 5 | | | 5 | | pA/√Hz |
| Differential Gain | $R_L$ = 1 kΩ | | 0.17 | | | 0.17 | | % |
| Differential Phase | $R_L$ = 1 kΩ | | 0.11 | | | 0.11 | | Degrees |
| Crosstalk (AD8032 Only) | f = 5 MHz | | –60 | | | –60 | | dB |
| DC PERFORMANCE | | | | | | | | |
| Input Offset Voltage | $V_{CM} = \frac{V_{CC}}{2}$; $V_{OUT}$ = 2.5 V | | ±1 | ±6 | | ±0.5 | ±1.5 | mV |
| | $T_{MIN}$ to $T_{MAX}$ | | ±6 | ±10 | | ±1.6 | ±2.5 | mV |
| Offset Drift | $V_{CM} = \frac{V_{CC}}{2}$; $V_{OUT}$ = 2.5 V | | 5 | | | 5 | | µV/°C |
| Input Bias Current | $V_{CM} = \frac{V_{CC}}{2}$; $V_{OUT}$ = 2.5 V | | 0.45 | 1.2 | | 0.45 | 1.2 | µA |
| | $T_{MIN}$ to $T_{MAX}$ | | | 2.0 | | | 2.0 | µA |
| Input Offset Current | | | 50 | 350 | | 50 | 250 | nA |
| Open Loop Gain | $V_{CM} = \frac{V_{CC}}{2}$; $V_{OUT}$ = 1.5 V to 3.5 V | 76 | 82 | | 76 | 82 | | dB |
| | $T_{MIN}$ to $T_{MAX}$ | 74 | | | 74 | | | dB |
| INPUT CHARACTERISTICS | | | | | | | | |
| Common-Mode Input Resistance | | | 40 | | | 40 | | MΩ |
| Differential Input Resistance | | | 280 | | | 280 | | kΩ |
| Input Capacitance | | | 1.6 | | | 1.6 | | pF |
| Input Voltage Range | | | –0.5 to +5.5 | | | –0.5 to +5.5 | | V |
| Input Common-Mode Voltage Range | | | –0.2 to +5.2 | | | –0.2 to +5.2 | | V |
| Common-Mode Rejection Ratio | $V_{CM}$ = 0 V to 5 V | 56 | 70 | | 56 | 70 | | dB |
| | $V_{CM}$ = 0 V to 3.8 V | 66 | 80 | | 66 | 80 | | dB |
| Differential Input Voltage | | | | 3.4 | | | 3.4 | V |
| OUTPUT CHARACTERISTICS | | | | | | | | |
| Output Voltage Swing Low | $R_L$ = 10 kΩ | +0.05 | +0.02 | | +0.05 | +0.02 | | V |
| Output Voltage Swing High | | +4.95 | +4.98 | | +4.95 | +4.98 | | V |
| Output Voltage Swing Low | $R_L$ = 1 kΩ | +0.2 | +0.1 | | +0.2 | +0.1 | | V |
| Output Voltage Swing High | | +4.8 | +4.9 | | +4.8 | +4.9 | | V |
| Output Current | | | 15 | | | 15 | | mA |
| Short Circuit Current | Sourcing | | 28 | | | 28 | | mA |
| | Sinking | | –46 | | | –46 | | mA |
| Capacitive Load Drive | G = +2 (See Figure 41) | | 15 | | | 15 | | pF |
| POWER SUPPLY | | | | | | | | |
| Operating Range | | +2.7 | | +12 | +2.7 | | +12 | V |
| Quiescent Current per Amplifier | | | 800 | 1400 | | 800 | 1400 | µA |
| Power Supply Rejection Ratio | $V_S$– = 0 V to –1 V or $V_S$+ = +5 V to +6 V | 75 | 86 | | 75 | 86 | | dB |

Specifications subject to change without notice.

# AD8031/AD8032–SPECIFICATIONS

## ±5 V Supply (@ $T_A$ = +25°C, $V_S$ = ±5 V, $R_L$ = 1 kΩ to 0 V, $R_F$ = 2.5 kΩ unless otherwise noted)

| Parameter | Conditions | AD8031A/AD8032A Min | AD8031A/AD8032A Typ | AD8031A/AD8032A Max | AD8031B/AD8032B Min | AD8031B/AD8032B Typ | AD8031B/AD8032B Max | Units |
|---|---|---|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | | | | |
| –3 dB Small Signal Bandwidth | G = +1, $V_O$ < 0.4 V p-p | 54 | 80 | | 54 | 80 | | MHz |
| Slew Rate | G = –1, $V_O$ = 2 V Step | 30 | 35 | | 30 | 35 | | V/µs |
| Settling Time to 0.1% | G = –1, $V_O$ = 2 V Step, $C_L$ = 10 pF | | 125 | | | 125 | | ns |
| DISTORTION/NOISE PERFORMANCE | | | | | | | | |
| Total Harmonic Distortion | $f_C$ = 1 MHz, $V_O$ = 2 V p-p, G = +2 | | –62 | | | –62 | | dBc |
| | $f_C$ = 100 kHz, $V_O$ = 2 V p-p, G = +2 | | –86 | | | –86 | | dBc |
| Input Voltage Noise | f = 1 kHz | | 15 | | | 15 | | nV/√Hz |
| Input Current Noise | f = 100 kHz | | 2.4 | | | 2.4 | | pA/√Hz |
| | f = 1 kHz | | 5 | | | 5 | | pA/√Hz |
| Differential Gain | $R_L$ = 1 kΩ | | 0.15 | | | 0.15 | | % |
| Differential Phase | $R_L$ = 1 kΩ | | 0.15 | | | 0.15 | | Degrees |
| Crosstalk (AD8032 Only) | f = 5 MHz | | –60 | | | –60 | | dB |
| DC PERFORMANCE | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0 V; $V_{OUT}$ = 0 V | | ±1 | ±6 | | ±0.5 | ±1.5 | mV |
| | $T_{MIN}$ to $T_{MAX}$ | | ±6 | ±10 | | ±1.6 | ±2.5 | mV |
| Offset Drift | $V_{CM}$ = 0 V; $V_{OUT}$ = 0 V | | 5 | | | 5 | | µV/°C |
| Input Bias Current | $V_{CM}$ = 0 V; $V_{OUT}$ = 0 V | | 0.45 | 1.2 | | 0.45 | 1.2 | µA |
| | $T_{MIN}$ to $T_{MAX}$ | | | 2.0 | | | 2.0 | µA |
| Input Offset Current | | | 50 | 350 | | 50 | 250 | nA |
| Open Loop Gain | $V_{CM}$ = 0 V; $V_{OUT}$ = ±2 V | 76 | 80 | | 76 | 80 | | dB |
| | $T_{MIN}$ to $T_{MAX}$ | 74 | | | 74 | | | dB |
| INPUT CHARACTERISTICS | | | | | | | | |
| Common-Mode Input Resistance | | | 40 | | | 40 | | MΩ |
| Differential Input Resistance | | | 280 | | | 280 | | kΩ |
| Input Capacitance | | | 1.6 | | | 1.6 | | pF |
| Input Voltage Range | | | –5.5 to +5.5 | | | –5.5 to +5.5 | | V |
| Input Common-Mode Voltage Range | | | –5.2 to +5.2 | | | –5.2 to +5.2 | | V |
| Common-Mode Rejection Ratio | $V_{CM}$ = –5 V to +5 V | 60 | 80 | | 60 | 80 | | dB |
| | $V_{CM}$ = –5 V to +3.5 V | 66 | 90 | | 66 | 90 | | dB |
| Differential/Input Voltage | | | | 3.4 | | | 3.4 | V |
| OUTPUT CHARACTERISTICS | | | | | | | | |
| Output Voltage Swing Low | $R_L$ = 10 kΩ | –4.94 | –4.98 | | –4.94 | –4.98 | | V |
| Output Voltage Swing High | | +4.94 | +4.98 | | +4.94 | +4.98 | | V |
| Output Voltage Swing Low | $R_L$ = 1 kΩ | –4.7 | –4.85 | | –4.7 | –4.85 | | V |
| Output Voltage Swing High | | +4.7 | +4.75 | | +4.7 | +4.75 | | V |
| Output Current | | | 15 | | | 15 | | mA |
| Short Circuit Current | Sourcing | | 35 | | | 35 | | mA |
| | Sinking | | –50 | | | –50 | | mA |
| Capacitive Load Drive | G = +2 (See Figure 41) | | 15 | | | 15 | | pF |
| POWER SUPPLY | | | | | | | | |
| Operating Range | | ±1.35 | | ±6 | ±1.35 | | ±6 | V |
| Quiescent Current per Amplifier | | | 900 | 1600 | | 900 | 1600 | µA |
| Power Supply Rejection Ratio | $V_S$– = –5 V to –6 V or | | | | | | | |
| | $V_S$+ = +5 V to +6 V | 76 | 86 | | 76 | 86 | | dB |

Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . +12.6 V
Internal Power Dissipation[2]
Plastic DIP Package (N) . . . . . 1.3 Watts
Small Outline Package (R) . . . . . 0.8 Watts
µSOIC (RM) . . . . . 0.6 Watts
SOT-23-5 (RT) . . . . . 0.5 Watts
Input Voltage (Common-Mode) . . . . . $\pm V_S \pm 0.5$ V
Differential Input Voltage . . . . . ±3.4 V
Output Short Circuit Duration
. . . . . Observe Power Derating Curves
Storage Temperature Range (N, R, RM, RT)
. . . . . –65°C to +125°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for the device in free air:
8-Lead Plastic DIP Package: $\theta_{JA}$ = 90°C/W.
8-Lead SOIC Package: $\theta_{JA}$ = 155°C/W.
8-Lead µSOIC Package: $\theta_{JA}$ = 200°C/W.
5-Lead SOT-23-5 Package: $\theta_{JA}$ = 240°C/W.

## MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8031/AD8032 are limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately +150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.

While the AD8031/AD8032 are internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves shown in Figure 2.

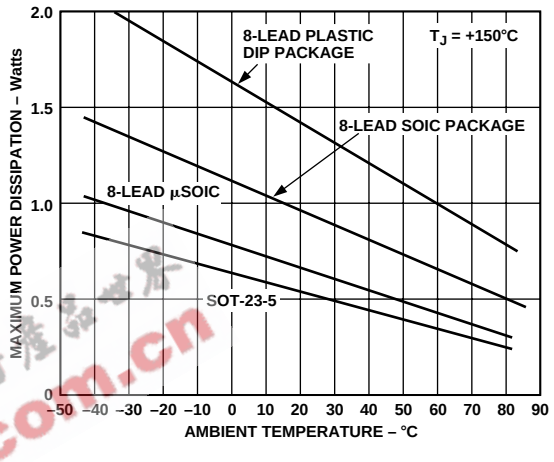



*Figure 2. Maximum Power Dissipation vs. Temperature*

## ORDERING GUIDE

| Model | Temperature Range | Package Descriptions | Package Options | Brand Code |
|---|---|---|---|---|
| AD8031AN | –40°C to +85°C | 8-Lead Plastic DIP | N-8 | |
| AD8031AR | –40°C to +85°C | 8-Lead SOIC | SO-8 | |
| AD8031AR-REEL | –40°C to +85°C | 13" Tape and Reel | SO-8 | |
| AD8031AR-REEL7 | –40°C to +85°C | 7" Tape and Reel | SO-8 | |
| AD8031ART-REEL | –40°C to +85°C | 13" Tape and Reel | RT-5 | H0A |
| AD8031ART-REEL7 | –40°C to +85°C | 7" Tape and Reel | RT-5 | H0A |
| AD8031BN | –40°C to +85°C | 8-Lead Plastic DIP | N-8 | |
| AD8031BR | –40°C to +85°C | 8-Lead SOIC | SO-8 | |
| AD8031BR-REEL | –40°C to +85°C | 13" Tape and Reel | SO-8 | |
| AD8031BR-REEL7 | –40°C to +85°C | 7" Tape and Reel | SO-8 | |
| AD8032AN | –40°C to +85°C | 8-Lead Plastic DIP | N-8 | |
| AD8032AR | –40°C to +85°C | 8-Lead SOIC | SO-8 | |
| AD8032AR-REEL | –40°C to +85°C | 13" Tape and Reel | SO-8 | |
| AD8032AR-REEL7 | –40°C to +85°C | 7" Tape and Reel | SO-8 | |
| AD8032ARM | –40°C to +85°C | 8-Lead µSOIC | RM-8 | H9A |
| AD8032ARM-REEL | –40°C to +85°C | 13" Tape and Reel | RM-8 | H9A |
| AD8032ARM-REEL7 | –40°C to +85°C | 7" Tape and Reel | RM-8 | H9A |
| AD8032BN | –40°C to +85°C | 8-Lead Plastic DIP | N-8 | |
| AD8032BR | –40°C to +85°C | 8-Lead SOIC | SO-8 | |
| AD8032BR-REEL | –40°C to +85°C | 13" Tape and Reel | SO-8 | |
| AD8032BR-REEL7 | –40°C to +85°C | 7" Tape and Reel | SO-8 | |

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8031/AD8032 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# AD8031/AD8032–Typical Performance Characteristics

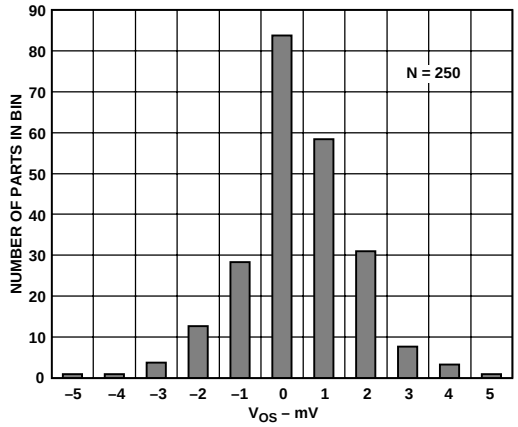



*Figure 3. Typical $V_{OS}$ Distribution @ $V_S$ = 5 V*

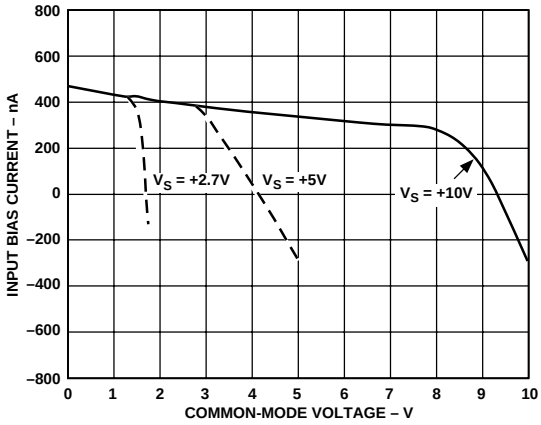



*Figure 6. Input Bias Current vs. Common-Mode Voltage*

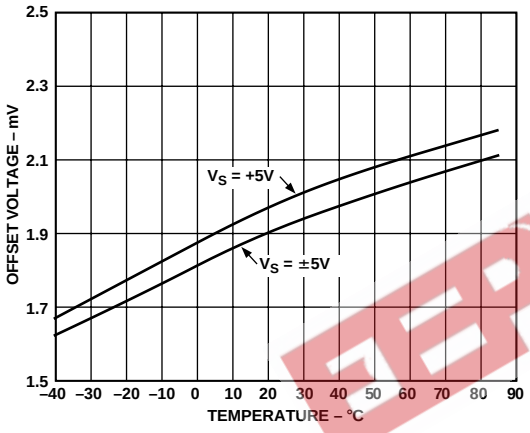



*Figure 4. Input Offset Voltage vs. Temperature*

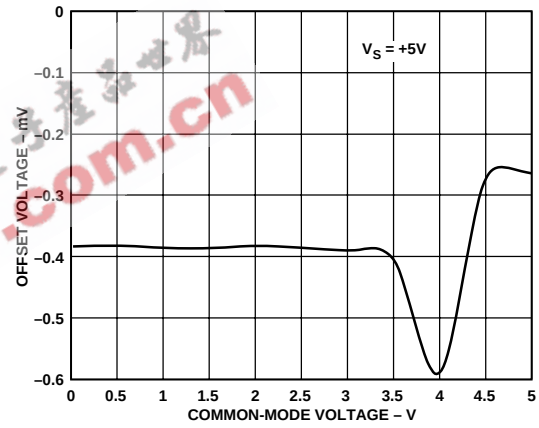



*Figure 7. $V_{OS}$ vs. Common-Mode Voltage*

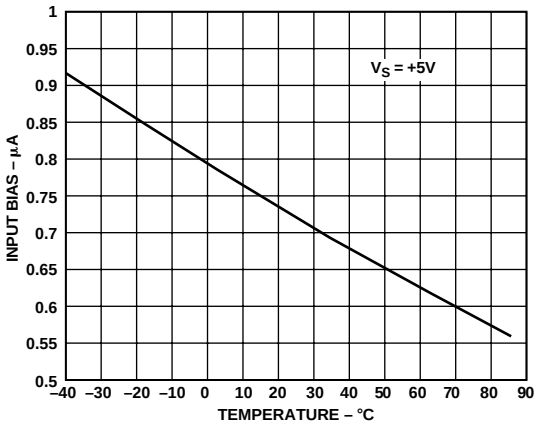



*Figure 5. Input Bias Current vs. Temperature*

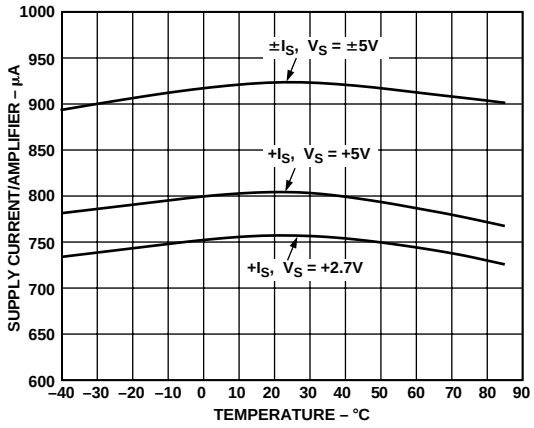



*Figure 8. Supply Current vs. Temperature*

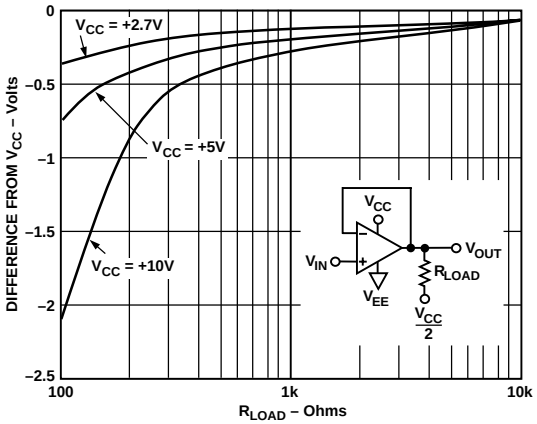



Figure 9. +Output Saturation Voltage vs. $R_{LOAD}$ @ +85°C

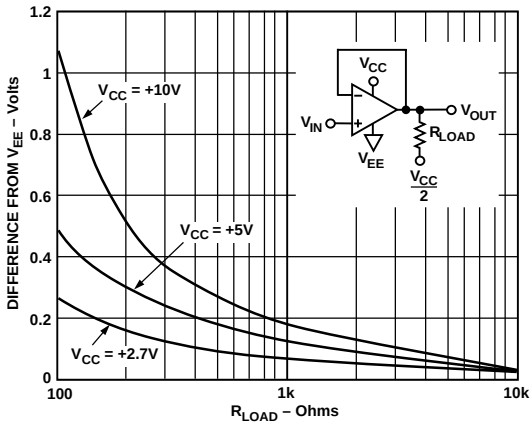



Figure 12. –Output Saturation Voltage vs. $R_{LOAD}$ @ +85°C

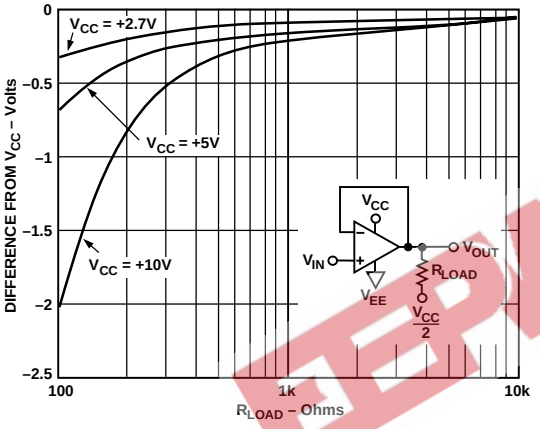



Figure 10. +Output Saturation Voltage vs. $R_{LOAD}$ @ +25°C

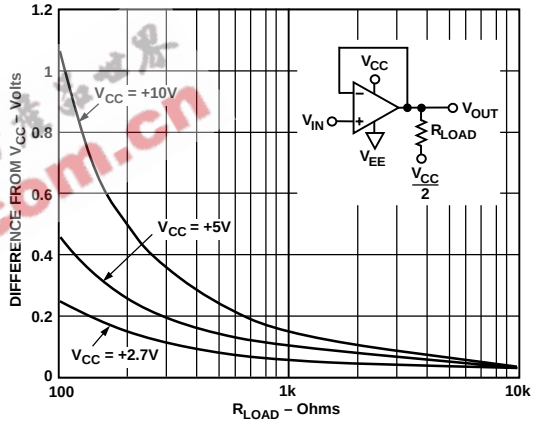



Figure 13. –Output Saturation Voltage vs. $R_{LOAD}$ @ +25°C

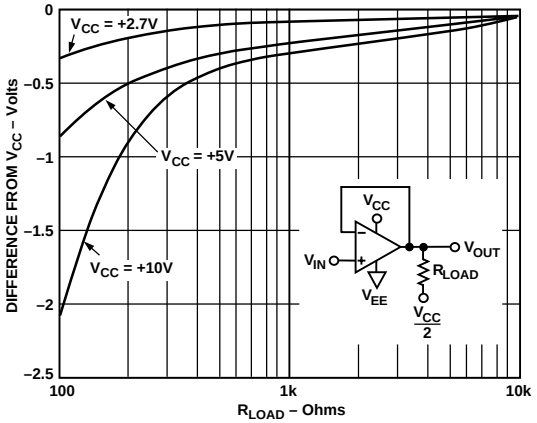



Figure 11. +Output Saturation Voltage vs. $R_{LOAD}$ @ –40°C

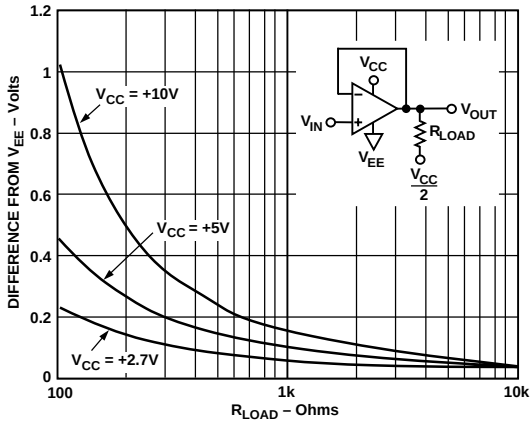



Figure 14. –Output Saturation Voltage vs. $R_{LOAD}$ @ –40°C

# AD8031/AD8032–Typical Performance Characteristics

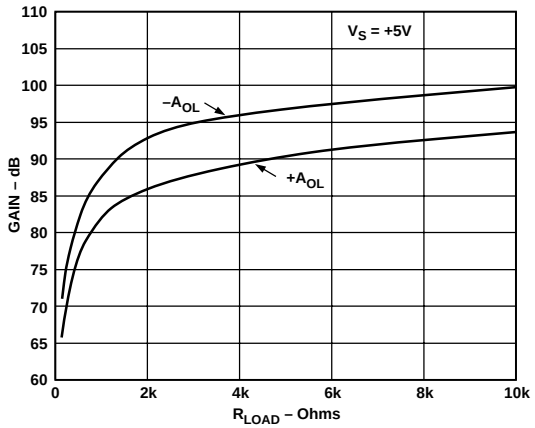



Figure 15. Open-Loop Gain ($A_{OL}$) vs. $R_{LOAD}$

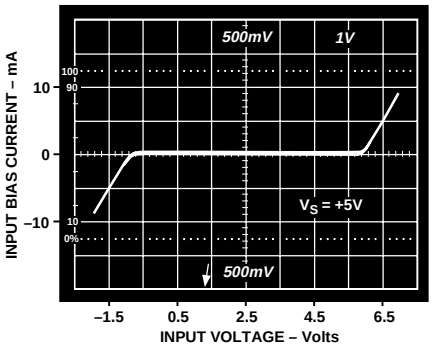



Figure 18. Differential Input Overvoltage I-V Characteristics

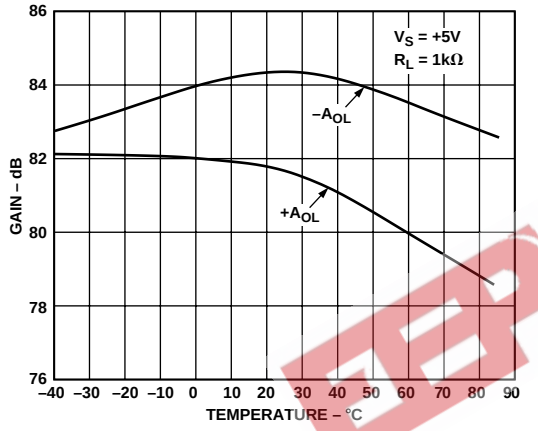



Figure 16. Open-Loop Gain ($A_{OL}$) vs. Temperature

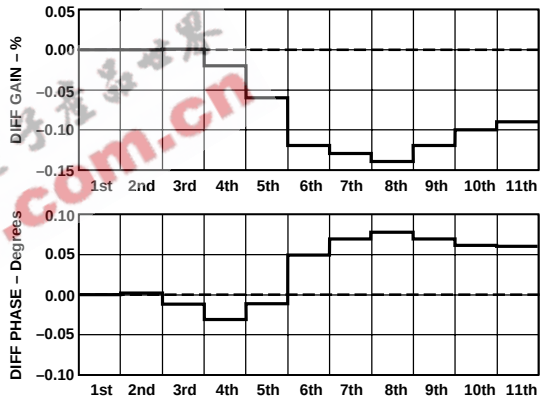



Figure 19. Differential Gain and Phase @ $V_S = \pm 5$ V; $R_L$ = 1 kΩ

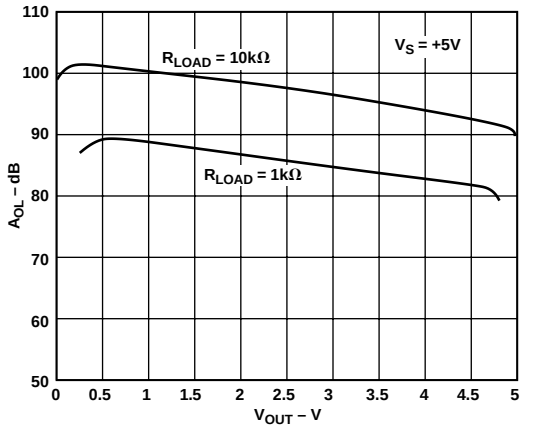



Figure 17. Open-Loop Gain ($A_{OL}$) vs. $V_{OUT}$

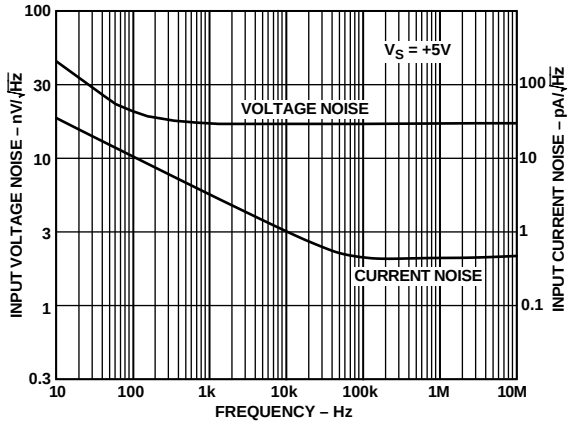



Figure 20. Input Voltage Noise vs. Frequency

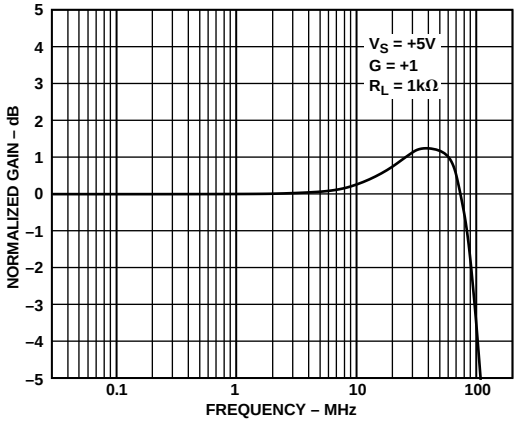



Figure 21. Unity Gain , –3 dB Bandwidth

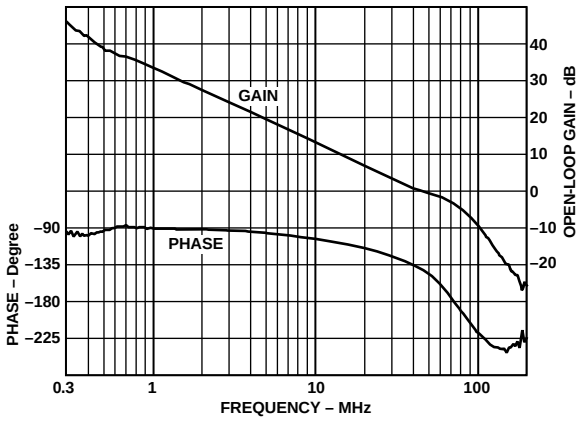



Figure 24. Open-Loop Frequency Response

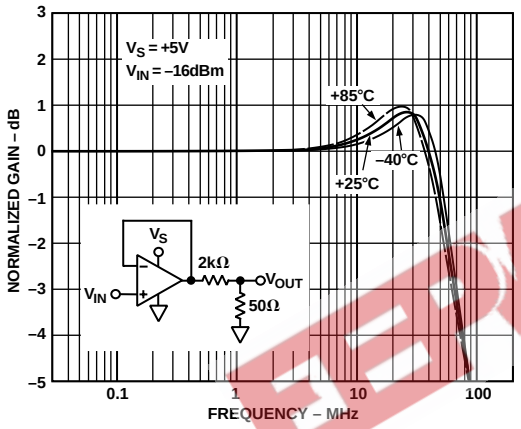



Figure 22. Closed-Loop Gain vs. Temperature

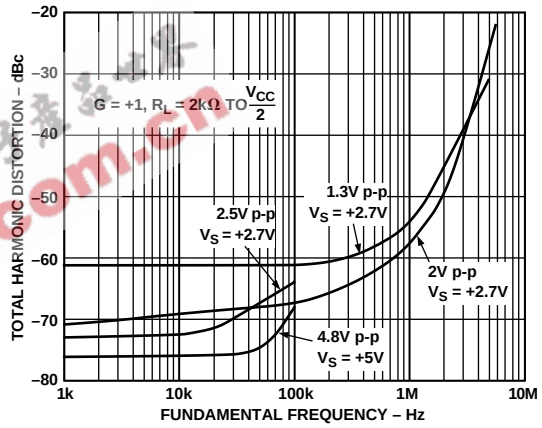



Figure 25. Total Harmonic Distortion vs. Frequency; G = +1

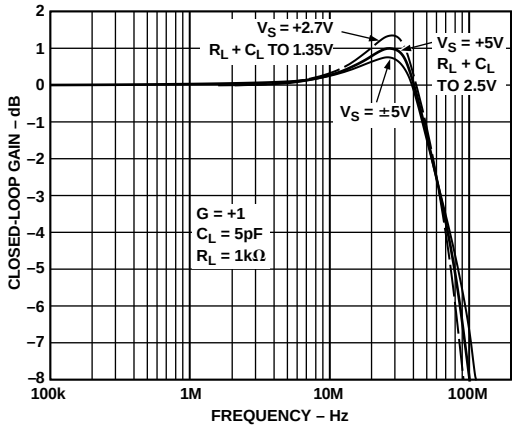



Figure 23. Closed-Loop Gain vs. Supply Voltage

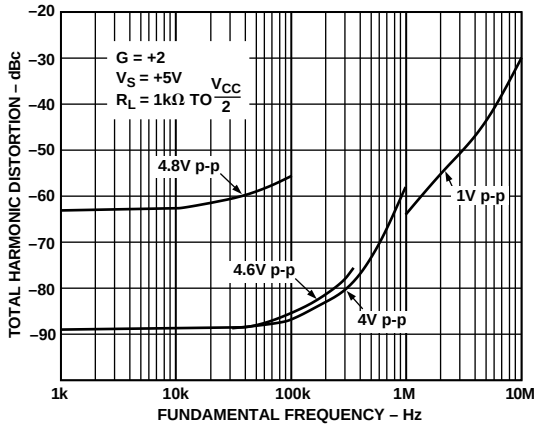



Figure 26. Total Harmonic Distortion vs. Frequency; G = +2

# AD8031/AD8032–Typical Performance Characteristics

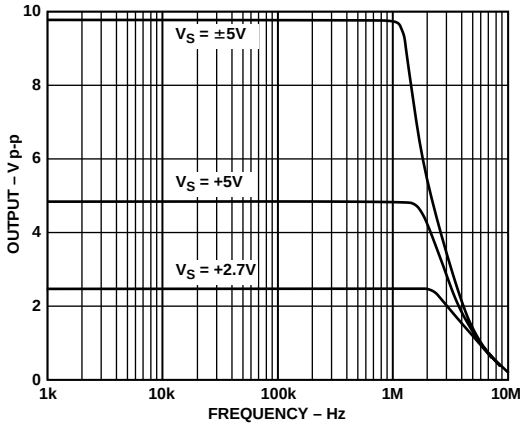



Figure 27. Large Signal Response

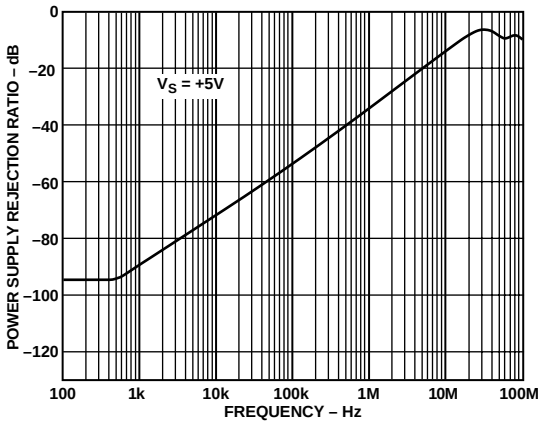



Figure 30. PSRR vs. Frequency

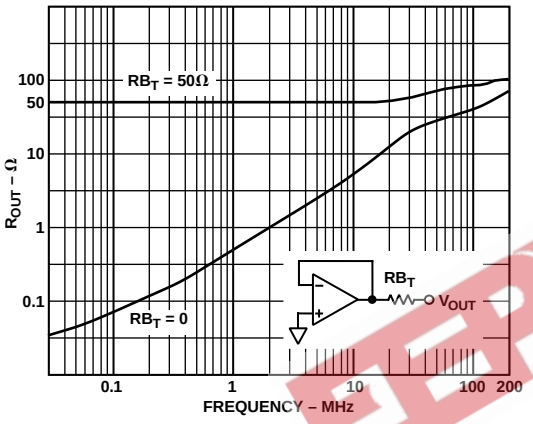



Figure 28. $R_{OUT}$ vs. Frequency

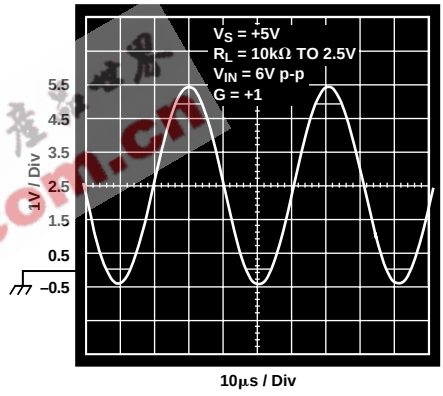



Figure 31. Output Voltage

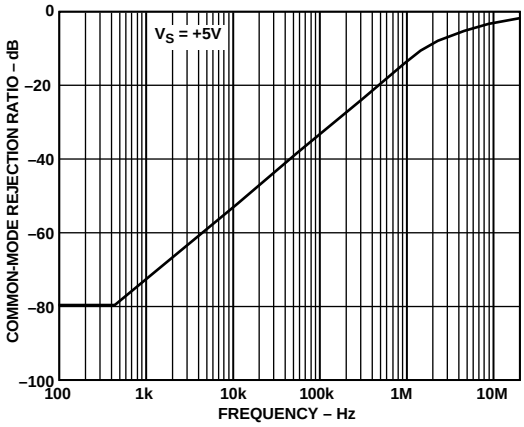



Figure 29. CMRR vs. Frequency

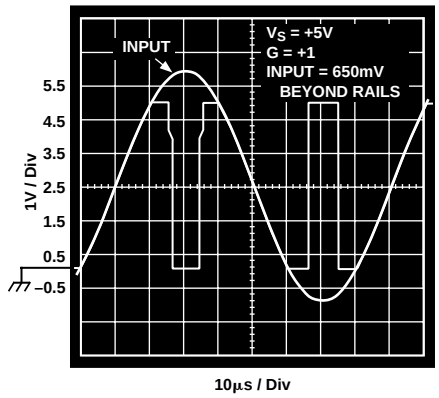



Figure 32. Output Voltage Phase Reversal Behavior

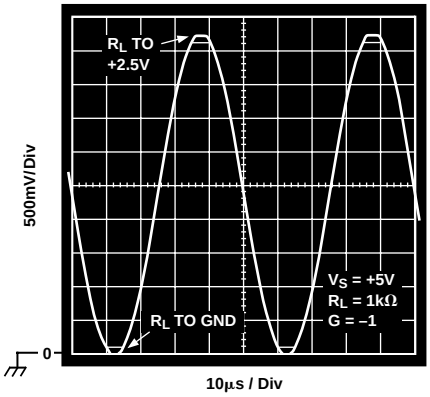



Figure 33. Output Swing

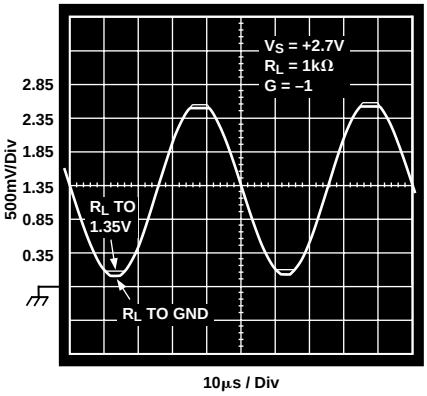



Figure 35. Output Swing

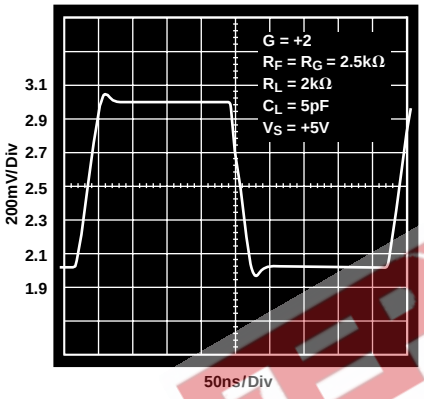



Figure 34. 1 V Step Response

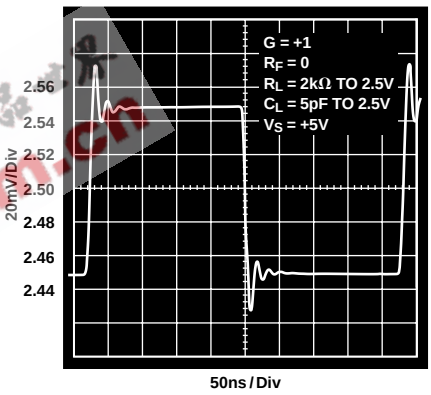



Figure 36. 100 mV Step Response

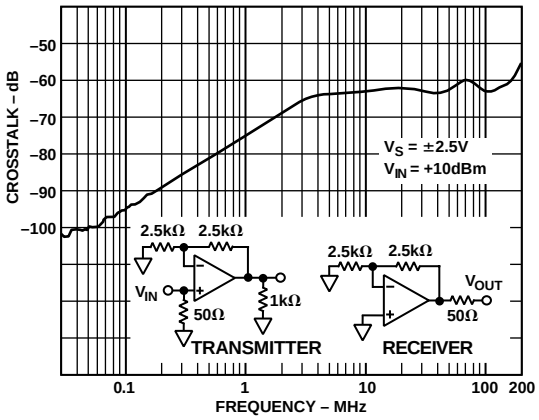



Figure 37. Crosstalk vs. Frequency

## THEORY OF OPERATION

The AD8031/AD8032 are single and dual versions of high speed, low power voltage feedback amplifiers featuring an innovative architecture that maximizes the dynamic range capability on the inputs and outputs. Linear input common-mode range exceeds either supply voltage by 200 mV, and the amplifiers show no phase reversal up to 500 mV beyond supply. The output swings to within 20 mV of either supply when driving a light load; 300 mV when driving up to 5 mA.

Fabricated on Analog Devices' XFCB, a 4 GHz dielectrically isolated fully complementary bipolar process, the amplifier provides an impressive 80 MHz bandwidth when used as a follower and 30 V/µs slew rate at only 800 µA supply current. Careful design allows the amplifier to operate with a supply voltage as low as 2.7 volts.

### Input Stage Operation

A simplified schematic of the input stage appears in Figure 38. For common-mode voltages up to 1.1 volts within the positive supply, (0 V to 3.9 V on a single 5 V supply) tail current I2 flows through the PNP differential pair, Q13 and Q17. Q5 is cut off; no bias current is routed to the parallel NPN differential pair Q2 and Q3. As the common-mode voltage is driven within 1.1 V of the positive supply, Q5 turns on and routes the tail current away from the PNP pair and to the NPN pair. During this transition region, the amplifier's input current will change magnitude and direction. Reusing the same tail current ensures that the input stage has the same transconductance (which determines the amplifier's gain and bandwidth) in both regions of operation.

Switching to the NPN pair as the common-mode voltage is driven beyond 1 V within the positive supply allows the amplifier to provide useful operation for signals at either end of the supply voltage range and eliminates the possibility of phase reversal for input signals up to 500 mV beyond either power supply. Offset voltage will also change to reflect the offset of the input pair in control. The transition region is small, on the order of 180 mV. These sudden changes in the dc parameters of the input stage can produce glitches that will adversely affect distortion.

### Overdriving the Input Stage

Sustained input differential voltages greater than 3.4 volts should be avoided as the input transistors may be damaged. Input clamp diodes are recommended if the possibility of this condition exists.

The voltages at the collectors of the input pairs are set to 200 mV from the power supply rails. This allows the amplifier to remain in linear operation for input voltages up to 500 mV beyond the supply voltages. Driving the input common-mode voltage beyond that point will forward bias the collector junction of the input transistor, resulting in phase reversal. Sustaining this condition for any length of time should be avoided as it is easy to exceed the maximum allowed input differential voltage when the amplifier is in phase reversal.

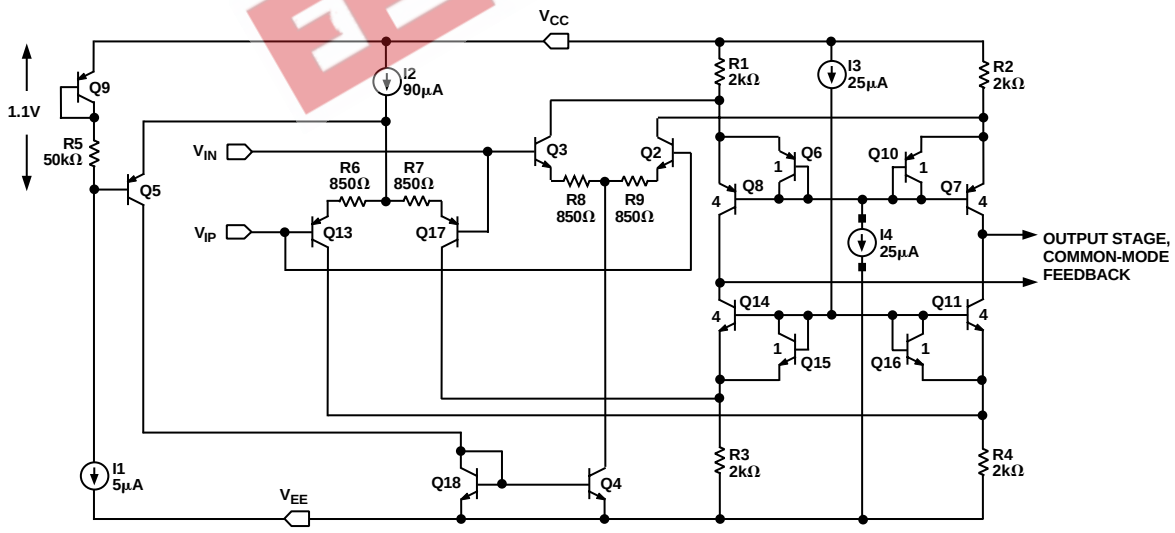



*Figure 38. Simplified Schematic of AD8031 Input Stage*

**Output Stage, Open-Loop Gain and Distortion vs. Clearance from Power Supply**

The AD8031 features a rail-to-rail output stage. The output transistors operate as common emitter amplifiers, providing the output drive current as well as a large portion of the amplifier's open-loop gain.

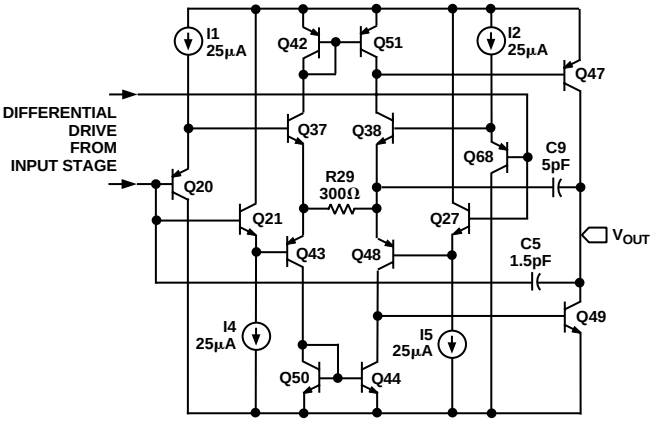



*Figure 39. Output Stage Simplified Schematic*

The output voltage limit depends on how much current the output transistors are required to source or sink. For applications with very low drive requirements (a unity gain follower driving another amplifier input, for instance), the AD8031 typically swings within 20 mV of either voltage supply. As the required current load increases, the saturation output voltage will increase linearly as $I_{LOAD} \times R_C$, where $I_{LOAD}$ is the required load current and $R_C$ is the output transistor collector resistance. For the AD8031, the collector resistances for both output transistors are typically 25 Ω. As the current load exceeds the rated output current of 15 mA, the amount of base drive current required to drive the output transistor into saturation will reach its limit, and the amplifier's output swing will rapidly decrease.

The open-loop gain of the AD8031 decreases approximately linearly with load resistance and also depends on the output voltage. Open-loop gain stays constant to within 250 mV of the positive power supply, 150 mV of the negative power supply and then decreases as the output transistors are driven further into saturation.

The distortion performance of the AD8031/AD8032 amplifiers differs from conventional amplifiers. Typically an amplifier's distortion performance degrades as the output voltage amplitude increases.

Used as a unity gain follower, the AD8031/AD8032 output will exhibit more distortion in the peak output voltage region around $V_{CC}$ –0.7 V. This unusual distortion characteristic is caused by the input stage architecture and is discussed in detail in the section covering "Input Stage Operation."

**Output Overdrive Recovery**

Output overdrive of an amplifier occurs when the amplifier attempts to drive the output voltage to a level outside its normal range. After the overdrive condition is removed, the amplifier must recover to normal operation in a reasonable amount of time. As shown in Figure 40, the AD8031/AD8032 recover within 100 ns from negative overdrive and within 80 ns from positive overdrive.

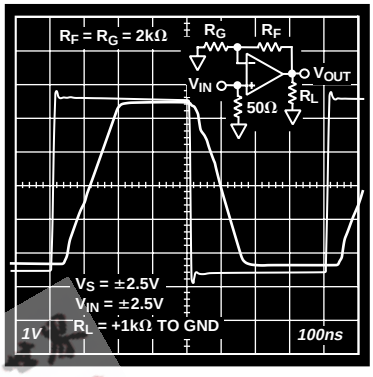



*Figure 40. Overdrive Recovery*

**Driving Capacitive Loads**

Capacitive loads interact with an op amp's output impedance to create an extra delay in the feedback path. This reduces circuit stability, and can cause unwanted ringing and oscillation. A given value of capacitance causes much less ringing when the amplifier is used with a higher noise gain.

The capacitive load drive of the AD8031/AD8032 can be increased by adding a low valued resistor in series with the capacitive load. Introducing a series resistor tends to isolate the capacitive load from the feedback loop, thereby, diminishing its influence. Figure 41 shows the effects of a series resistor on capacitive drive for varying voltage gains. As the closed-loop gain is increased, the larger phase margin allows for larger capacitive loads with less overshoot. Adding a series resistor at lower closed-loop gains accomplishes the same effect. For large capacitive loads, the frequency response of the amplifier will be dominated by the roll-off of the series resistor and capacitive load.

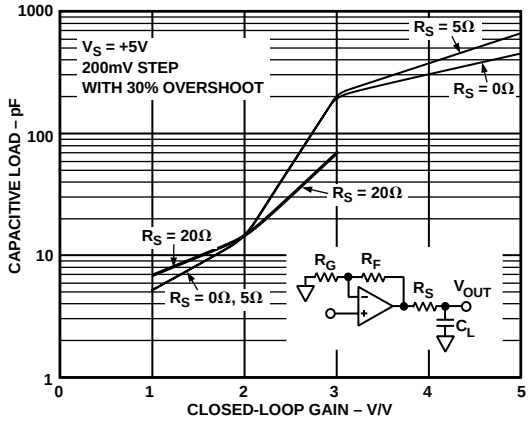



*Figure 41. Capacitive Load Drive vs. Closed-Loop Gain*

## APPLICATIONS

### A 2 MHz Single Supply Biquad Bandpass Filter

Figure 42 shows a circuit for a single supply biquad bandpass filter with a center frequency of 2 MHz. A 2.5 V bias level is easily created by connecting the noninverting inputs of all three op amps to a resistor divider consisting of two 1 kΩ resistors connected between +5 V and ground. This bias point is also decoupled to ground with a 0.1 µF capacitor. The frequency response of the filter is shown in Figure 43.

In order to maintain an accurate center frequency, it is essential that the op amp has sufficient loop gain at 2 MHz. This requires the choice of an op amp with a significantly higher unity gain crossover frequency. The unity gain crossover frequency of the AD8031/AD8032 is 40 MHz. Multiplying the open-loop gain by the feedback factors of the individual op amp circuits yields the loop gain for each gain stage. From the feedback networks of the individual op amp circuits, we can see that each op amp has a loop gain of at least 21 dB. This level is high enough to ensure that the center frequency of the filter is not affected by the op amp's bandwidth. If, for example, an op amp with a gain bandwidth product of 10 MHz was chosen in this application, the resulting center frequency would shift by 20% to 1.6 MHz.

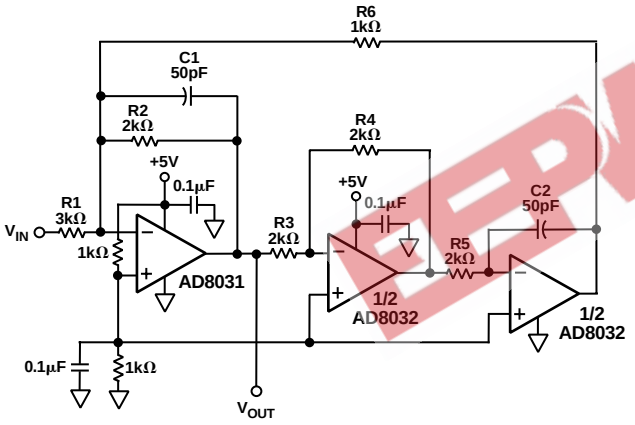



*Figure 42. A 2 MHz Biquad Bandpass Filter Using AD8031/AD8032*

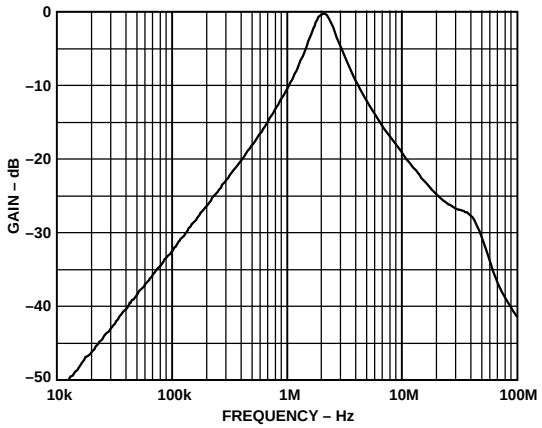



*Figure 43. Frequency Response of 2 MHz Bandpass Filter*

### High Performance Single Supply Line Driver

Even though the AD8031/AD8032 swing close to both rails, the AD8031 has optimum distortion performance when the signal has a common-mode level half way between the supplies and when there is about 500 mV of headroom to each rail. If low distortion is required in single supply applications for signals that swing close to ground, an emitter follower circuit can be used at the op amp output.

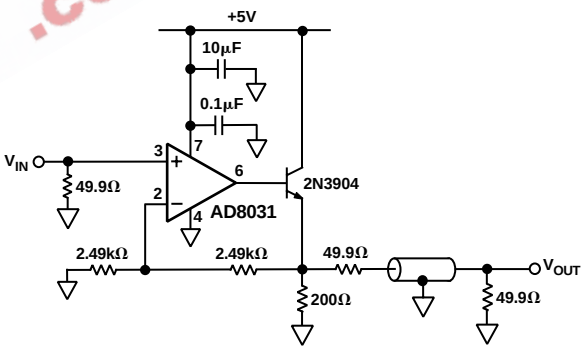



*Figure 44. Low Distortion Line Driver for Single Supply Ground Referenced Signals*

Figure 44 shows the AD8031 configured as a single supply gain-of-2 line driver. With the output driving a back terminated 50 Ω line, the overall gain from $V_{IN}$ to $V_{OUT}$ is unity. In addition to minimizing reflections, the 50 Ω back termination resistor protects the transistor from damage if the cable is short circuited. The emitter follower, which is inside the feedback loop, ensures that the output voltage from the AD8031 stays about 700 mV above ground. Using this circuit, very low distortion is attainable even when the output signal swings to within 50 mV of ground. The circuit was tested at 500 kHz and 2 MHz. Figures 45 and 46 show the output signal swing and frequency spectrum at 500 kHz. At this frequency, the output signal (at $V_{OUT}$), which has a peak-to-peak swing of 1.95 V (50 mV to 2 V), has a THD of –68 dB (SFDR = –77 dB).

Figures 47 and 48 show the output signal swing and frequency spectrum at 2 MHz. As expected, there is some degradation in signal quality at the higher frequency. When the output signal has a peak-to-peak swing of 1.45 V (swinging from 50 mV to 1.5 V), the THD is –55 dB (SFDR = –60 dB).

This circuit could also be used to drive the analog input of a single supply high speed ADC whose input voltage range is referenced to ground (e.g., 0 V to 2 V or 0 V to 4 V). In this case, a back termination resistor is not necessary (assuming a short physical distance from transistor to ADC), so the emitter of the external transistor would be connected directly to the ADC input. The available output voltage swing of the circuit would, therefore be doubled.

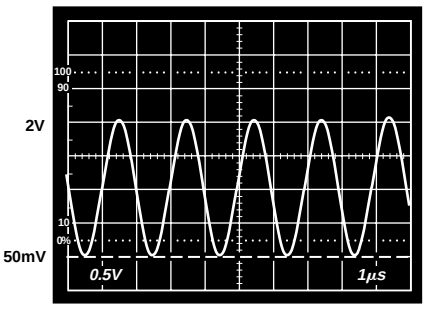



*Figure 45. Output Signal Swing of Low Distortion Line Driver at 500 kHz*

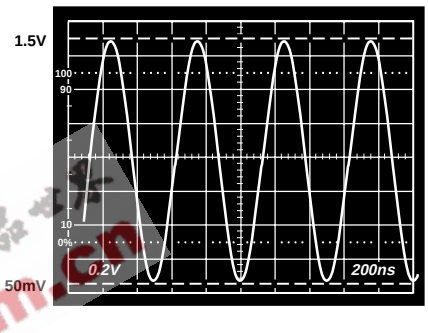



*Figure 47. Output Signal Swing of Low Distortion Line Driver at 2 MHz*

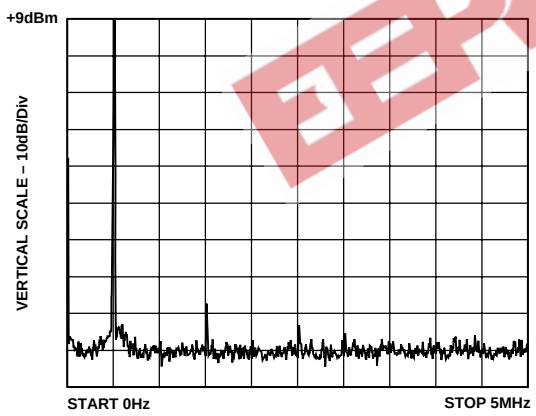



*Figure 46. THD of Low Distortion Line Driver at 500 kHz*

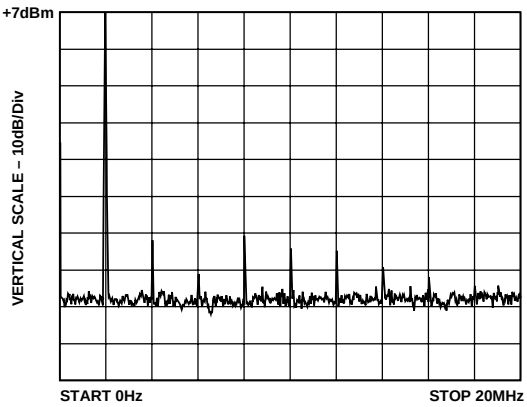
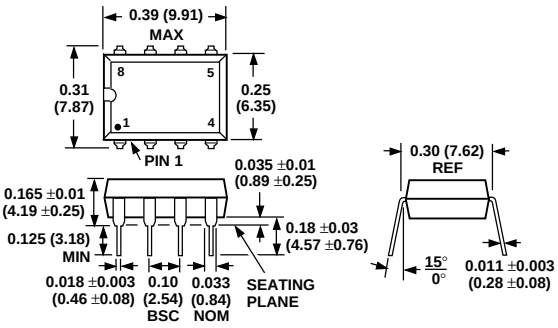



*Figure 48. THD of Low Distortion Line Driver at 2 MHz*

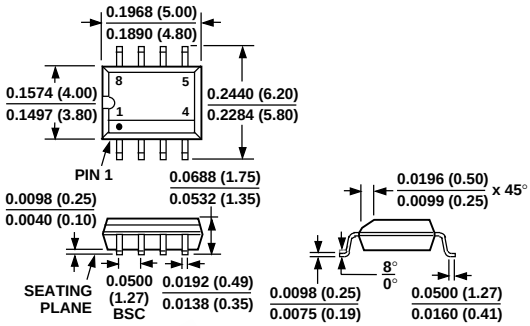
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

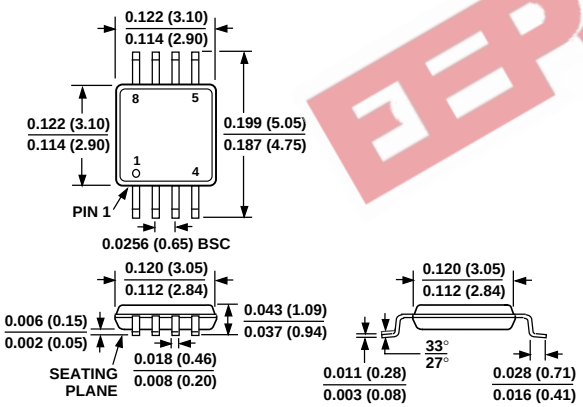
### 8-Lead Plastic DIP (N-8)




### 8-Lead Plastic SOIC (SO-8)




### 8-Lead µSOIC (RM-8)




### 5-Lead Plastic Surface Mount (SOT-23) (RT-5)