

# SN54LS373, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374

## OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

SDLS165B – OCTOBER 1975 – REVISED AUGUST 2002

- Choice of Eight Latches or Eight D-Type Flip-Flops in a Single Package
- 3-State Bus-Driving Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Clock-Enable Input Has Hysteresis to Improve Noise Rejection ('S373 and 'S374)
- P-N-P Inputs Reduce DC Loading on Data Lines ('S373 and 'S374)

### description

These 8-bit registers feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The high-impedance 3-state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pullup components. These devices are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

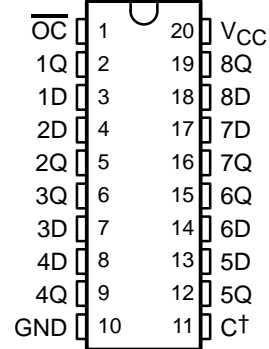
The eight latches of the 'LS373 and 'S373 are transparent D-type latches, meaning that while the enable (C or CLK) input is high, the Q outputs follow the data (D) inputs. When C or CLK is taken low, the output is latched at the level of the data that was set up.

The eight flip-flops of the 'LS374 and 'S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic states that were set up at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines of the 'S373 and 'S374 devices simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output-control (OC) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

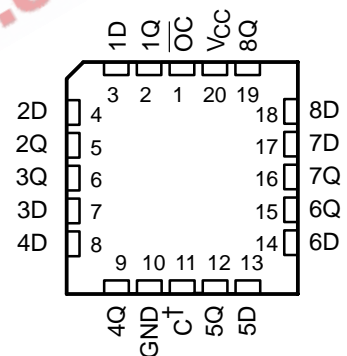
OC does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered, even while the outputs are off.

SN54LS373, SN54LS374, SN54S373,  
SN54S374 . . . J OR W PACKAGE  
SN74LS373, SN74S374 . . . DW, N, OR NS PACKAGE  
SN74LS374 . . . DB, DW, N, OR NS PACKAGE  
SN74S373 . . . DW OR N PACKAGE  
(TOP VIEW)



† C for 'LS373 and 'S373; CLK for 'LS374 and 'S374.

SN54LS373, SN54LS374, SN54S373,  
SN54S374 . . . FK PACKAGE  
(TOP VIEW)



† C for 'LS373 and 'S373; CLK for 'LS374 and 'S374.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**SN54LS373, SN54LS374, SN54S373, SN54S374,  
SN74LS373, SN74LS374, SN74S373, SN74S374  
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS**

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**ORDERING INFORMATION**

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
0°C to 70°C	PDIP – N	Tube	SN74LS373N	SN74LS373N	
		Tube	SN74LS374N	SN74LS374N	
		Tube	SN74S373N	SN74S373N	
		Tube	SN74S374N	SN74S374N	
	SOIC – DW	Tube		SN74LS373DW	LS373
				SN74LS373DWR	
		Tape and reel		SN74LS374DW	LS374
				SN74LS374DWR	
		Tube		SN74S373DW	S373
				SN74S373DWR	
		Tape and reel		SN74S374DW	S374
				SN74S374DWR	
	SOP – NS	Tape and reel		SN74LS373NSR	74LS373
				SN74LS374NSR	74LS374
				SN74S374NSR	74S374
	SSOP – DB	Tape and reel		SN74LS374DBR	LS374A
–55°C to 125°C	CDIP – J	Tube	SN54LS373J	SN54LS373J	
		Tube	SNJ54LS373J	SNJ54LS373J	
		Tube	SN54LS374J	SN54LS374J	
		Tube	SNJ54LS374J	SNJ54LS374J	
		Tube	SN54S373J	SN54S373J	
		Tube	SNJ54S373J	SNJ54S373J	
		Tube	SN54S374J	SN54S374J	
		Tube	SNJ54S374J	SNJ54S374J	
	CFP – W	Tube		SNJ54LS373W	SNJ54LS373W
				SNJ54LS374W	SNJ54LS374W
				SNJ54S374W	SNJ54S374W
	LCCC – FK	Tube		SNJ54LS373FK	SNJ54LS373FK
				SNJ54LS374FK	SNJ54LS374FK
				SNJ54S373FK	SNJ54S373FK
				SNJ54S374FK	SNJ54S374FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

SN54LS373, SN54LS374, SN54S373, SN54S374,  
SN74LS373, SN74LS374, SN74S373, SN74S374

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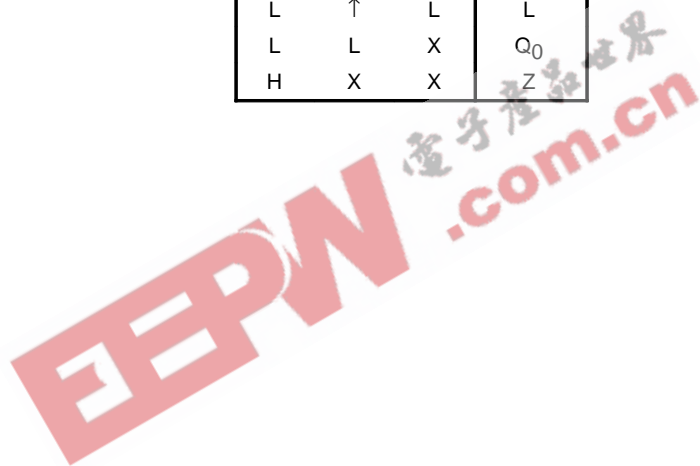
**Function Tables**

'LS373, 'S373  
(each latch)

INPUTS			OUTPUT Q
$\overline{OC}$	C	D	
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

'LS374, 'S374  
(each latch)

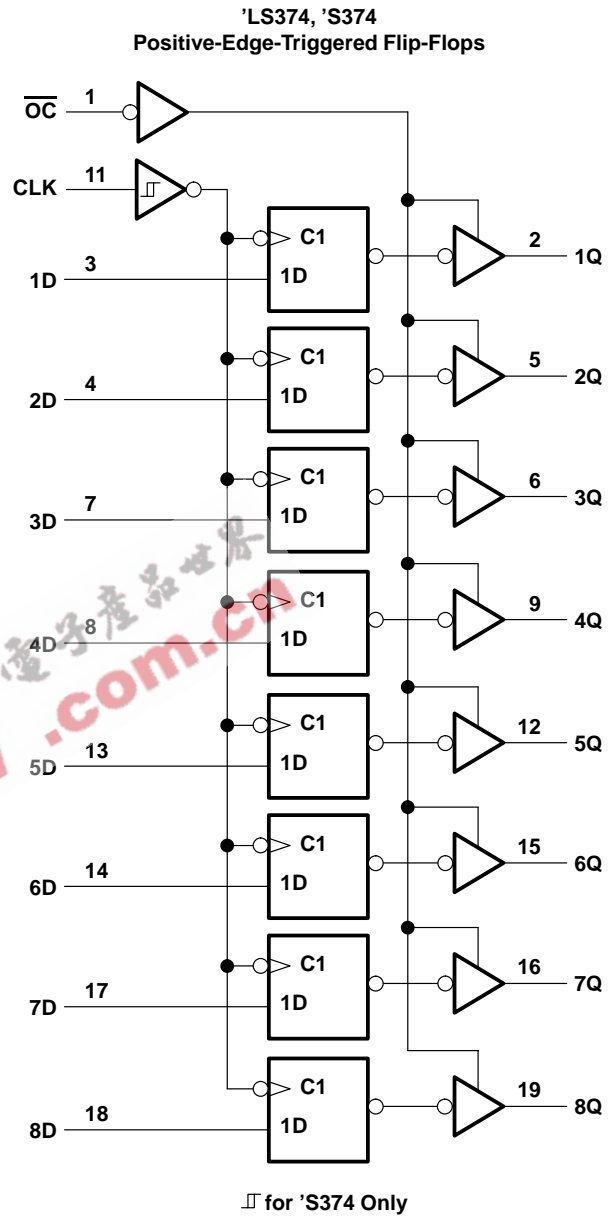
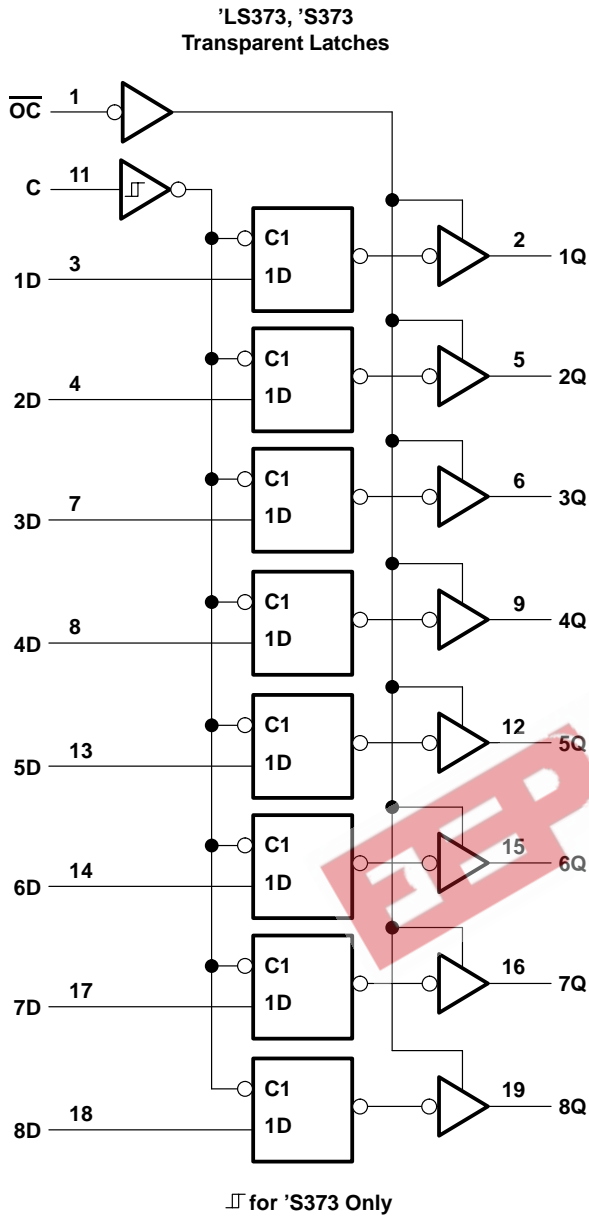
INPUTS			OUTPUT Q
$\overline{OC}$	CLK	D	
L	↑	H	H
L	↑	L	L
L	L	X	$Q_0$
H	X	X	Z



**SN54LS373, SN54LS374, SN54S373, SN54S374,  
SN74LS373, SN74LS374, SN74S373, SN74S374**  
**OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS**

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**logic diagrams (positive logic)**



Pin numbers shown are for DB, DW, J, N, NS, and W packages.

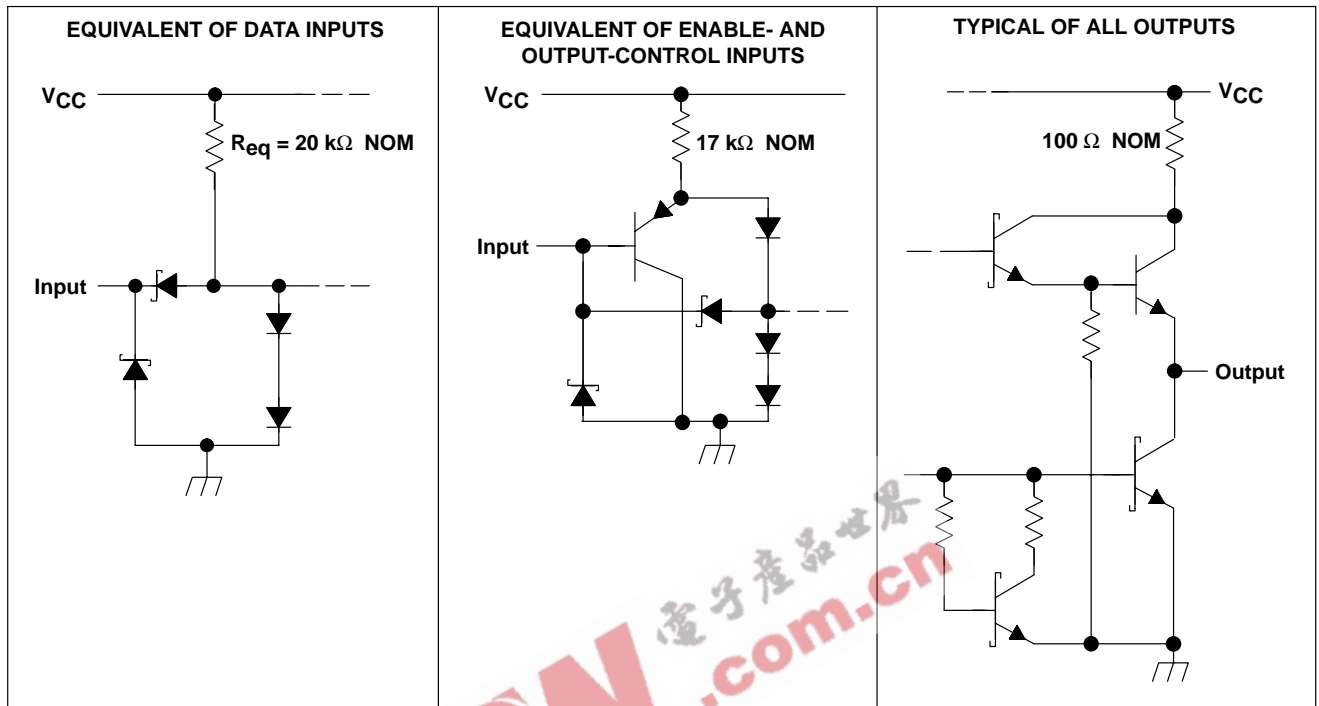
SN54LS373, SN54LS374, SN54S373, SN54S374,  
SN74LS373, SN74LS374, SN74S373, SN74S374

**OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS**

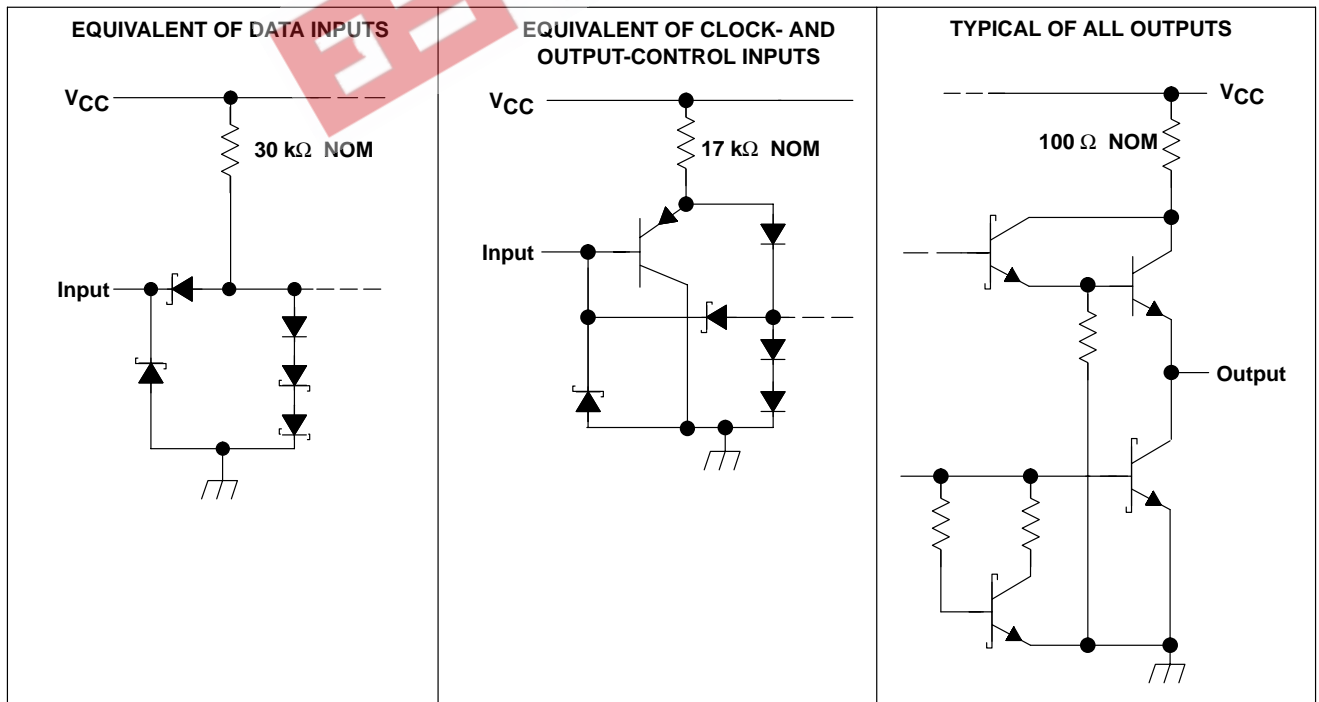
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**schematic of inputs and outputs**

'LS373



'LS374



**SN54LS373, SN54LS374, SN54S373, SN54S374,  
SN74LS373, SN74LS374, SN74S373, SN74S374  
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS**

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†  
(‘LS devices)**

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage, $V_I$	7 V
Off-state output voltage	5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package	70°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Voltage values are with respect to network ground terminal.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions**

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5	4.75	5	5.25	V
$V_{OH}$	High-level output voltage			5.5			5.5	V
$I_{OH}$	High-level output current			–1			–2.6	mA
$I_{OL}$	Low-level output current			12			24	mA
$t_w$	Pulse duration	CLK high		15		15		ns
		CLK low		15		15		
$t_{su}$	Data setup time	'LS373		5↓		5↓		ns
		'LS374		20↑		20↑		
$t_h$	Data hold time	'LS373		20↓		20↓		ns
		'LS374‡		5↑		0↑		
$T_A$	Operating free-air temperature		–55	125		0	70	°C

‡ The  $t_h$  specification applies only for data frequency below 10 MHz. Designs above 10 MHz should use a minimum of 5 ns (commercial only).

**SN54LS373, SN54LS374, SN54S373, SN54S374,  
SN74LS373, SN74LS374, SN74S373, SN74S374**  
**OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†	SN54LS'			SN74LS'			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IH</sub> High-level input voltage		2			2			V
V <sub>IL</sub> Low-level input voltage				0.7			0.8	V
V <sub>IK</sub> Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5			-1.5	V
V <sub>OH</sub> High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> max, I <sub>OH</sub> = MAX	2.4	3.4		2.4	3.1		V
V <sub>OL</sub> Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> max	I <sub>OL</sub> = 12 mA		0.25	0.4	0.25 0.4		V
		I <sub>OL</sub> = 24 mA				0.35 0.5		
I <sub>OZH</sub> Off-state output current, high-level voltage applied	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7 V, V <sub>IH</sub> = 2 V			20			20	μA
I <sub>OZL</sub> Off-state output current, low-level voltage applied	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.4 V, V <sub>IH</sub> = 2 V			-20			-20	μA
I <sub>I</sub> Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V			0.1			0.1	mA
I <sub>IH</sub> High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			20			20	μA
I <sub>IL</sub> Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-0.4			-0.4	mA
I <sub>OS</sub> Short-circuit output current§	V <sub>CC</sub> = MAX			-30	-130		-30 -130	mA
I <sub>CC</sub> Supply current	V <sub>CC</sub> = MAX, Output control at 4.5 V	'LS373		24	40	24 40		mA
		'LS374		27	40	27 40		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS373			'LS374			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f <sub>max</sub>			R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 45 pF, See Note 3				35	50		MHz
t <sub>PLH</sub>	Data	Any Q	R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 45 pF, See Note 3	12	18					ns
t <sub>PHL</sub>				12	18					
t <sub>PLH</sub>	C or CLK	Any Q	R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 45 pF, See Note 3	20	30		15	28		ns
t <sub>PHL</sub>				18	30		19	28		
t <sub>PZH</sub>	$\overline{OC}$	Any Q	R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 45 pF, See Note 3	15	28		20	26		ns
t <sub>PZL</sub>				25	36		21	28		
t <sub>PHZ</sub>	$\overline{OC}$	Any Q	R <sub>L</sub> = 667 Ω, C <sub>L</sub> = 5 pF	15	25		15	28		ns
t <sub>PLZ</sub>				12	20		12	20		

NOTE 3: Maximum clock frequency is tested with all outputs loaded.

f<sub>max</sub> = maximum clock frequency

t<sub>PLH</sub> = propagation delay time, low-to-high-level output

t<sub>PHL</sub> = propagation delay time, high-to-low-level output

t<sub>PZH</sub> = output enable time to high level

t<sub>PZL</sub> = output enable time to low level

t<sub>PHZ</sub> = output disable time from high level

t<sub>PLZ</sub> = output disable time from low level

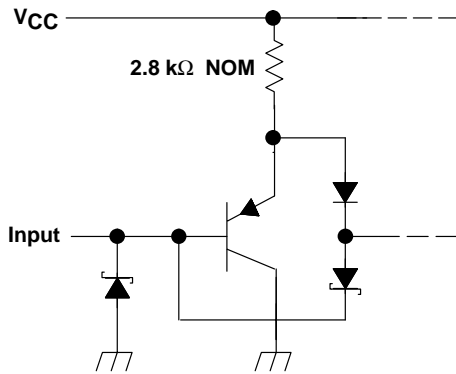
**SN54LS373, SN54LS374, SN54S373, SN54S374,  
SN74LS373, SN74LS374, SN74S373, SN74S374**  
**OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS**

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**schematic of inputs and outputs**

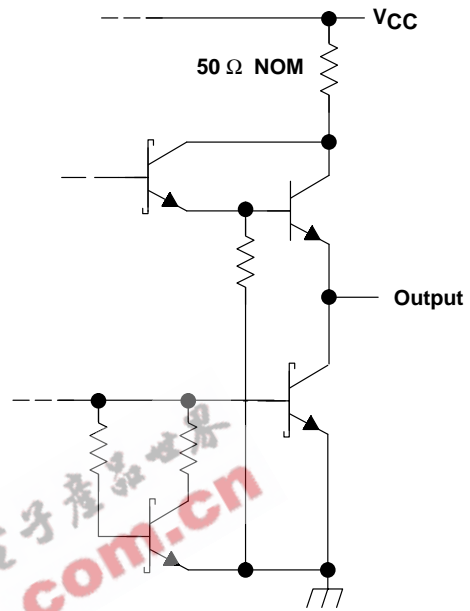
'S373 and 'S374

EQUIVALENT OF EACH INPUT



'S373 and 'S374

TYPICAL OF ALL OUTPUTS



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SN74LS373, SN74LS374, SN74S373, SN74S374**  
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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†  
(‘S devices)**

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Input voltage, $V_I$ .....	5.5 V
Off-state output voltage .....	5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package .....	58°C/W
N package .....	69°C/W
NS package .....	60°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Voltage values are with respect to network ground terminal.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions**

		SN54S*			SN74S*			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{OH}$	High-level output voltage			5.5			5.5	V
$I_{OH}$	High-level output current			–2			–6.5	mA
$t_w$	Pulse duration, clock/enable	High	6		6			ns
		Low	7.3		7.3			
$t_{su}$	Data setup time	‘S373	0↓		0↓			ns
		‘S374	5↑		5↑			
$t_h$	Data hold time	‘S373	10↓		10↓			ns
		‘S374	2↑		2↑			
$T_A$	Operating free-air temperature		–55	125		0	70	°C

**SN54LS373, SN54LS374, SN54S373, SN54S374,  
SN74LS373, SN74LS374, SN74S373, SN74S374**  
**OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS**  
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (SN54S373, SN54S374, SN74S373, SN74S374)

PARAMETER	TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V <sub>IH</sub>				2			V
V <sub>IL</sub>						0.8	V
V <sub>IK</sub>	V <sub>CC</sub> = MIN,	I <sub>I</sub> = -18 mA				-1.2	V
V <sub>OH</sub>	SN54S' SN74S'	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = MAX		2.4	3.4		V
				2.4	3.1		
V <sub>OL</sub>	V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 20 mA				0.5	V
I <sub>OZH</sub>	V <sub>CC</sub> = MAX,	V <sub>IH</sub> = 2 V, V <sub>O</sub> = 2.4 V				50	μA
I <sub>OZL</sub>	V <sub>CC</sub> = MAX,	V <sub>IH</sub> = 2 V, V <sub>O</sub> = 0.5 V				-50	μA
I <sub>I</sub>	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 5.5 V				1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 2.7 V				50	μA
I <sub>IL</sub>	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 0.5 V				-250	μA
I <sub>OS</sub> §	V <sub>CC</sub> = MAX			-40		-100	mA
I <sub>CC</sub>	V <sub>CC</sub> = MAX	'S373	Outputs high			160	mA
			Outputs low			160	
			Outputs disabled			190	
		'S374	Outputs high			110	
			Outputs low			140	
			Outputs disabled			160	
			CLK and $\overline{OC}$ at 4 V, D inputs at 0 V			180	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see Figure 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'S373			'S374			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f <sub>max</sub>			R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 15 pF, See Note 3				75	100		MHz
t <sub>PLH</sub>	Data	Any Q	R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 15 pF, See Note 3		7	12				ns
t <sub>PHL</sub>					7	12				
t <sub>PLH</sub>	C or CLK	Any Q	R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 15 pF, See Note 3		7	14		8	15	ns
t <sub>PHL</sub>					12	18		11	17	
t <sub>PZH</sub>	$\overline{OC}$	Any Q	R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 15 pF, See Note 3		8	15		8	15	ns
t <sub>PZL</sub>					11	18		11	18	
t <sub>PHZ</sub>	$\overline{OC}$	Any Q	R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 5 pF		6	9		5	9	ns
t <sub>PLZ</sub>					8	12		7	12	

NOTE 3. Maximum clock frequency is tested with all outputs loaded.

f<sub>max</sub> = maximum clock frequency

t<sub>PLH</sub> = propagation delay time, low-to-high-level output

t<sub>PHL</sub> = propagation delay time, high-to-low-level output

t<sub>PZH</sub> = output enable time to high level

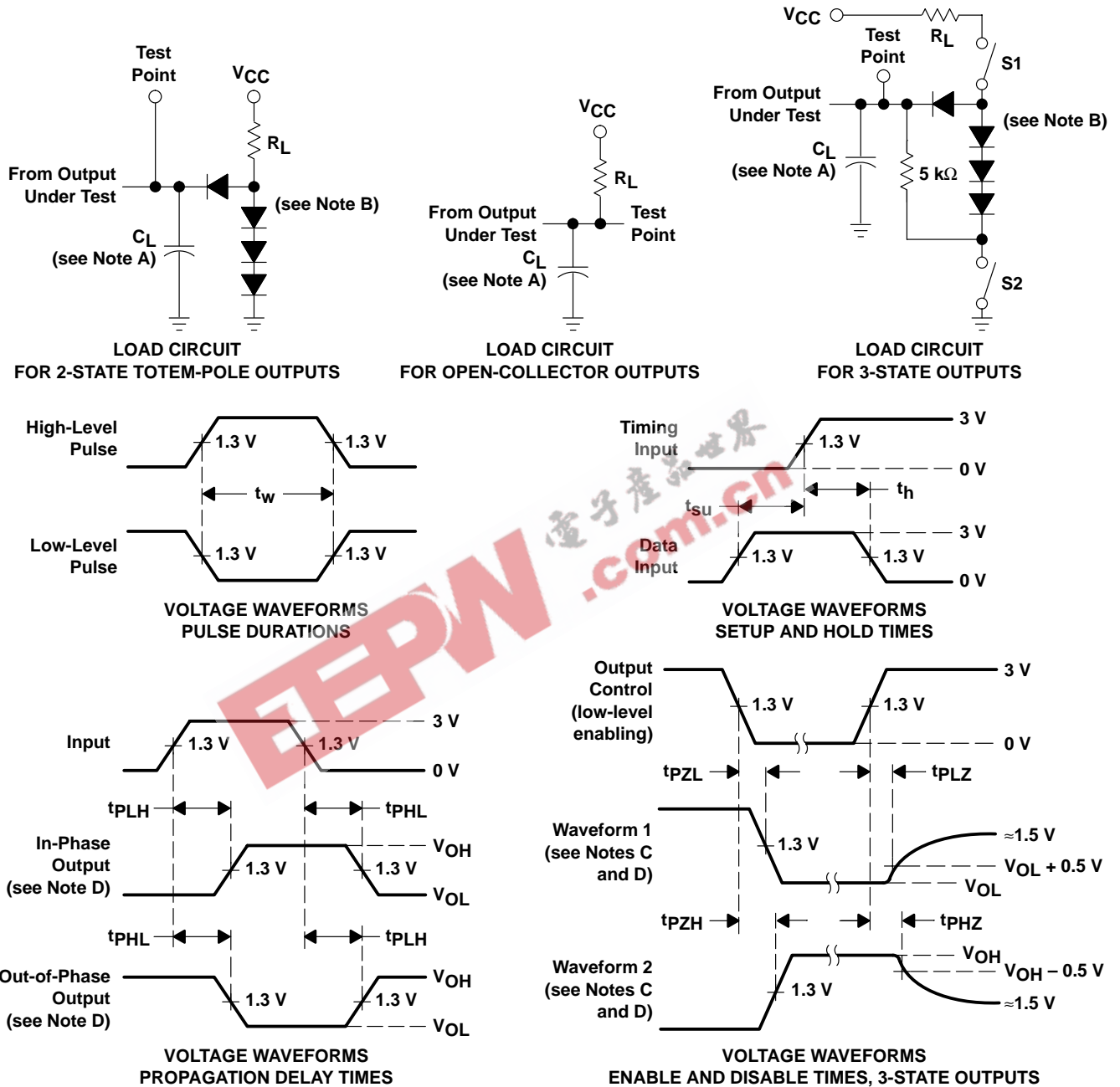
t<sub>PZL</sub> = output enable time to low level

t<sub>PHZ</sub> = output disable time from high level

t<sub>PLZ</sub> = output disable time from low level

**SN54LS373, SN54LS374, SN54S373, SN54S374,  
SN74LS373, SN74LS374, SN74S373, SN74S374**  
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**PARAMETER MEASUREMENT INFORMATION  
SERIES 54LS/74LS DEVICES**



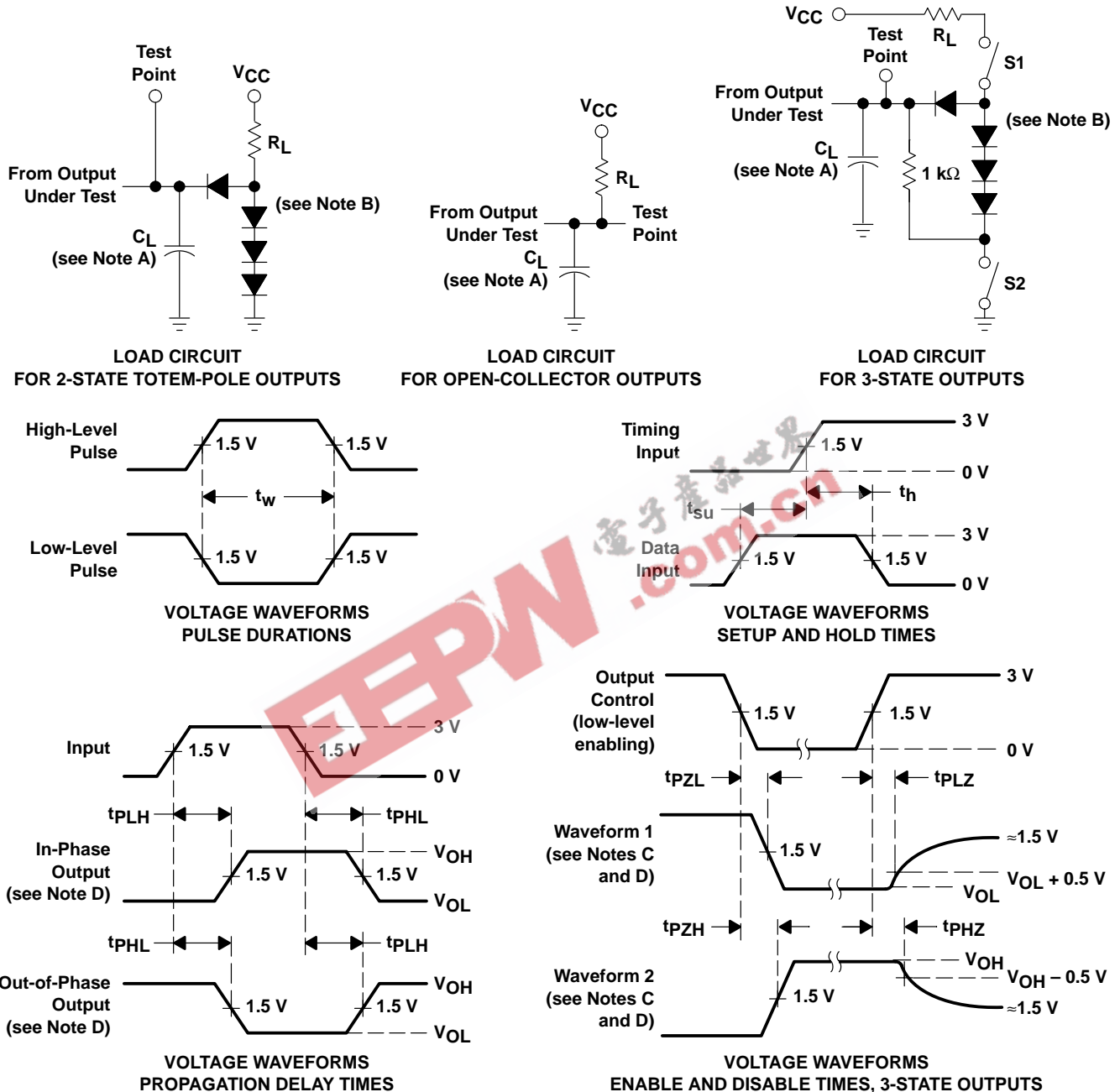
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All diodes are 1N3064 or equivalent.  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. S1 and S2 are closed for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_{PHZ}$ , and  $t_{PLZ}$ ; S1 is open and S2 is closed for  $t_{PZH}$ ; S1 is closed and S2 is open for  $t_{PZL}$ .  
 E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.  
 F. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O \approx 50 \Omega$ ,  $t_r \leq 1.5$  ns,  $t_f \leq 2.6$  ns.  
 G. The outputs are measured one at a time with one input transition per measurement.  
 H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuits and Voltage Waveforms**

**SN54LS373, SN54LS374, SN54S373, SN54S374,  
SN74LS373, SN74LS374, SN74S373, SN74S374  
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS**

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**PARAMETER MEASUREMENT INFORMATION  
SERIES 54S/74S DEVICES**



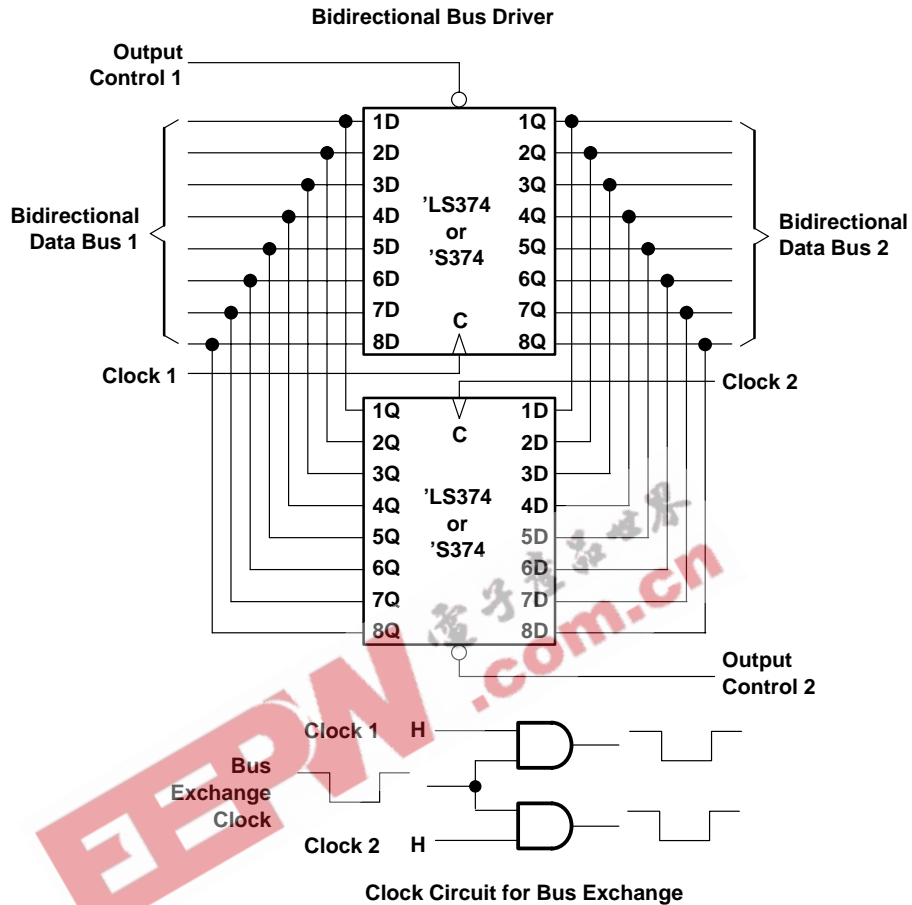
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All diodes are 1N3064 or equivalent.  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. S1 and S2 are closed for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_{PHZ}$ , and  $t_{PLZ}$ ; S1 is open and S2 is closed for  $t_{PZH}$ ; S1 is closed and S2 is open for  $t_{PZL}$ .  
 E. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O \approx 50 \Omega$ ;  $t_r$  and  $t_f \leq 7$  ns for Series 54/74 devices and  $t_r$  and  $t_f \leq 2.5$  ns for Series 54S/74S devices.  
 F. The outputs are measured one at a time with one input transition per measurement.  
 G. All parameters and waveforms are not applicable to all devices.

**Figure 2. Load Circuits and Voltage Waveforms**

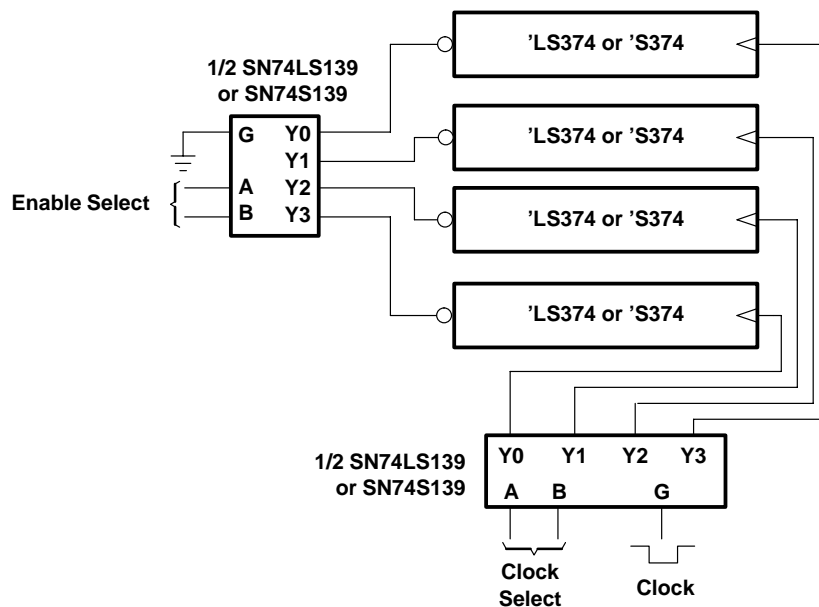
**SN54LS373, SN54LS374, SN54S373, SN54S374,  
SN74LS373, SN74LS374, SN74S373, SN74S374**  
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

SDLS165B – OCTOBER 1975 – REVISED AUGUST 2002

**TYPICAL APPLICATION DATA**



**Expandable 4-Word by 8-Bit General Register File**



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-7801102VRA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
5962-7801102VSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
78011022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
7801102RA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
7801102SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
JM38510/32502B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/32502BRA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/32502BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
JM38510/32502SRA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/32502SSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
JM38510/32503B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/32503BRA	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/32503BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
SN54LS373J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS374J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SN54S373J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SN54S374J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SN74LS373DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS373DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS373DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS373DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS373DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS373DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS373N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS373N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74LS373NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS373NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS373NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS373NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS374DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS374DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS374DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LS374DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS374DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS374DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS374DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS374J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI
SN74LS374N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS374N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74LS374NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS374NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS374NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS374NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S373DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S373DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S373DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S373DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S373DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S373DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S373J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI
SN74S373N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S373N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74S373NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S374DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S374DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S374DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S374DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S374DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S374DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S374J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI



Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74S374N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S374N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74S374NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S374NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S374NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S374NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54LS373FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS373J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS373W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
SNJ54LS374FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS374J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS374W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
SNJ54S373FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54S373J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54S374FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54S374J	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54S374W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

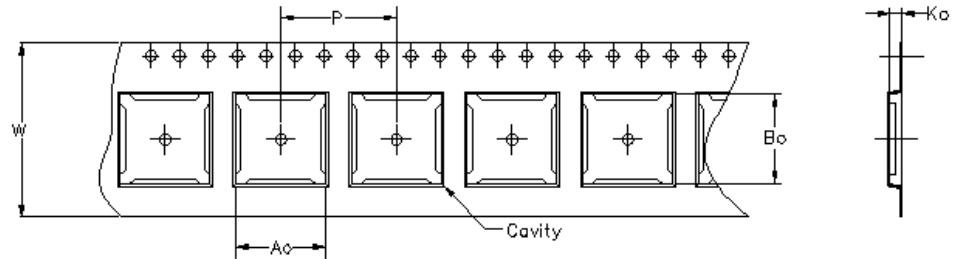
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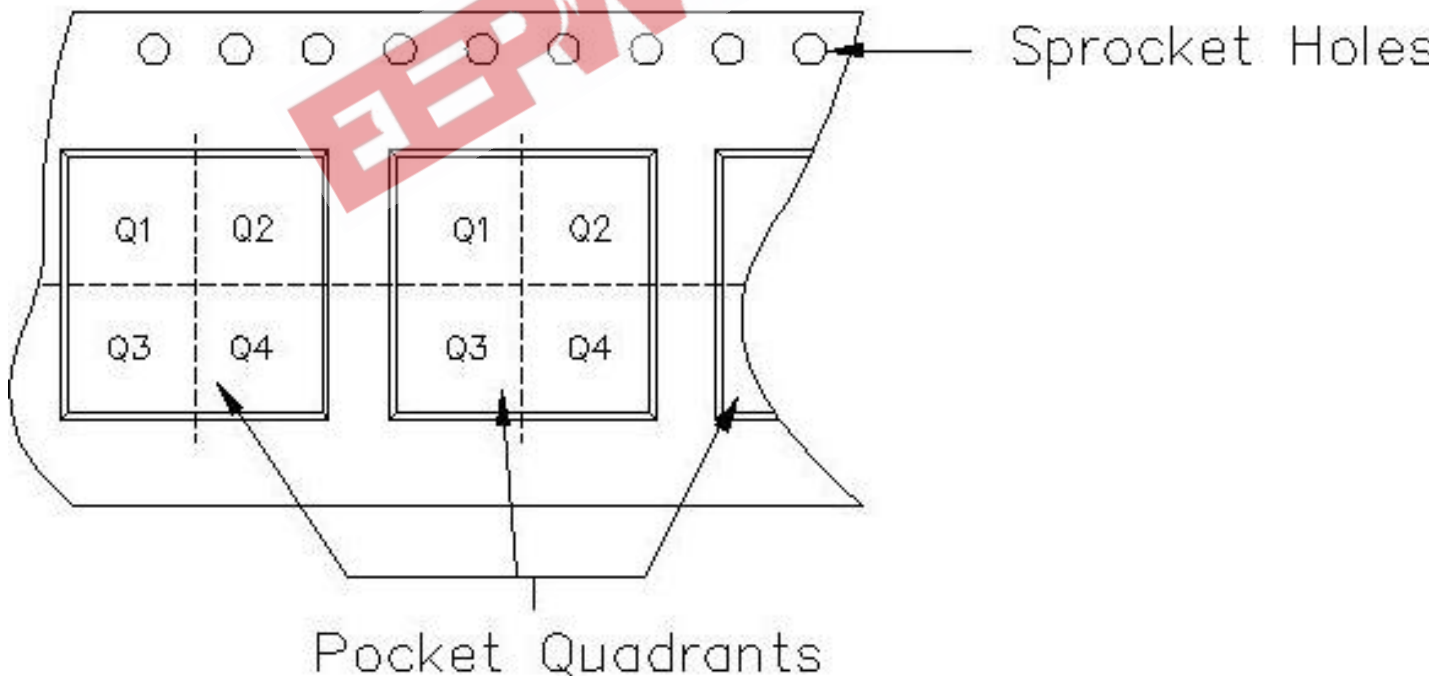
to Customer on an annual basis.

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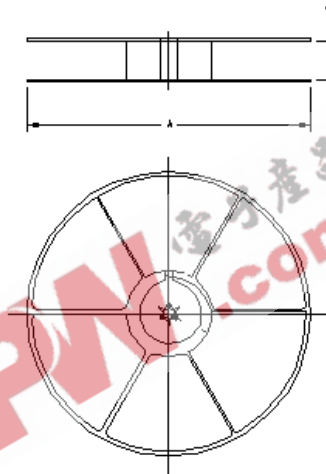
Carrier tape design is defined largely by the component length, width, and thickness.

$A_o$ = Dimension designed to accommodate the component width.
$B_o$ = Dimension designed to accommodate the component length.
$K_o$ = Dimension designed to accommodate the component thickness.
$W$ = Overall width of the carrier tape.
$P$ = Pitch between successive cavity centers.



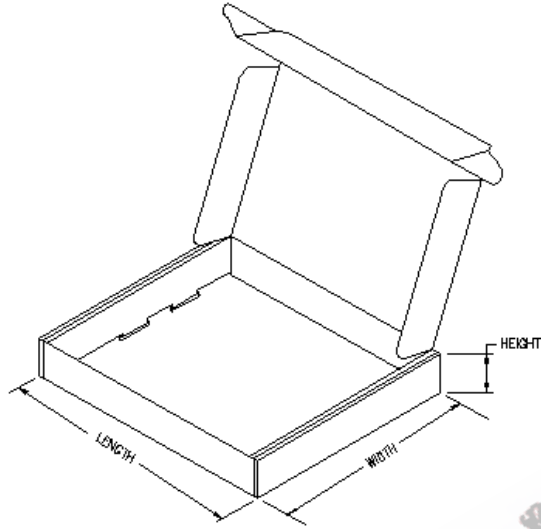
**TAPE AND REEL INFORMATION**

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS373DWR	DW	20	MLA	330	24	10.8	13.0	2.7	12	24	Q1
SN74LS373NSR	NS	20	MLA	330	24	8.2	13.0	2.5	12	24	Q1
SN74LS374DBR	DB	20	MLA	330	16	8.2	7.5	2.5	12	16	Q1
SN74LS374DWR	DW	20	MLA	330	24	10.8	13.0	2.7	12	24	Q1
SN74LS374NSR	NS	20	MLA	330	24	8.2	13.0	2.5	12	24	Q1
SN74S373DWR	DW	20	MLA	330	24	10.8	13.0	2.7	12	24	Q1
SN74S374DWR	DW	20	MLA	330	24	10.8	13.0	2.7	12	24	Q1
SN74S374NSR	NS	20	MLA	330	24	8.2	13.0	2.5	12	24	Q1



**TAPE AND REEL BOX INFORMATION**

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74LS373DWR	DW	20	MLA	333.2	333.2	31.75
SN74LS373NSR	NS	20	MLA	333.2	333.2	31.75
SN74LS374DBR	DB	20	MLA	342.9	336.6	28.58
SN74LS374DWR	DW	20	MLA	333.2	333.2	31.75
SN74LS374NSR	NS	20	MLA	333.2	333.2	31.75
SN74S373DWR	DW	20	MLA	333.2	333.2	31.75
SN74S374DWR	DW	20	MLA	333.2	333.2	31.75
SN74S374NSR	NS	20	MLA	333.2	333.2	31.75



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J (R-GDIP-T\*\*)  
14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



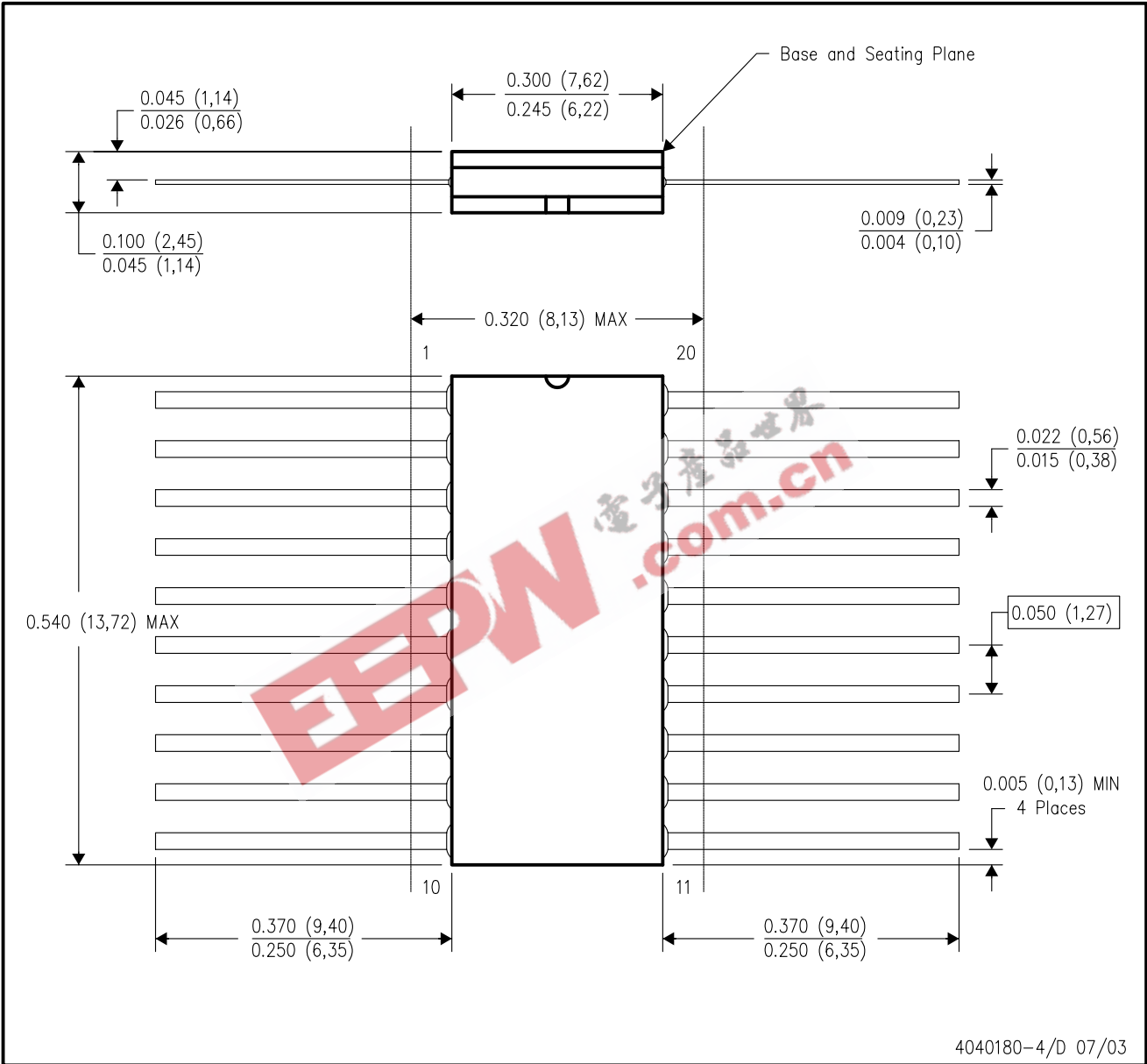
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



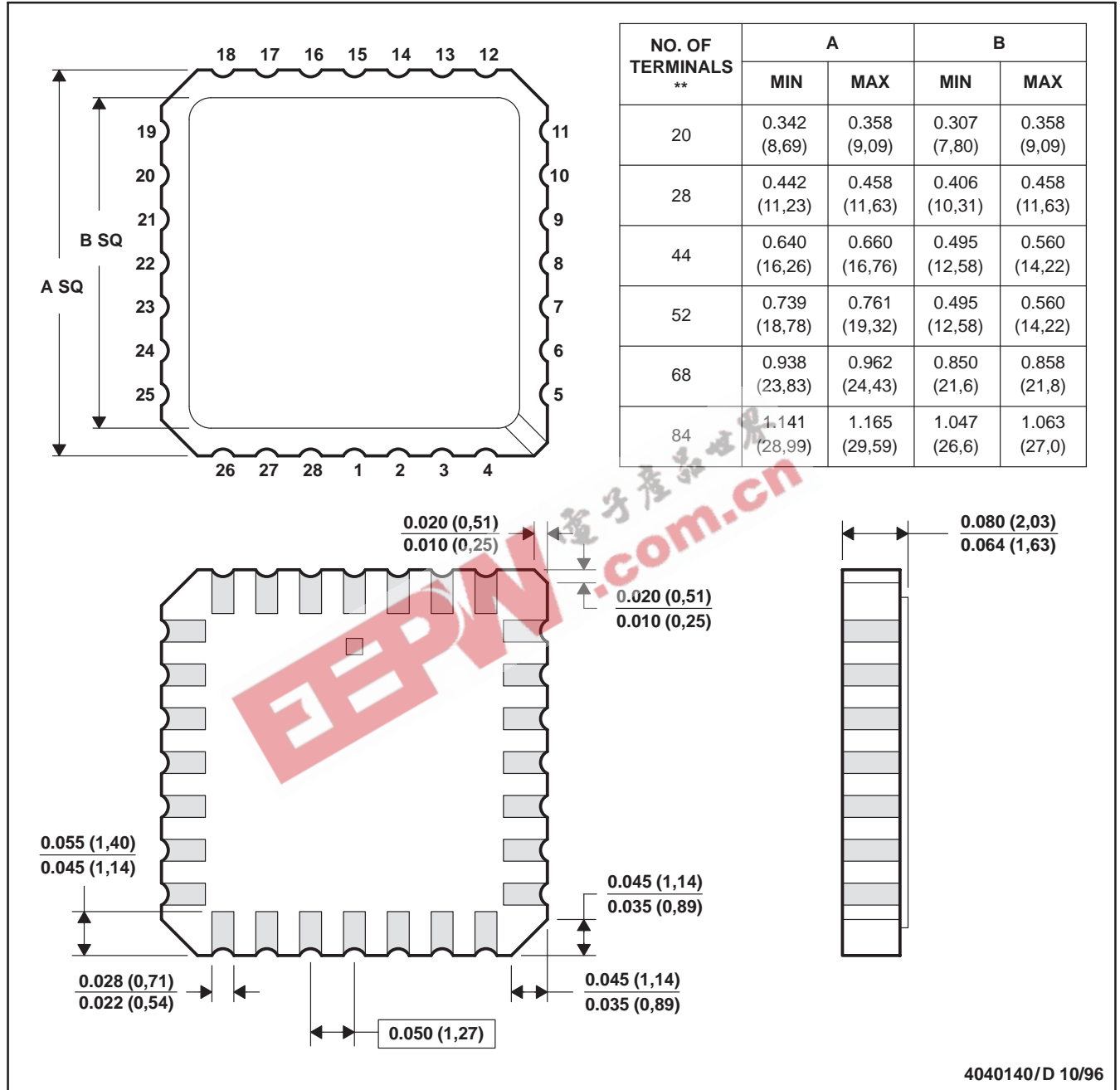
4040180-4/D 07/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



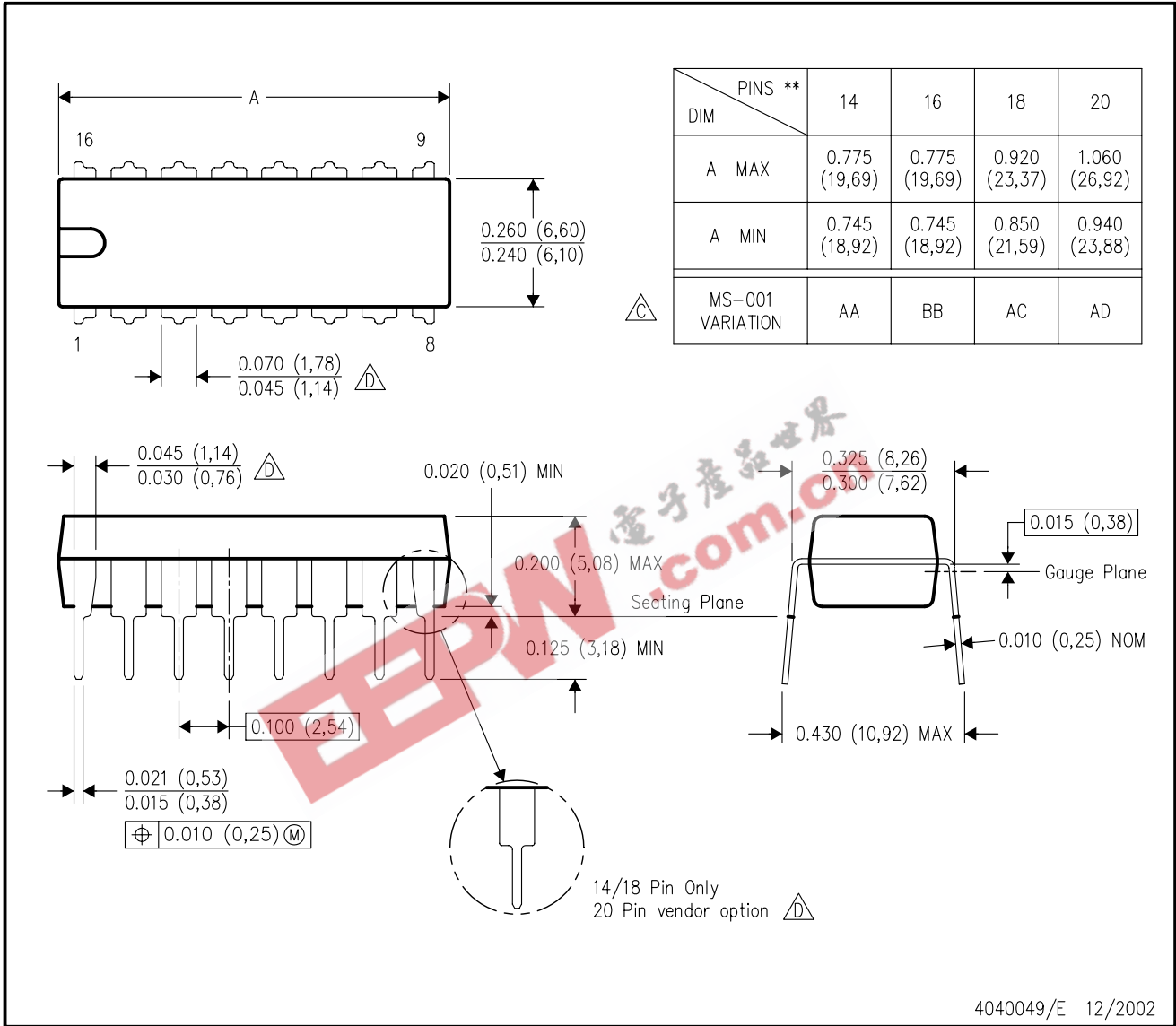
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

# MECHANICAL DATA

## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



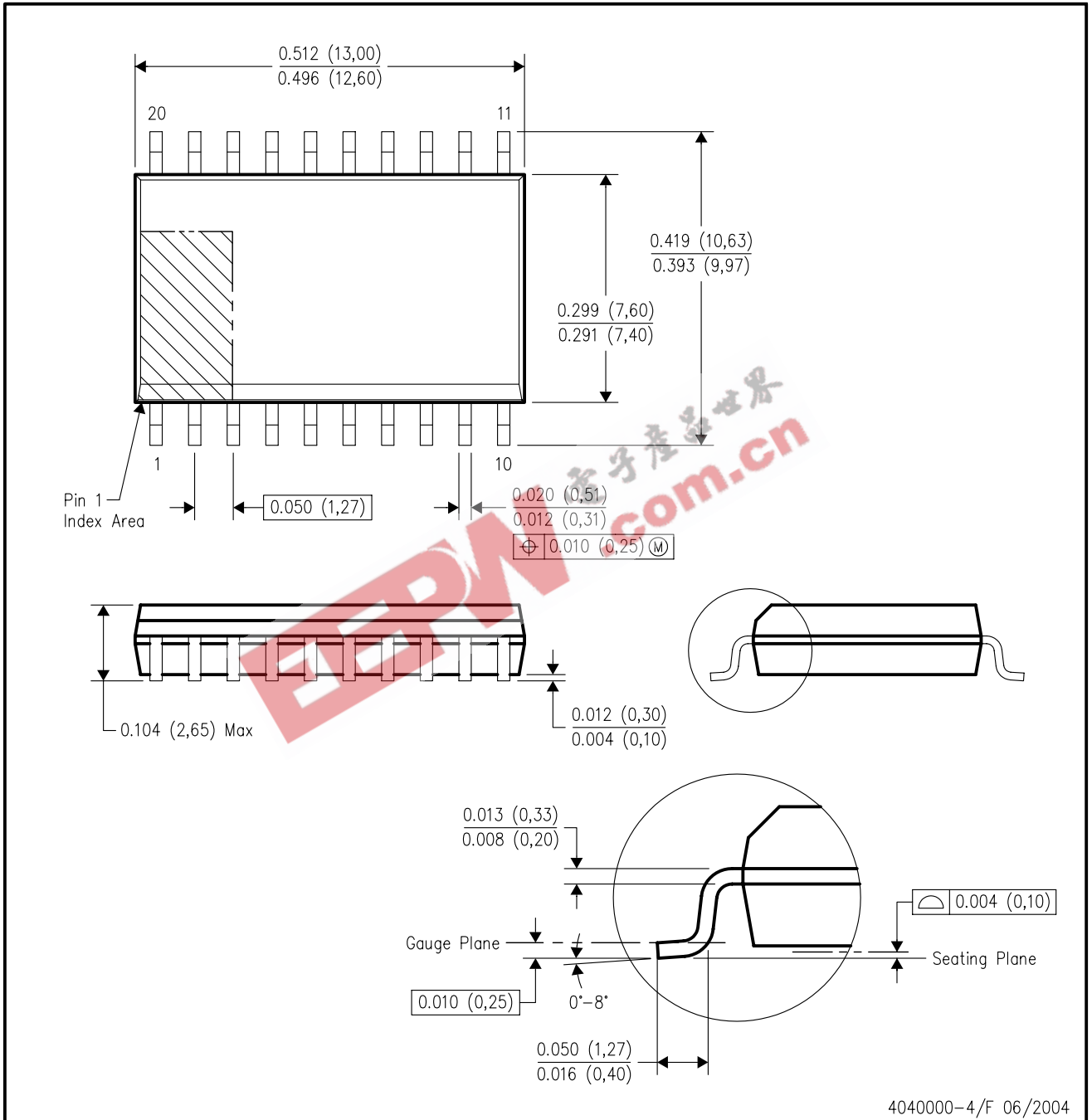
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



# MECHANICAL DATA

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



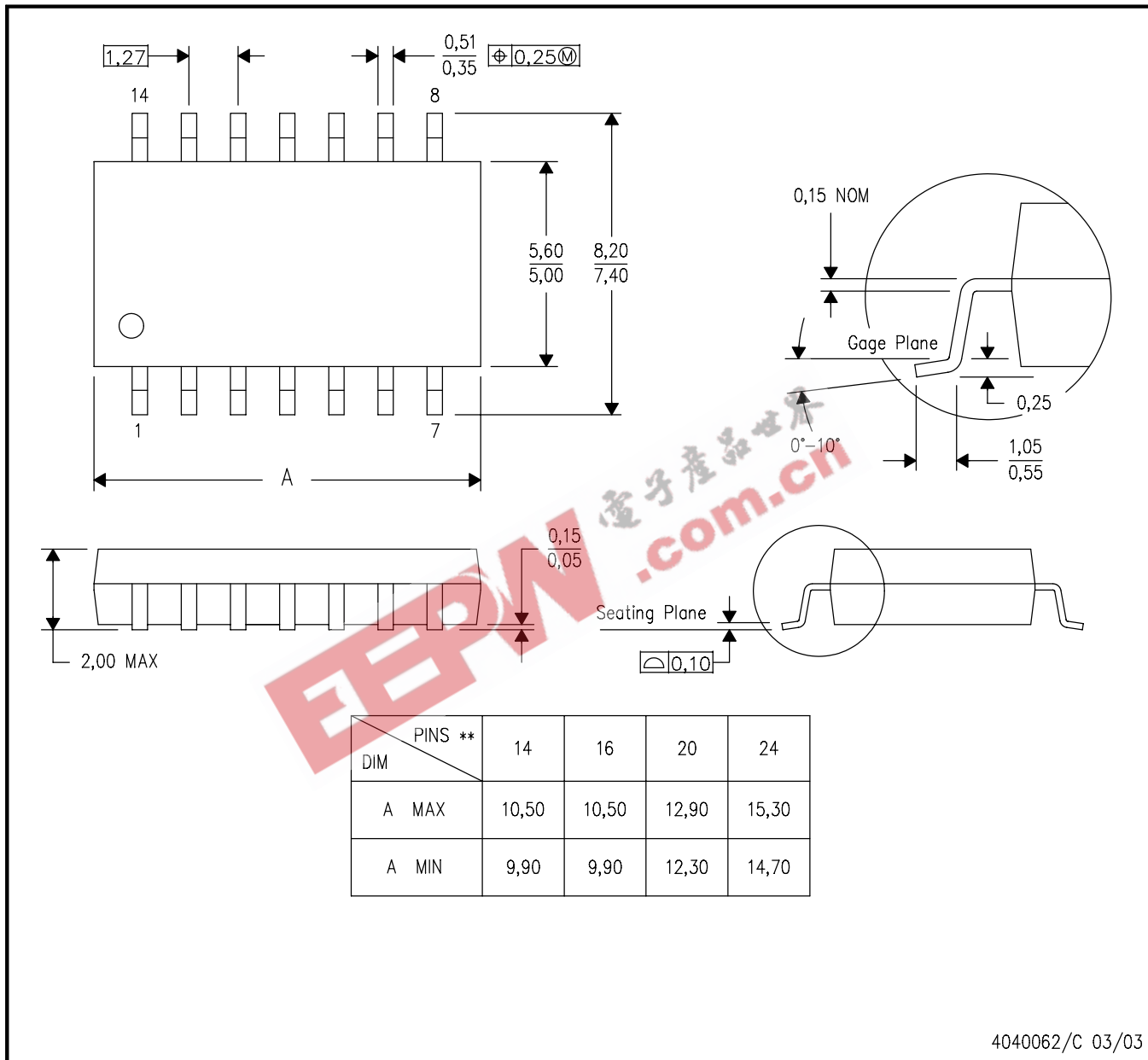
4040000-4/F 06/2004

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

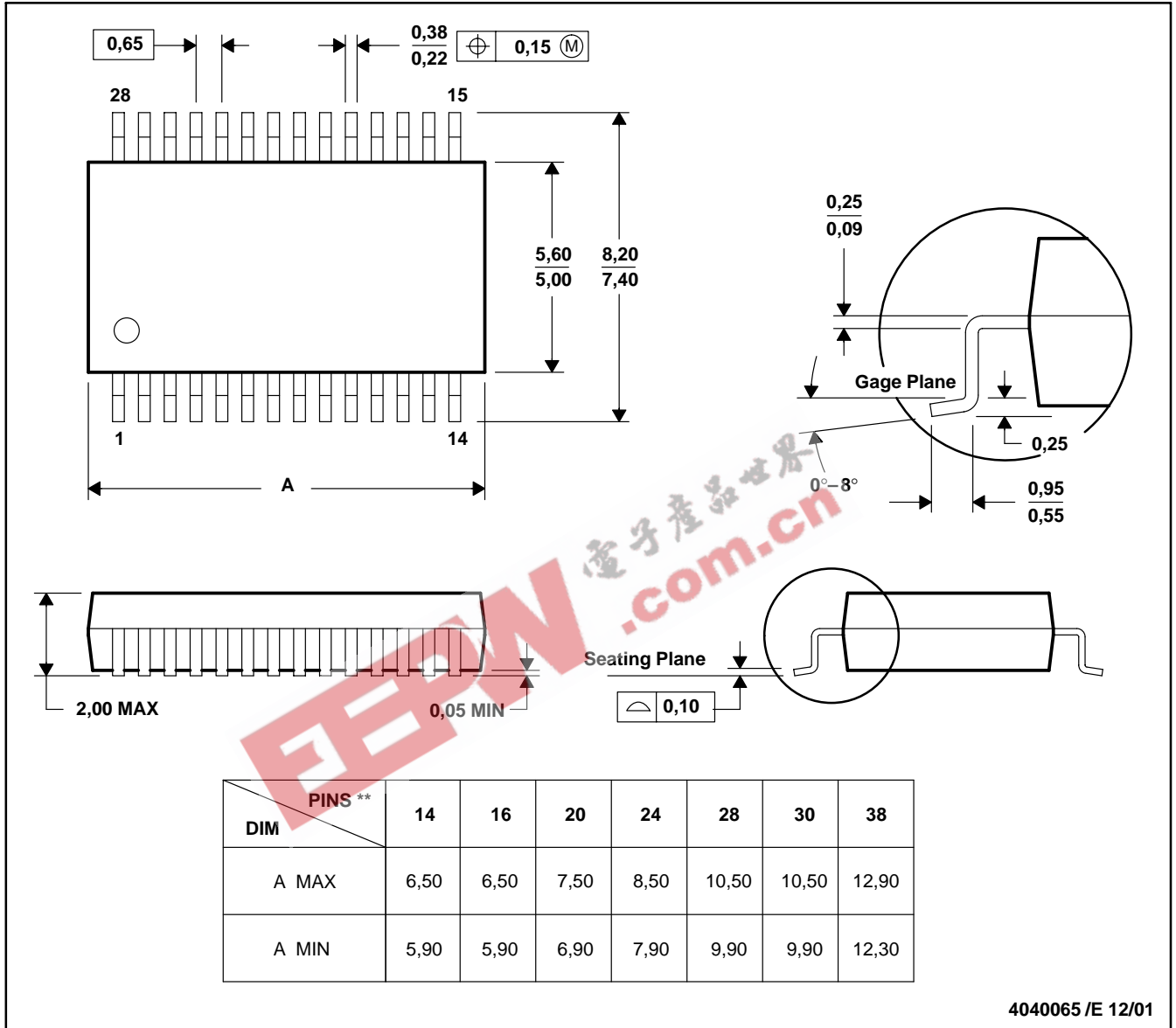
# MECHANICAL DATA

MSS0002E – JANUARY 1995 – REVISED DECEMBER 2001

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



4040065 /E 12/01

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
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