FAIRCHILD SEMICONDUCTOR®

February 1994
Revised May 2005

74LCX16245
Low Voltage 16-Bit Bidirectional Transceiver with 5V Tolerant Inputs and Outputs

General Description

The LCX16245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The device is byte controlled. Each byte has separate control inputs which could be shorted together for full 16-bit operation. The T/$\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

The LCX16245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V V_{CC} specifications provided
- 4.5 ns t_{PD} max (V_{CC} = 3.3V), 20 μA I_{CC} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- ±24 mA output drive (V_{CC} = 3.0V)
- Uses patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

Note 1: To ensure the high-impedance state during power up or down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

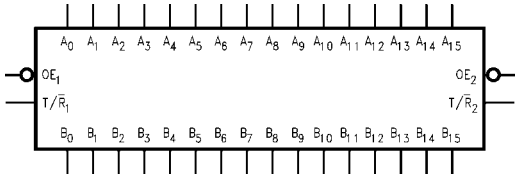
Ordering Code:

Order Number	Package Number	Package Description
74LCX16245G (Note 2)(Note 3)	BGA54A	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74LCX16245MEA (Note 3)	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LCX16245MTD (Note 3)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Note 2: Ordering code "G" indicates Trays.

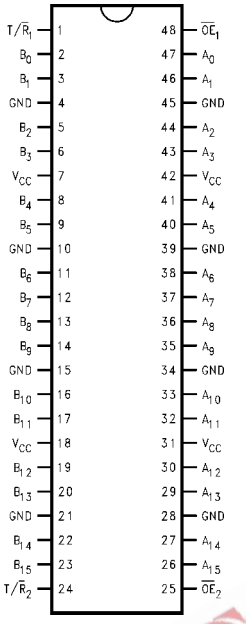
Note 3: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol

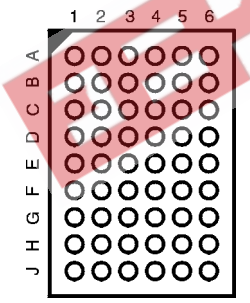


Connection Diagrams

Pin Assignment for SSOP and TSSOP



Pin Assignment for FBGA



(Top Thru View)

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input
$T/\overline{R}_n$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs or 3-STATE Outputs
B_0–B_{15}	Side B Inputs or 3-STATE Outputs
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
A	B_0	NC	T/R_1	$\overline{OE}_1$	NC	A_0
B	B_2	B_1	NC	NC	A_1	A_2
C	B_4	B_3	V_{CC}	V_{CC}	A_3	A_4
D	B_6	B_5	GND	GND	A_5	A_6
E	B_8	B_7	GND	GND	A_7	A_8
F	B_{10}	B_9	GND	GND	A_9	A_{10}
G	B_{12}	B_{11}	V_{CC}	V_{CC}	A_{11}	A_{12}
H	B_{14}	B_{13}	NC	NC	A_{13}	A_{14}
J	B_{15}	NC	$T/\overline{R}_2$	OE_2	NC	A_{15}

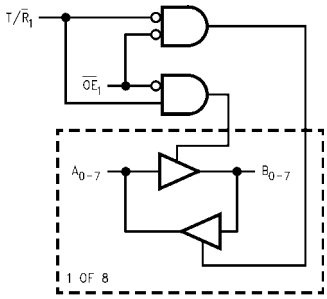
Truth Tables

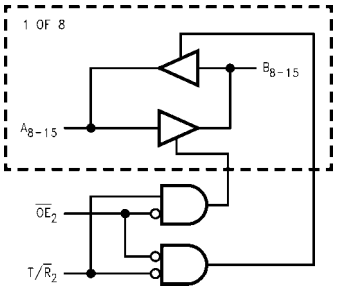
Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH Z State on A_0–A_7, B_0–B_7

Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH Z State on A_8–A_{15}, B_8–B_{15}

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagrams





Note: Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 4)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0 −0.5 to V_{CC} + 0.5	Output in 3-STATE Output in HIGH or LOW State (Note 5)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50 +50	V_O < GND V_O > V_{CC}	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions (Note 6)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		3-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V − 3.6V		±24	mA
		V_{CC} = 2.7V − 3.0V		±12	
		V_{CC} = 2.3V − 2.7V		±8	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

Note 4: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 5: I_O Absolute Maximum Rating must be observed.

Note 6: Unused inputs or I/O's must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		
V_{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	2.3 – 3.6	V_{CC} – 0.2		V
		I_{OH} = −8 mA	2.3	1.8		
		I_{OH} = −12 mA	2.7	2.2		
		I_{OH} = −18 mA	3.0	2.4		
		I_{OH} = −24 mA	3.0	2.2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	2.3 – 3.6		0.2	V
		I_{OL} = 8mA	2.3		0.6	
		I_{OL} = 12 mA	2.7		0.4	
		I_{OL} = 16 mA	3.0		0.4	
		I_{OL} = 24 mA	3.0		0.55	
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.3 – 3.6		±5.0	μA
I_{OZ}	3-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	2.3 – 3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units
				Min	Max	
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3–3.6		20	μA
		$3.6V \le V_I, V_O \le 5.5V$ (Note 7)	2.3–3.6		±20	
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.3–3.6		500	μA

Note 7: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5V \pm 0.2V$		
		$C_L = 50$ pF		$C_L = 50$ pF		$C_L = 30$ pF		
		Min	Max	Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.5	4.5	1.5	5.2	1.5	5.4	ns
t_{PLH}	A_n to B_n or B_n to A_n	1.5	4.5	1.5	5.2	1.5	5.4	
t_{PZL}	Output Enable Time	1.5	6.5	1.5	7.2	1.5	8.5	ns
t_{PZH}		1.5	6.5	1.5	7.2	1.5	8.5	
t_{PLZ}	Output Disable Time	1.5	6.4	1.5	6.9	1.5	7.7	ns
t_{PHZ}		1.5	6.4	1.5	6.9	1.5	7.7	
t_{OSHL}	Output to Output Skew		1.0					ns
t_{OSLH}	(Note 8)		1.0					

Note 8: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	–0.8	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	–0.6	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, f = 10 MHz	20	pF

AC LOADING and WAVEFORMS Generic for LCX Family

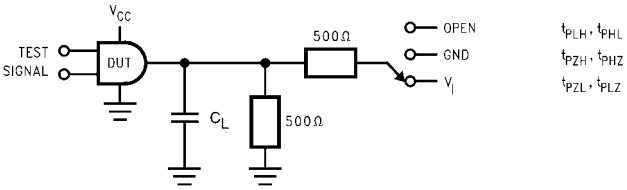
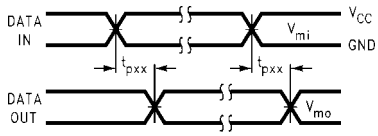
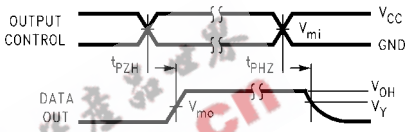


FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

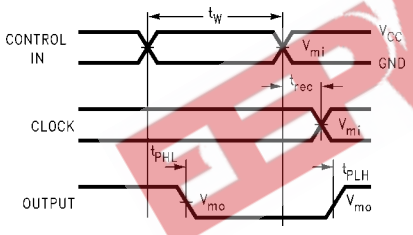
Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ± 0.3V V_{CC} x 2 at V_{CC} = 2.5 ± 0.2V
t_{PZH},t_{PHZ}	GND



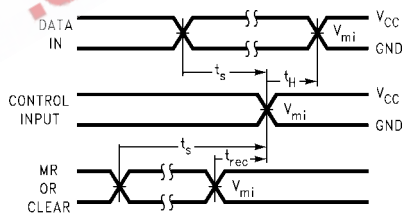
Waveform for Inverting and Non-Inverting Functions



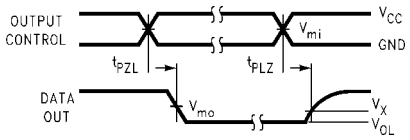
3-STATE Output High Enable and Disable Times for Logic



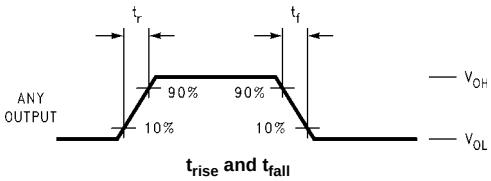
Propagation Delay. Pulse Width and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

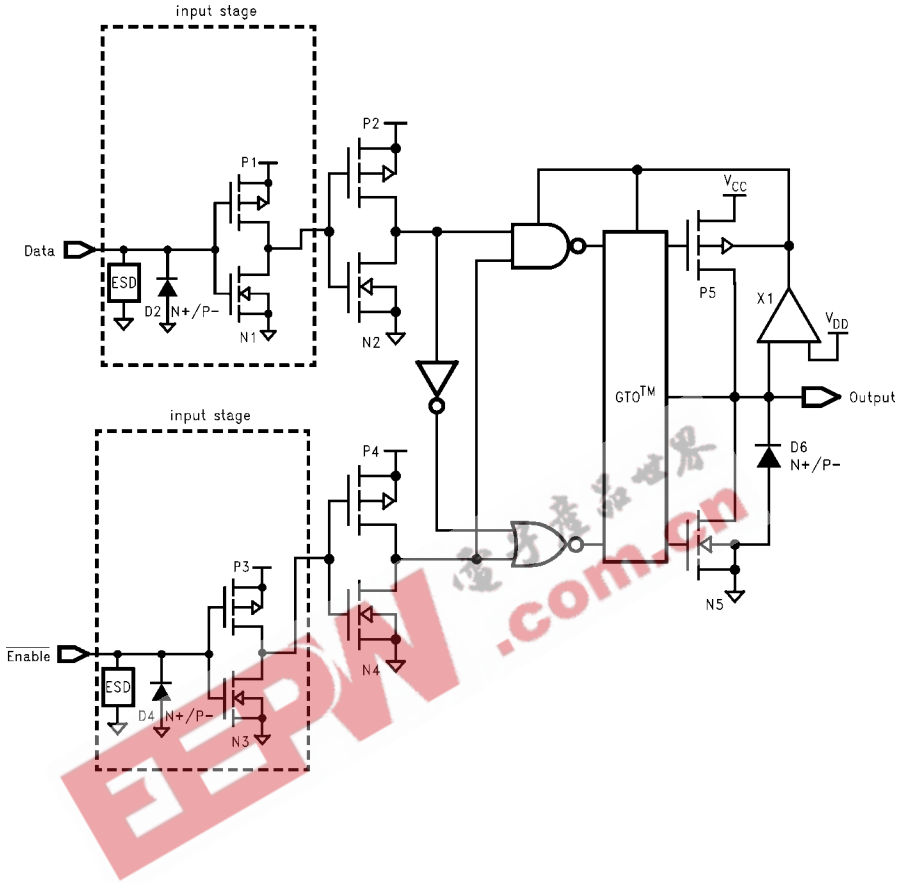


t_{rise} and t_{fall}

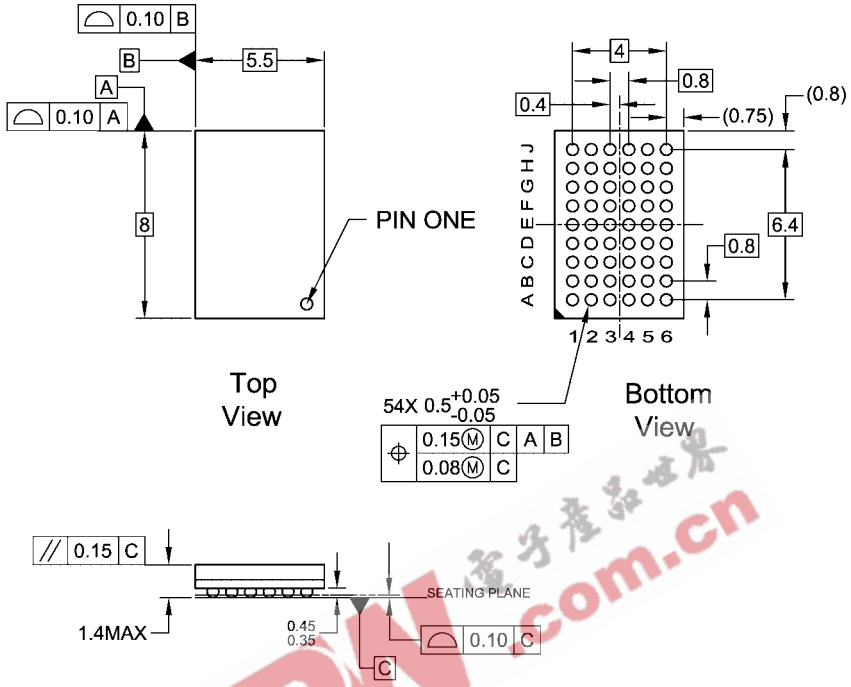
FIGURE 2. Waveforms
(Input Characteristics; f =1MHz, t_r = t_f = 3ns)

Symbol	V_{CC}		
	3.3V ± 0.3V	2.7V	2.5V ± 0.2V
V_{mi}	1.5V	1.5V	V_{CC}/2
V_{mo}	1.5V	1.5V	V_{CC}/2
V_x	V_{OL} + 0.3V	V_{OL} + 0.3V	V_{OL} + 0.15V
V_y	V_{OH} − 0.3V	V_{OH} − 0.3V	V_{OH} − 0.15V

Schematic Diagram Generic for LCX Family



Physical Dimensions inches (millimeters) unless otherwise noted



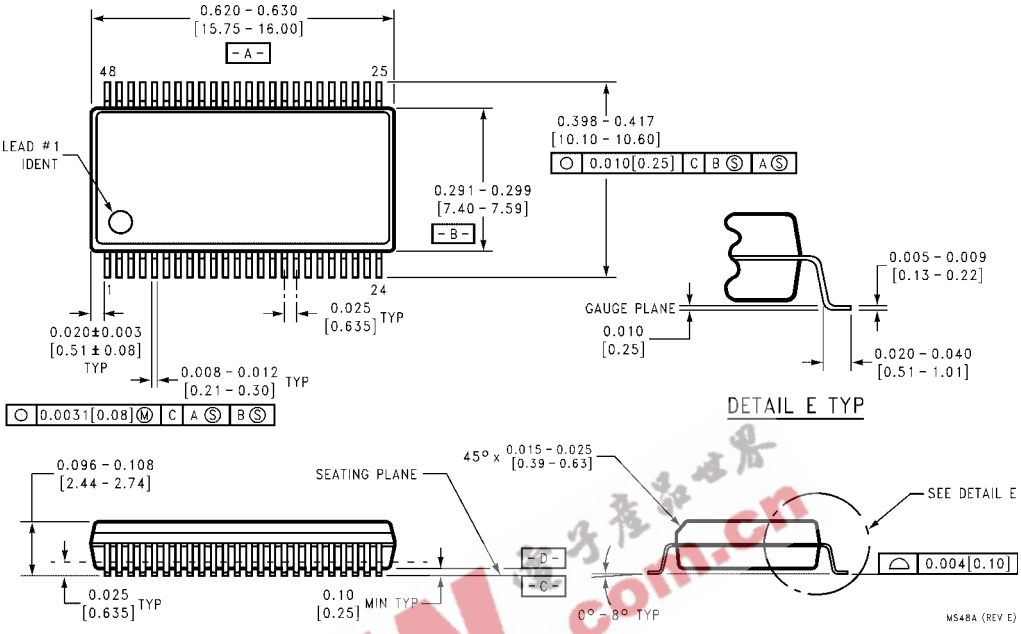
NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

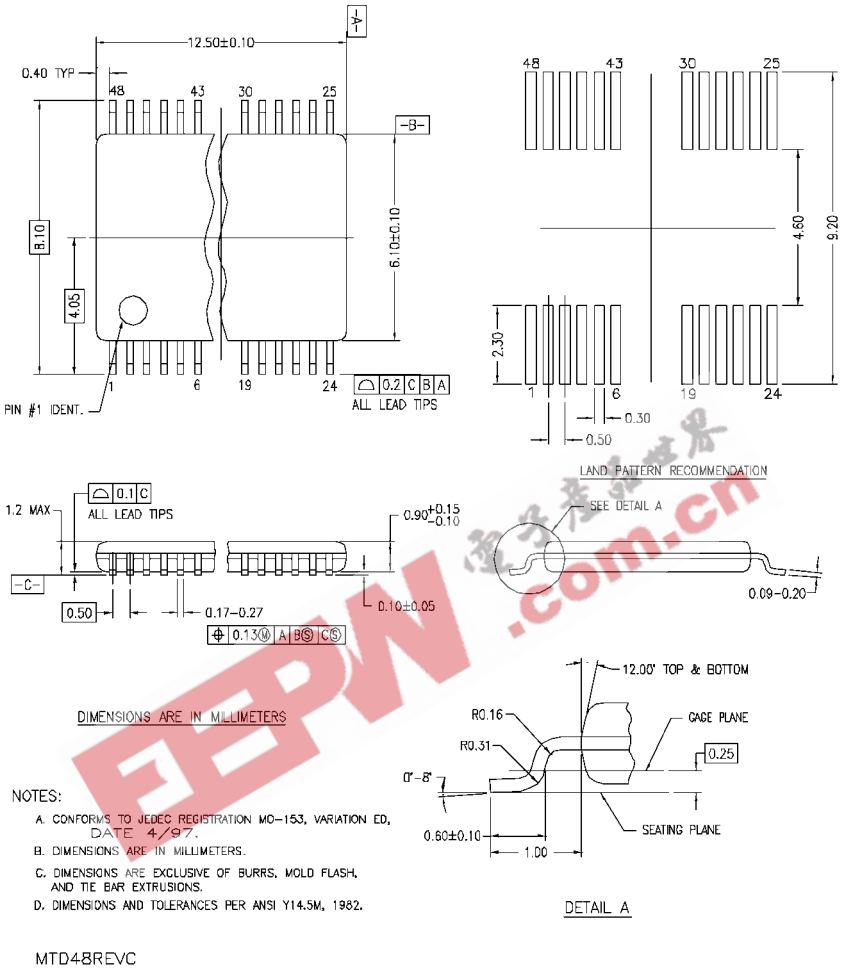
54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com