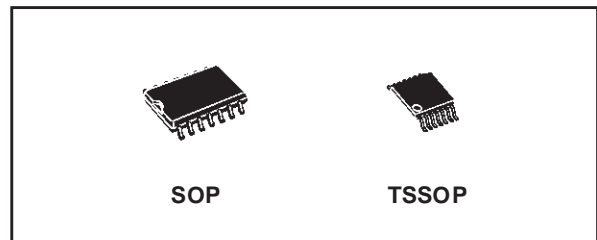


## QUAD EXCLUSIVE OR GATE

- HIGH SPEED:  $t_{PD} = 4.8 \text{ ns}$  (TYP.) at  $V_{CC} = 5V$
- LOW POWER DISSIPATION:  
 $I_{CC} = 2 \mu\text{A}$  (MAX.) at  $T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY:  
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (MIN.)
- POWER DOWN PROTECTION ON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 8 \text{ mA}$  (MIN)
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CC}(\text{OPR}) = 2V \text{ to } 5.5V$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 86
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE:  $V_{OLP} = 0.8V$  (MAX.)



### ORDER CODES

PACKAGE	TUBE	T & R
SOP	74VHC86M	74VHC86MTR
TSSOP		74VHC86TTR

regard to the supply voltage. This device can be used to interface 5V to 3V.

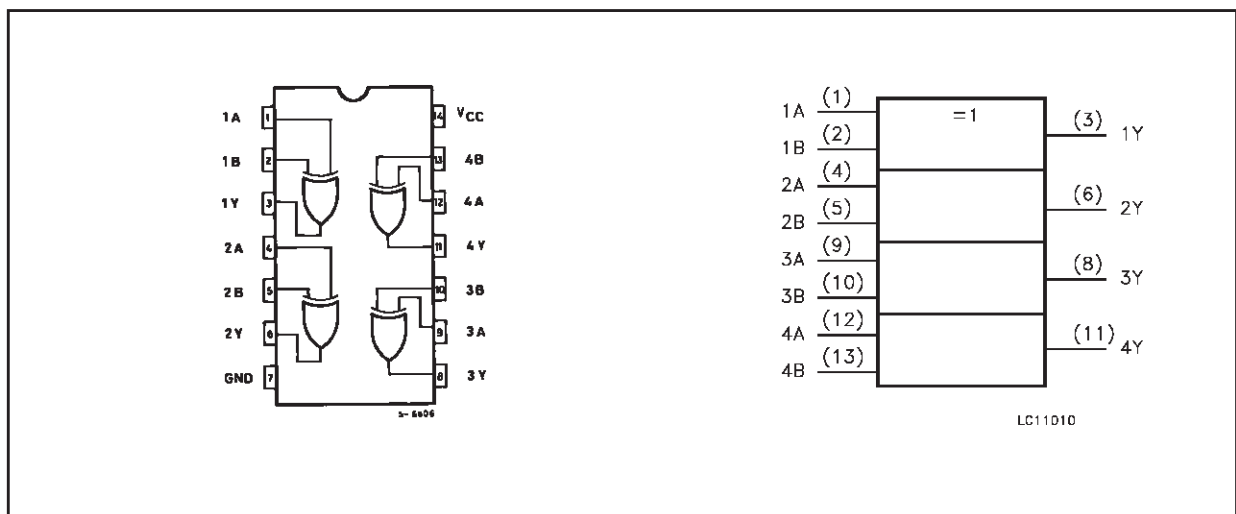
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

### DESCRIPTION

The 74VHC86 is an advanced high-speed CMOS QUAD EXCLUSIVE OR GATE fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no

### PIN CONNECTION AND IEC LOGIC SYMBOLS





## DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>IH</sub>	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		3.0 to 5.5		0.7V <sub>CC</sub>			0.7V <sub>CC</sub>		0.7V <sub>CC</sub>		
V <sub>IL</sub>	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		3.0 to 5.5				0.3V <sub>CC</sub>		0.3V <sub>CC</sub>		0.3V <sub>CC</sub>	
V <sub>OH</sub>	High Level Output Voltage	2.0	I <sub>O</sub> = -50 μA	1.9	2.0		1.9		1.9		V
		3.0	I <sub>O</sub> = -50 μA	2.9	3.0		2.9		2.9		
		4.5	I <sub>O</sub> = -50 μA	4.4	4.5		4.4		4.4		
		3.0	I <sub>O</sub> = -4 mA	2.58			2.48		2.4		
		4.5	I <sub>O</sub> = -8 mA	3.94			3.8		3.7		
V <sub>OL</sub>	Low Level Output Voltage	2.0	I <sub>O</sub> = 50 μA		0.0	0.1		0.1		0.1	V
		3.0	I <sub>O</sub> = 50 μA		0.0	0.1		0.1		0.1	
		4.5	I <sub>O</sub> = 50 μA		0.0	0.1		0.1		0.1	
		3.0	I <sub>O</sub> = 4 mA			0.36		0.44		0.55	
		4.5	I <sub>O</sub> = 8 mA			0.36		0.44		0.55	
I <sub>I</sub>	Input Leakage Current	0 to 5.5	V <sub>I</sub> = 5.5V or GND			± 0.1		± 1		± 1	μA
I <sub>CC</sub>	Quiescent Supply Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND			2		20		20	μA

AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3ns)

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time	3.3 <sup>(*)</sup>	15		7.0	11.0	1.0	13.0	1.0	13.0	ns
		3.3 <sup>(*)</sup>	50		9.5	14.5	1.0	16.5	1.0	16.5	
		5.0 <sup>(**)</sup>	15		4.8	6.8	1.0	8.0	1.0	8.0	
		5.0 <sup>(**)</sup>	50		6.3	8.8	1.0	10.0	1.0	10.0	

(\*) Voltage range is 3.3V ± 0.3V

(\*\*) Voltage range is 5.0V ± 0.5V

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
				T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C <sub>IN</sub>	Input Capacitance				6	10		10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (note 1)				18						pF

1) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I<sub>CC(opr)</sub> = C<sub>PD</sub> × V<sub>CC</sub> × f<sub>IN</sub> + I<sub>CC</sub>/4 (per gate)

## DYNAMIC SWITCHING CHARACTERISTICS

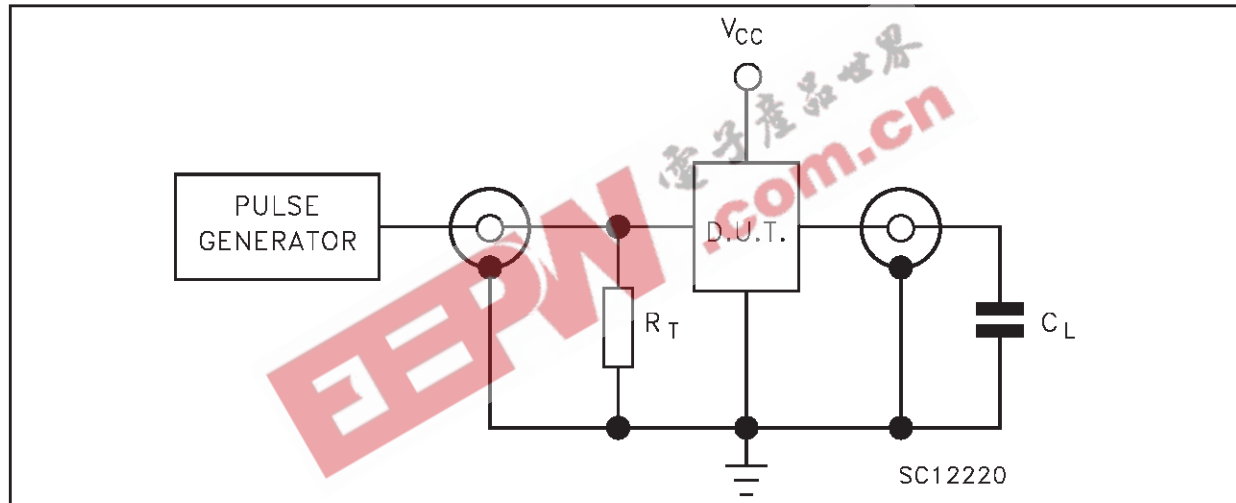
Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)	C <sub>L</sub> = 50 pF	T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>OLP</sub>	Dynamic Low Voltage Quiet Output (note 1, 2)	5.0	C <sub>L</sub> = 50 pF		0.3	0.8					V
V <sub>OLV</sub>				-0.8	-0.3						
V <sub>IHD</sub>	Dynamic High Voltage Input (note 1, 3)	5.0		3.5							V
V <sub>ILD</sub>	Dynamic Low Voltage Input (note 1, 3)	5.0				1.5					V

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 5.0V, (n-1) outputs switching and one output at GND.

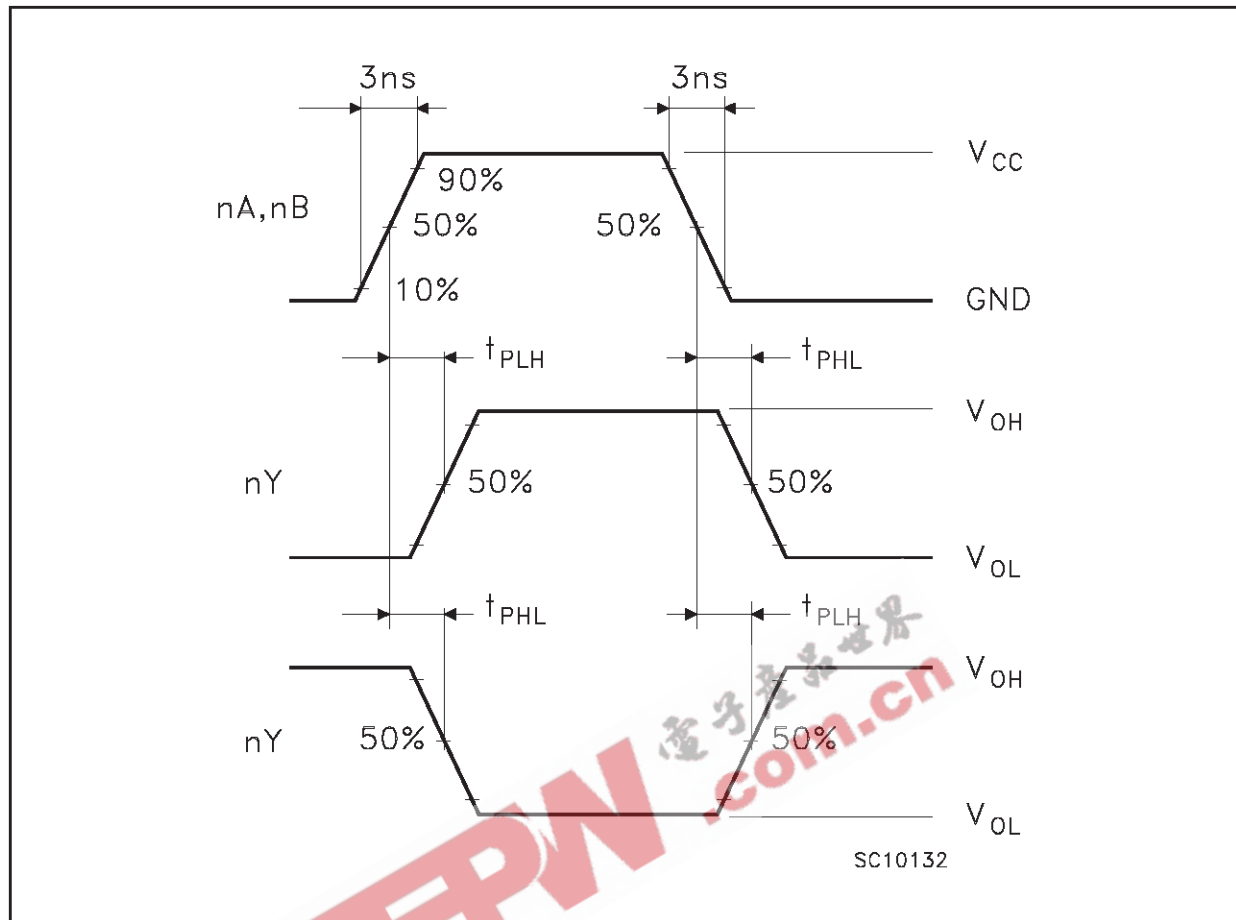
3) Max number of data inputs (n) switching. (n-1) switching 0V to 5.0V. Inputs under test switching: 5.0V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f=1MHz.

## TEST CIRCUIT



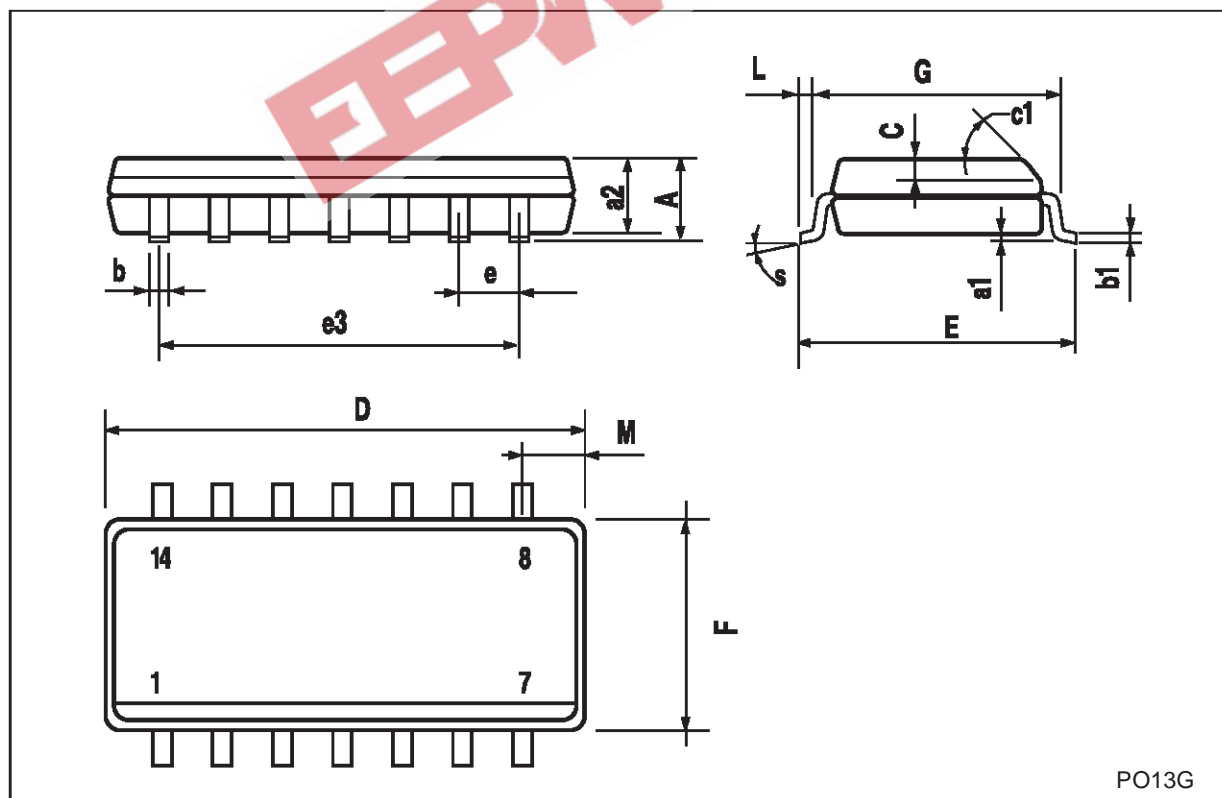
C<sub>L</sub> = 15/50pF or equivalent (includes jig and probe capacitance)

R<sub>T</sub> = Z<sub>OUT</sub> of pulse generator (typically 50Ω)

WAVEFORM: PROPAGATION DELAYS ( $f=1\text{MHz}$ ; 50% duty cycle)

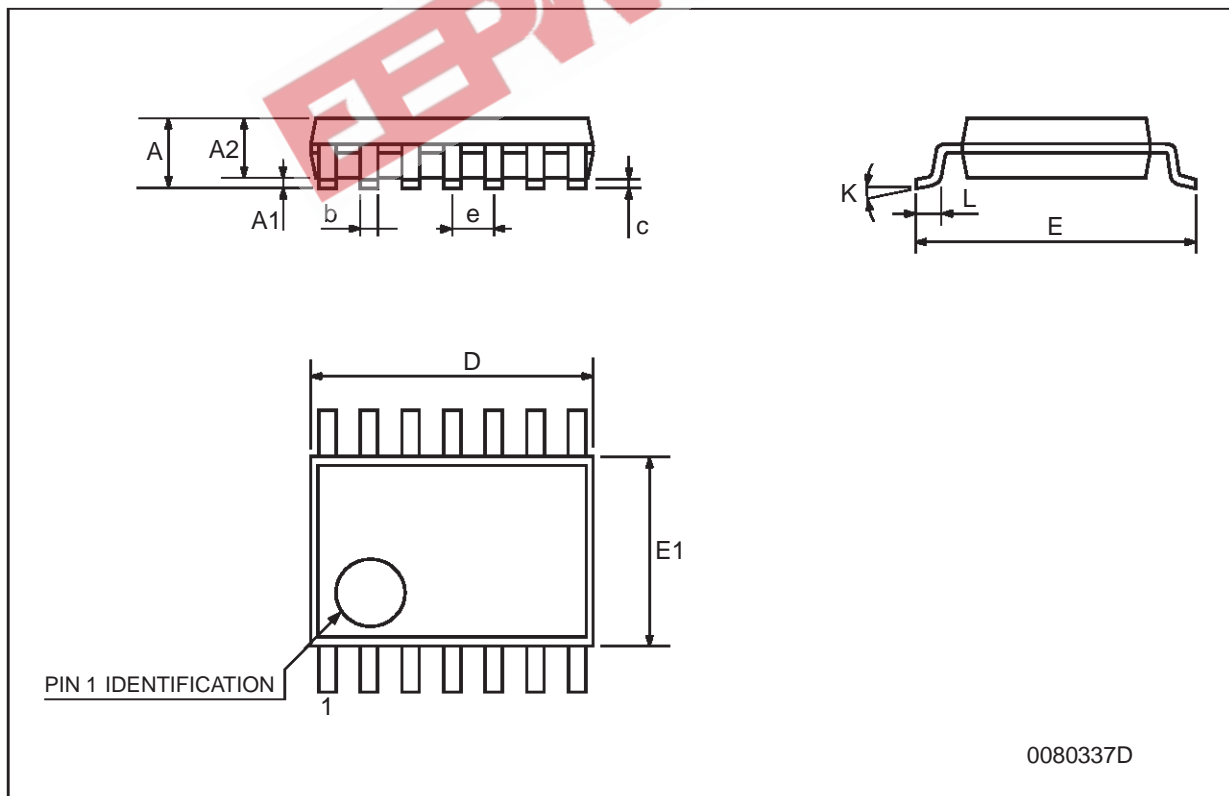
## SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					



## TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



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