



Integrated Device Technology, Inc.

MULTILEVEL PIPELINE REGISTERS

IDT29FCT520AT/BT/CT/DT IDT29FCT521AT/BT/CT/DT

FEATURES:

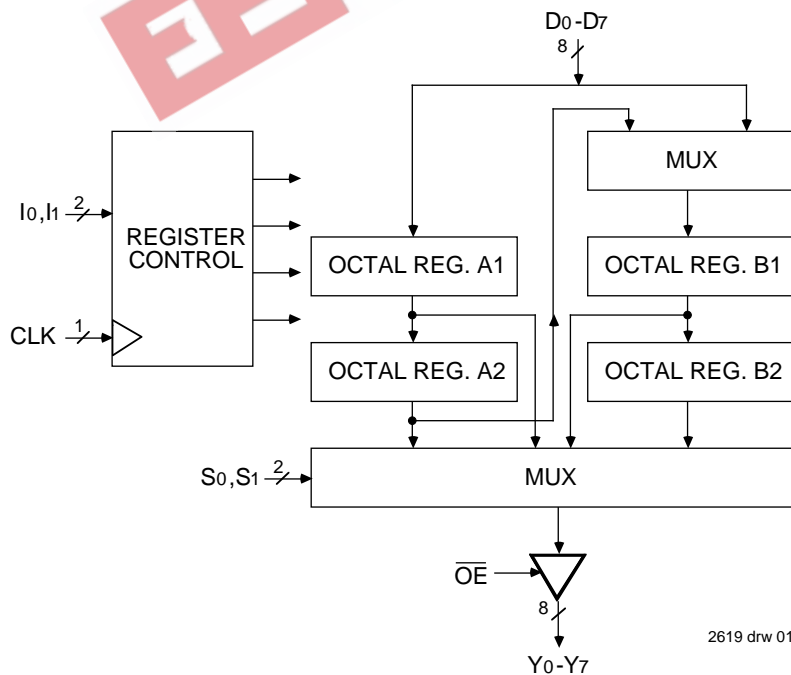
- A, B, C and D speed grades
- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- CMOS power levels
- True TTL input and output compatibility
 - $V_{OH} = 3.3\text{V}$ (typ.)
 - $V_{OL} = 0.3\text{V}$ (typ.)
- High drive outputs (-15mA IOH, 48mA IOL)
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages

DESCRIPTION:

The IDT29FCT520AT/BT/CT/DT and IDT29FCT521AT/BT/CT/DT each contain four 8-bit positive edge-triggered registers. These may be operated as a dual 2-level or as a single 4-level pipeline. A single 8-bit input is provided and any of the four registers is available at the 8-bit, 3-state output.

These devices differ only in the way data is loaded into and between the registers in 2-level operation. The difference is illustrated in Figure 1. In the IDT29FCT520AT/BT/CT/DT when data is entered into the first level ($I = 2$ or $I = 1$), the existing data in the first level is moved to the second level. In the IDT29FCT521AT/BT/CT/DT, these instructions simply cause the data in the first level to be overwritten. Transfer of data to the second level is achieved using the 4-level shift instruction ($I = 0$). This transfer also causes the first level to change. In either part $I=3$ is for hold.

FUNCTIONAL BLOCK DIAGRAM



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MILITARY AND COMMERCIAL TEMPERATURE RANGES

APRIL 1994

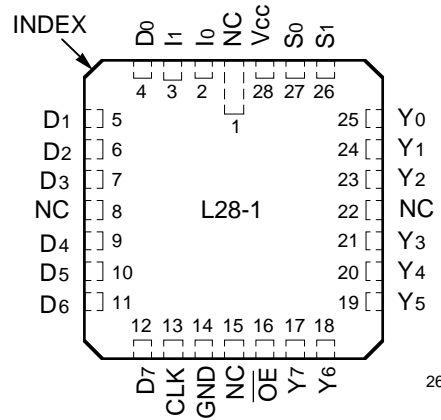
PIN CONFIGURATIONS



2619 drw 02

**DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW**

*FCT520 only



2619 drw 03

**LCC
TOP VIEW**

DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
D _n	Register input Port.
CLK	Clock input. Enter data into registers on LOW-to-HIGH transitions.
I ₀ , I ₁	Instruction inputs. See Figure 1 and instruction Control Tables.
S ₀ , S ₁	Multiplexer select. Inputs either register A ₁ , A ₂ , B ₁ or B ₂ data to be available at the output port.
\overline{OE}	Output enable for 3-state output port.
Y _n	Register output port.

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REGISTER SELECTION

S ₁	S ₀	Register
0	0	B ₂
0	1	B ₁
1	0	A ₂
1	1	A ₁

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NOTE:
1. I = 3 for hold.

Figure 1. Data Loading in 2-Level Operation

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	-0.5 to V _{CC} +0.5	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	0.5	0.5	W
I _{OUT}	DC Output Current	-60 to +120	-60 to +120	mA

NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Input and V_{CC} terminals only.
- Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

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- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V
I _{IH}	Input HIGH Current ⁽⁴⁾	V _{CC} = Max. V _I = 2.7V	—	—	±1	μA
I _{IL}	Input LOW Current ⁽⁴⁾	V _{CC} = Max. V _I = 0.5V	—	—	±1	μA
I _{OZH}	High Impedance ⁽⁴⁾	V _{CC} = Max. V _O = 2.7V	—	—	±1	μA
I _{OZL}	Output Current	V _{CC} = Max. V _O = 0.5V	—	—	±1	μA
I _I	Input HIGH Current ⁽⁴⁾	V _{CC} = Max., V _I = V _{CC} (Max.)	—	—	±1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _N = -18mA	—	-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _O = GND	-60	-120	-225	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	2.4	3.3	—	V
		I _{OH} = -6mA MIL. I _{OH} = -8mA COM'L.				
		I _{OH} = -12mA MIL. I _{OH} = -15mA COM'L.	2.0	3.0	—	
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	—	0.3	0.5	V
		I _{OL} = 32mA MIL. I _{OL} = 48mA COM'L.				
V _H	Input Hysteresis	—	—	200	—	mV
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max. V _{IN} = GND or V _{CC}	—	0.01	1	mA

NOTES:

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- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- The test limit for this parameter is ±5μA at T_A = -55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current, TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$, Outputs Open $\overline{OE} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$, Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = \text{GND}$ One Bit Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.5	3.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	2.0	5.5	
		$V_{CC} = \text{Max.}$, Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = \text{GND}$ Eight Bits Toggling at $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.8	7.3 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	6.0	16.3 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$
 All currents are in milliamps and all frequencies are in megahertz.

2619 tbl 06

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT520AT/521AT				FCT520BT/521BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPHL tPLH	Propagation Delay CLK to Yn	CL = 50pF RL = 500Ω	2.0	14.0	2.0	16.0	2.0	7.5	2.0	8.0	ns
tPHL tPLH	Propagation Delay S0 or S1 to Yn		2.0	13.0	2.0	15.0	2.0	7.5	2.0	8.0	ns
tsu	Set-up Time, HIGH or LOW Dn to CLK		5.0	—	6.0	—	2.5	—	2.8	—	ns
th	Hold Time, HIGH or LOW Dn to CLK		2.0	—	2.0	—	2.0	—	2.0	—	ns
tsu	Set-up Time, HIGH or LOW I0 or I1 to CLK		5.0	—	6.0	—	4.0	—	4.5	—	ns
th	Hold Time, HIGH or LOW I0 or I1 to CLK		2.0	—	2.0	—	2.0	—	2.0	—	ns
tPHZ tPLZ	Output Disable Time		1.5	12.0	1.5	13.0	1.5	7.0	1.5	7.5	ns
tPZH tPZL	Output Enable Time		1.5	15.0	1.5	16.0	1.5	7.5	1.5	8.0	ns
tw	Clock Pulse Width HIGH or LOW		7.0	—	8.0	—	5.5	—	6.0	—	ns

2619 tbl 07

Symbol	Parameter	Condition ⁽¹⁾	FCT520CT/521CT				FCT520DT/521DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPHL tPLH	Propagation Delay CLK to Yn	CL = 50pF RL = 500Ω	2.0	6.0	2.0	7.0	2.0	5.2	—	—	ns
tPHL tPLH	Propagation Delay S0 or S1 to Yn		2.0	6.0	2.0	7.0	2.0	4.8	—	—	ns
tsu	Set-up Time, HIGH or LOW Dn to CLK		2.5	—	2.8	—	1.5	—	—	—	ns
th	Hold Time, HIGH or LOW Dn to CLK		2.0	—	2.0	—	1.0	—	—	—	ns
tsu	Set-up Time, HIGH or LOW I0 or I1 to CLK		4.0	—	4.5	—	2.0	—	—	—	ns
th	Hold Time, HIGH or LOW I0 or I1 to CLK		2.0	—	2.0	—	1.0	—	—	—	ns
tPHZ tPLZ	Output Disable Time		1.5	6.0	1.5	6.0	1.5	4.8	—	—	ns
tPZH tPZL	Output Enable Time		1.5	6.0	1.5	7.0	1.5	4.0	—	—	ns
tw	Clock Pulse Width HIGH or LOW ⁽³⁾		5.5	—	6.0	—	3.0	—	—	—	ns

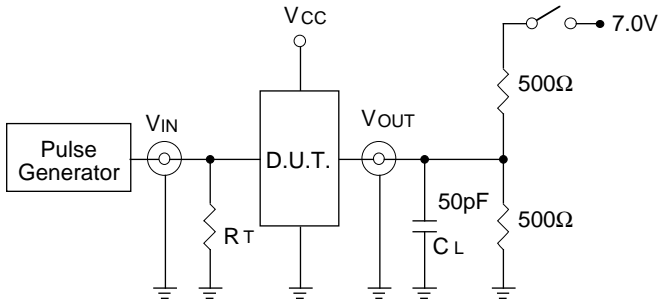
NOTES:

1. See test circuit and waveforms.
2. Minimum units are guaranteed but not tested on Propagation Delays.

2619 tbl 08

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2619 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

CL= Load capacitance: includes jig and probe capacitance.
RT= Termination resistance: should be equal to ZOUT of the Pulse Generator.

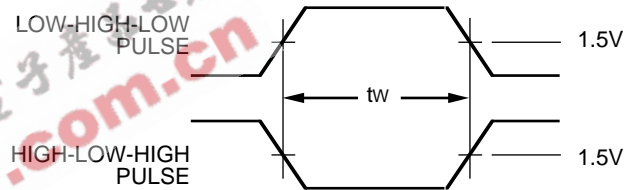
2619 Ink 09

SET-UP, HOLD AND RELEASE TIMES



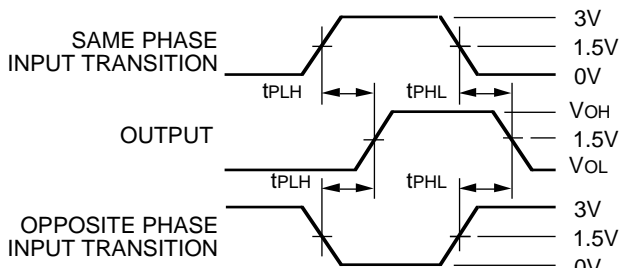
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PULSE WIDTH



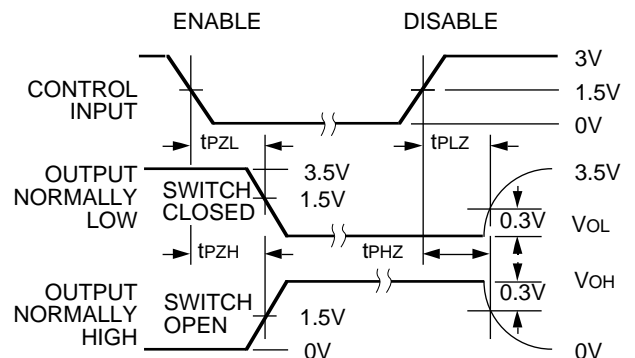
2619 drw 07

PROPAGATION DELAY



2619 drw 08

ENABLE AND DISABLE TIMES

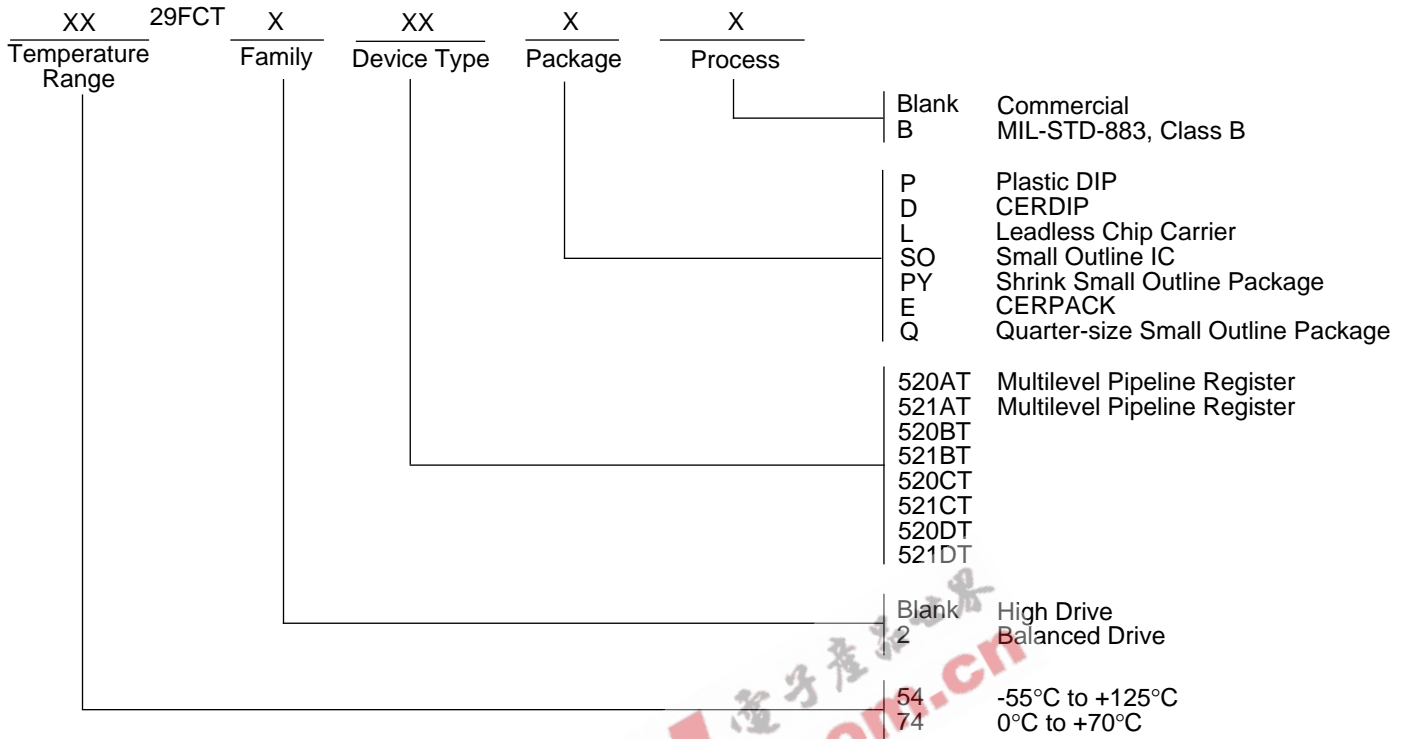


2619 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$

ORDERING INFORMATION



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