DATA SHEET

74F1604
Latch

Product specification

1990 Oct 04

IC15 Data Handbook

Philips
Semiconductors

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Latch 74F1604

FEATURES

- High impedance NPN base inputs for reduced loading (20µA in high and low state)
- Stores 16–bit wide data inputs, multiplexed 8–bit outputs
- Propagation delay 7.0ns typical
- Power supply current 70mA typical

DESCRIPTION

The 74F1604 is a dual octal transparent latch. Organized as 8–bit A and B latches, the latch outputs are connected by pairs to eight 2–input multiplexers. A select (SELECT A/$\overline{B}$) input determines whether the A or B latch contents are multiplexed to the eight outputs. Data from the B inputs are selected when SELECT A/$\overline{B}$ is low; data from the A inputs are selected when SELECT A/$\overline{B}$ is high. Data enters the latch on the falling edge of the latch enable ($\overline{LE}$) input. The latch remains transparent to the data inputs while $\overline{LE}$ is low, and stores the data that is present one setup time before the low–to–high latch enable transition.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1604	7.0ns	70mA

ORDERING INFORMATION

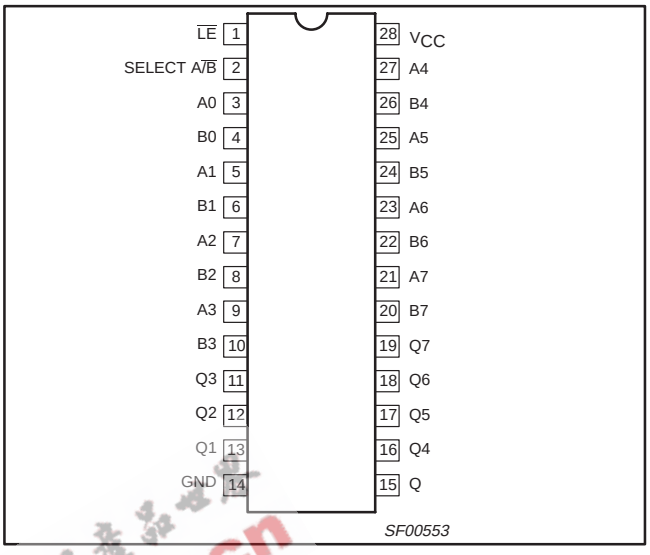
DESCRIPTION	ORDER CODE	
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
28–pin plastic DIP	N74F1604N	SOT117-2
28–pin plastic SOL	N74F1604D	SOT136-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

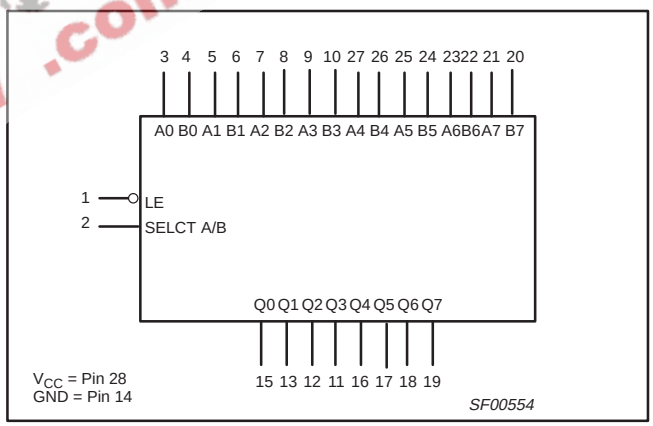
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A7	Data inputs	1.0/0.033	20µA/20µA
B0 – B7	Data inputs	1.0/0.033	20µA/20µA
SELECT A/$\overline{B}$	Select input	1.0/0.033	20µA/20µA
$\overline{LE}$	Latch enable input (active low)	1.0/0.033	20µA/20µA
Q0 – Q7	Data outputs	50/33	1.0mA/20mA

Note to input and output loading and fan out table
One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

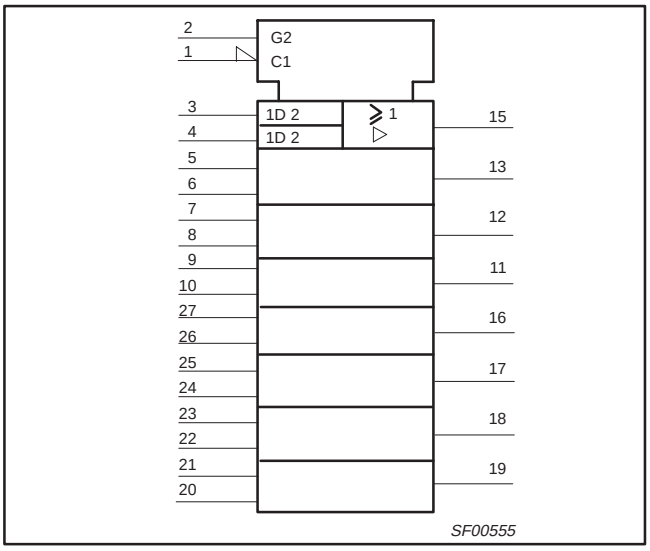
PIN CONFIGURATION



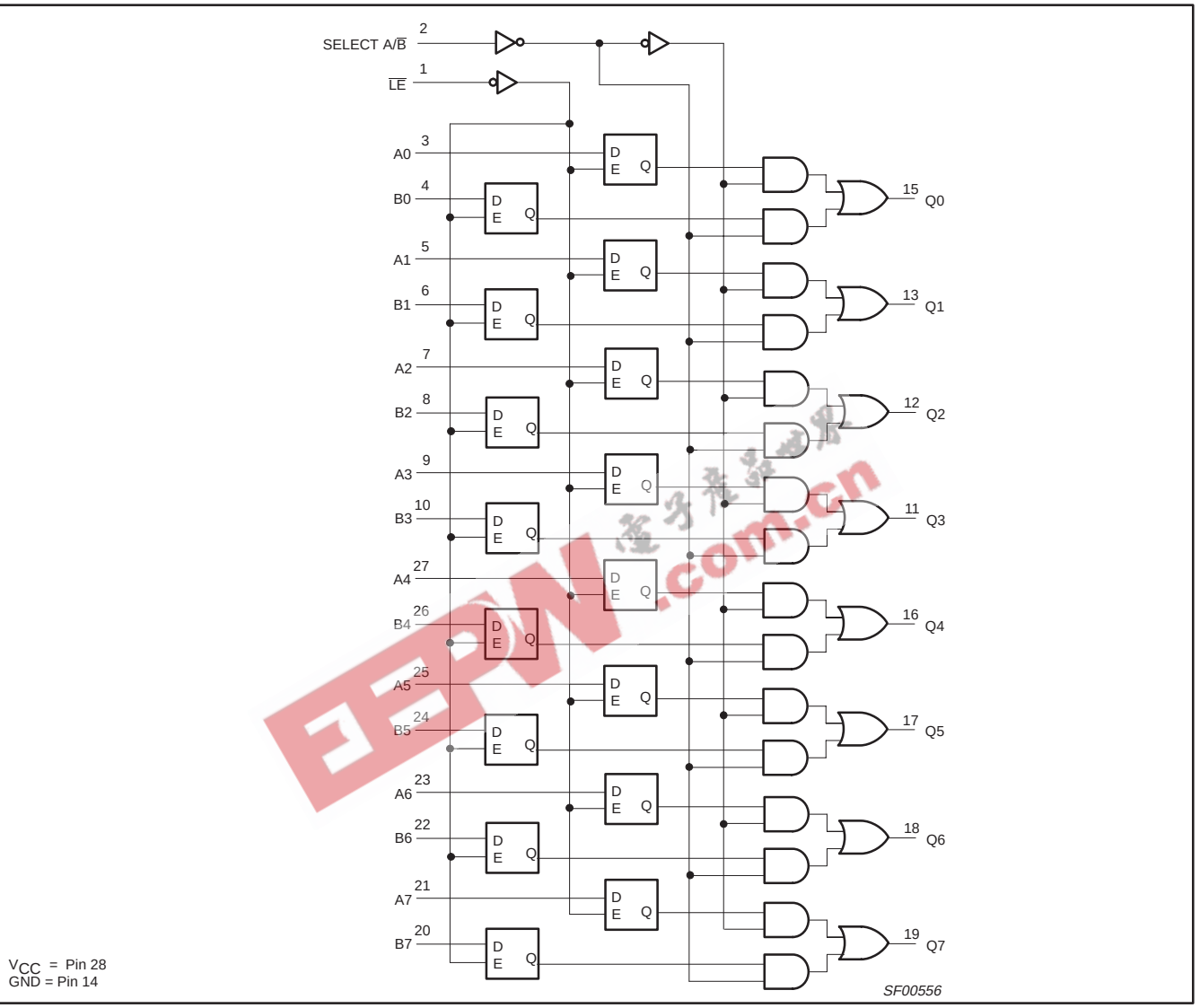
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	OUTPUTS
OPERATING MODE					
A0 – A7	B0 –B7	SELECT A/$\overline{B}$	$\overline{LE}$	Q0 – Q7	
A data	B data	L	L	B data	Enable and read register
A data	B data	H	L	A data	
X	X	X	H	NC	Hold
A data	B data	l	↑	B data	Latch and read register
A data	B data	h	↑	A data	

Notes to function table
H = High–voltage level
h = High–voltage level one setup time before the low–to–high latch enable transition
L = Low–voltage level
l = Low–voltage level one setup time before the low–to–high latch enable transition
NC= No change (If SELECT A/$\overline{B}$ is toggled and the A latched data is different from B latched data then the output will change accordingly.)
X = Don't care
↑ = Low–to–high latch enable transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	40	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{Ik}	Input clamp current			–18	mA
I_{OH}	High–level output current			–1	mA
I_{OL}	Low–level output current			20	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = –3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current		V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OS}	Short–circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				60	80	mA
		I_{CCL}					75	100	mA

Notes to DC electrical characteristics

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

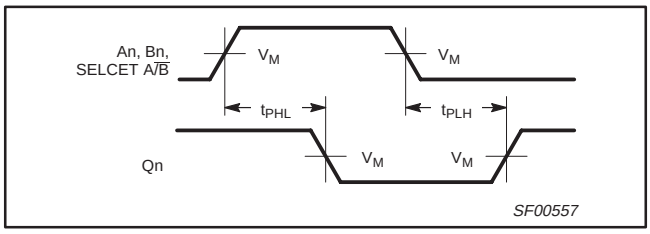
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Qn (non–inverting)	Waveform 2	3.0 3.5	5.5 6.5	8.5 10.0	2.5 3.0	9.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Qn (inverting)	Waveform 1	4.0 2.5	7.0 4.5	10.5 7.5	3.5 2.0	12.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$ to Qn	Waveform 3	6.5 6.0	9.5 9.0	13.0 12.5	5.5 5.0	15.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay An or Bn to Qn	Waveform 1, 2	4.0 4.0	6.5 7.0	9.5 10.5	3.5 3.5	10.5 12.5	ns

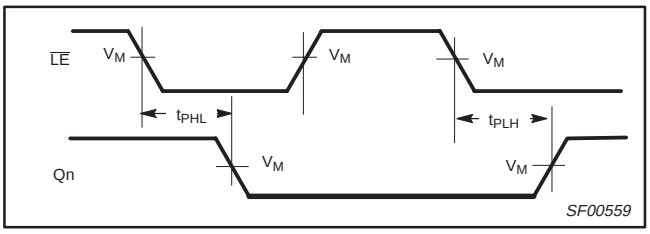
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_D = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_D= 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Setup time, high or low An, Bn to $\overline{LE}$	Waveform 4	0.0 1.0			0.0 3.5		ns
t_h (H) t_h (L)	Hold time, high or low An, Bn to $\overline{LE}$	Waveform 4	1.5 3.0			2.0 3.5		ns
t_w (L)	$\overline{LE}$ Pulse width, low	Waveform 4	6.5			7.5		ns

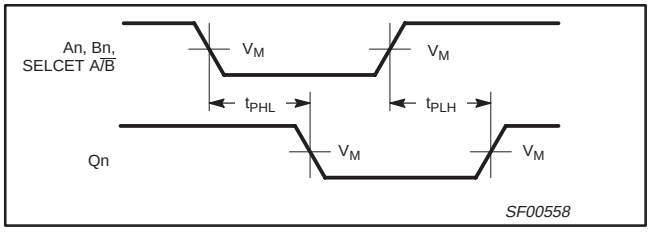
AC WAVEFORMS



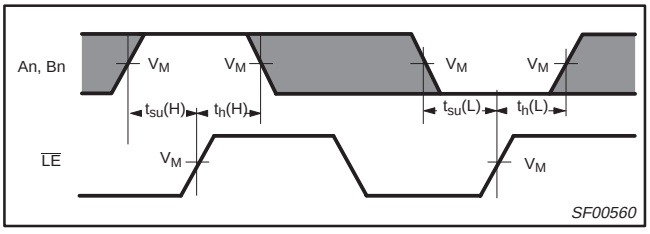
Waveform 1. Propagation delay for SELECT A/$\overline{B}$ to output (A register stored data = low) or An. Bn to output



Waveform 3. Propagation delay for latch enable to output



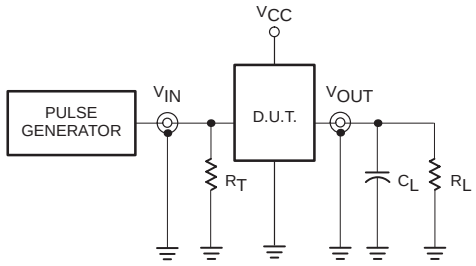
Waveform 2. Propagation delay for SELECT A/$\overline{B}$ to output (A register stored data = low) or An. Bn to output



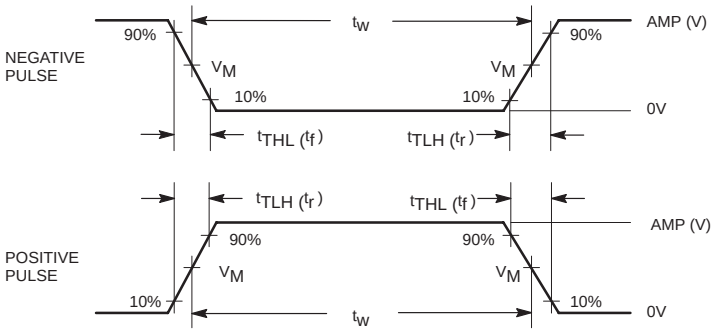
Waveform 4. Setup time and hold times and $\overline{LE}$ pulse width

Note to AC waveforms
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

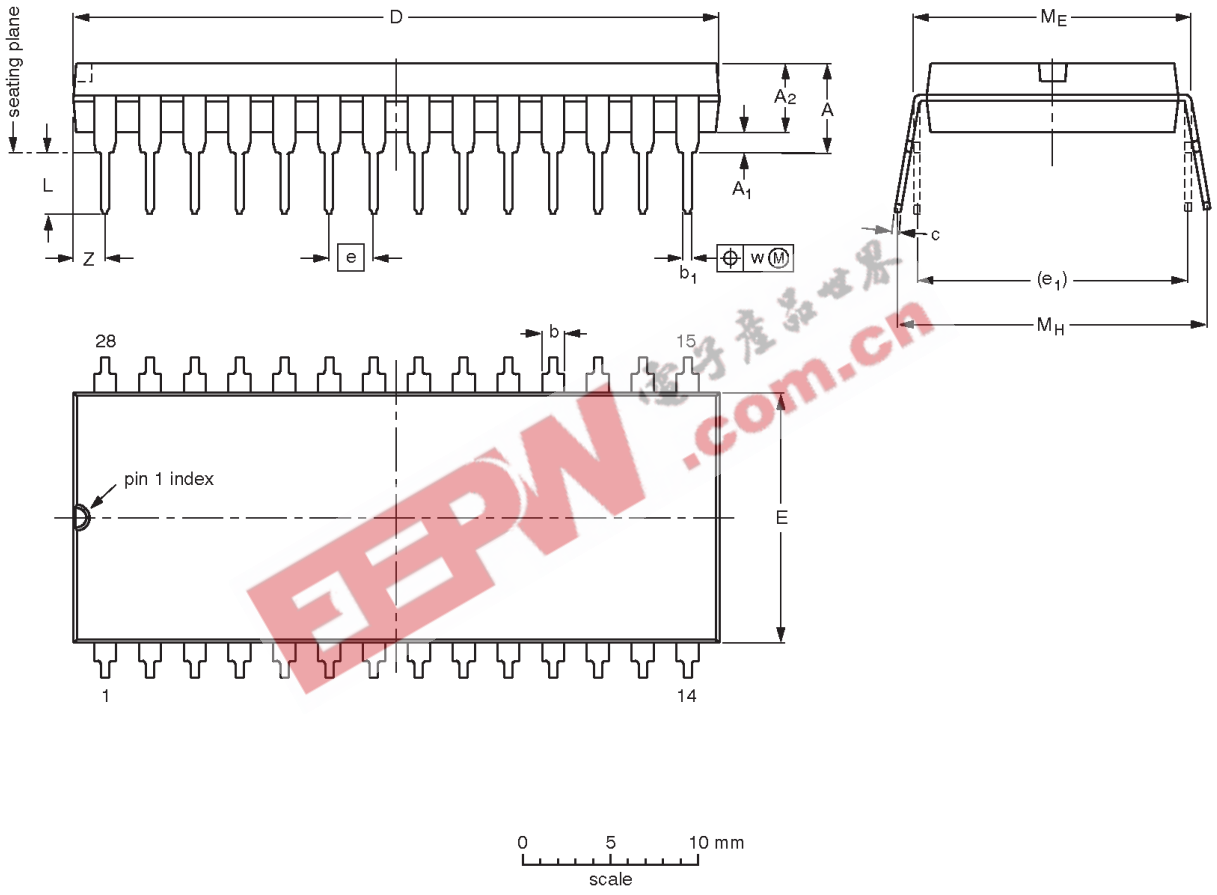
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

DIP28: plastic dual in-line package; 28 leads (600 mil); long body SOT117-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

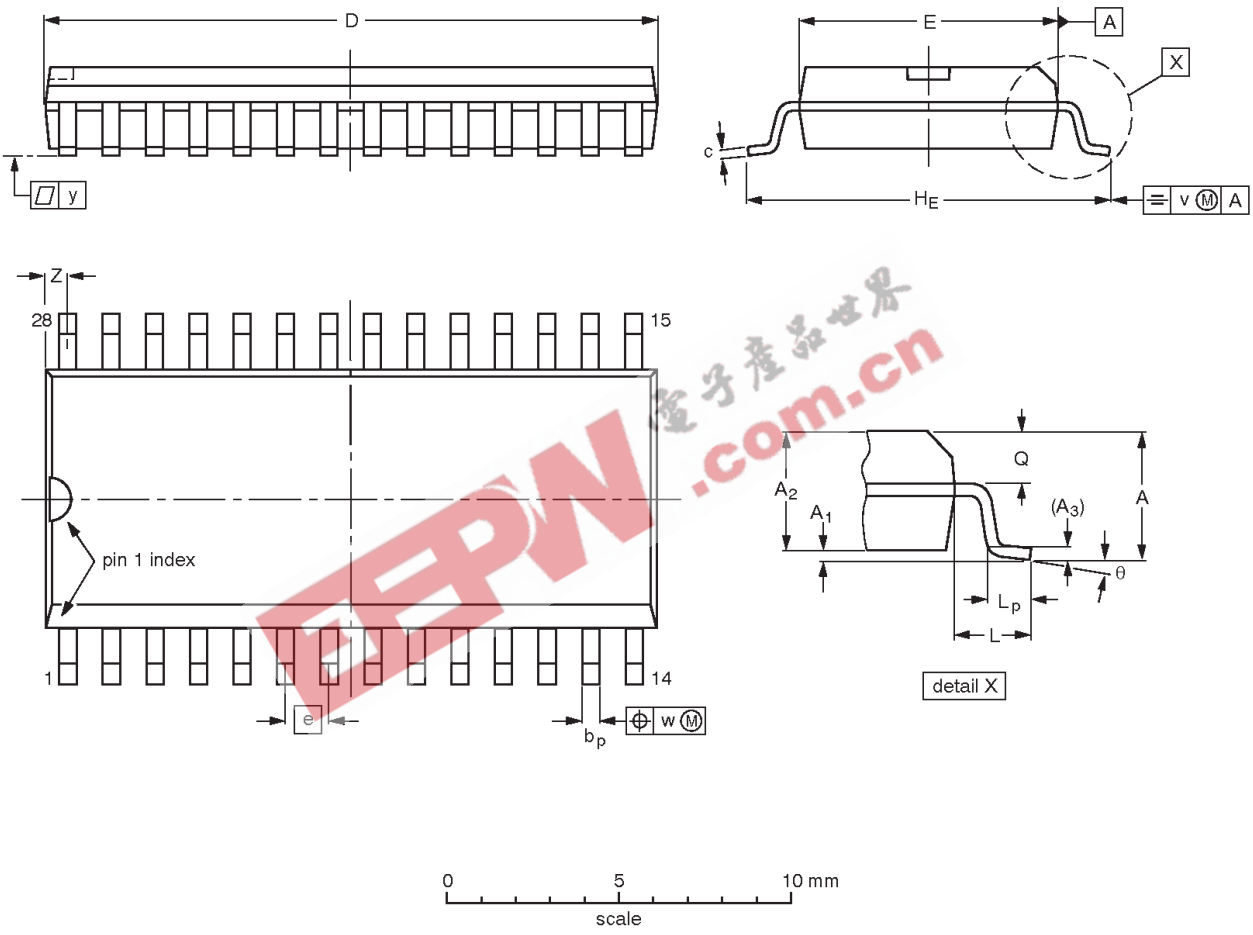
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	3.94	1.63 1.14	0.56 0.43	0.38 0.25	37.08 35.94	14.22 13.84	2.54	15.24	3.51 3.05	15.75 15.24	17.65 15.24	0.25	2.10
inches	0.200	0.020	0.155	0.064 0.045	0.022 0.017	0.015 0.010	1.460 1.415	0.560 0.545	0.100	0.600	0.138 0.120	0.62 0.60	0.695 0.600	0.01	0.083

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-2		MS-011AB				95-03-11

SO28: plastic small outline package; 28 leads; body width 7.5mm SOT136-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~95-01-24~~ 97-05-22

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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