

# 74FST3245

## 8-Bit Bus Switch

The ON Semiconductor 74FST3245 is an 8-bit, high performance switch. The device is CMOS TTL compatible when operating between 4 and 5.5 Volts. The device exhibits extremely low  $R_{ON}$  and adds nearly zero propagation delay. The device adds no noise or ground bounce to the system.

The device consists of an 8-bit switch. Port A is connected to Port B when  $\overline{OE}$  is low. If  $\overline{OE}$  is high, the switch is high Z.

- $R_{ON} < 4 \Omega$  Typical
- Less Than 0.25 ns–Max Delay Through Switch
- Nearly Zero Standby Current
- No Circuit Bounce
- Control Inputs are TTL/CMOS Compatible
- Pin-For-Pin Compatible with QS3245, FST3245, CBT3245
- All Popular Packages: QSOP–20, TSSOP–20, SOIC–20

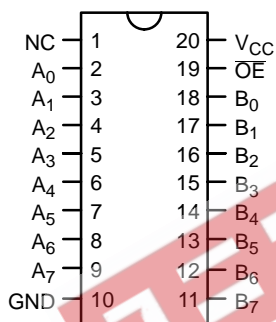


Figure 1. 20-Lead Pinout

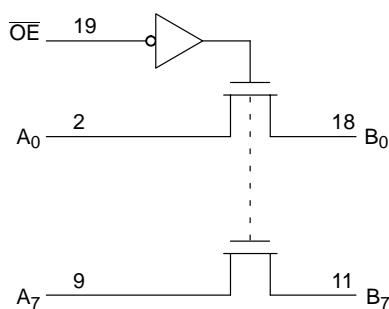


Figure 2. Logic Diagram

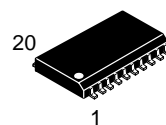
### TRUTH TABLE

Input OE	Function
L	Connect
H	Disconnect

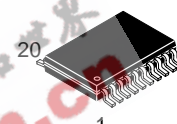


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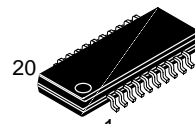
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SO–20  
DW SUFFIX  
CASE 751D

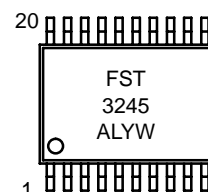
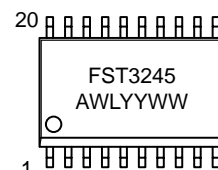


TSSOP–20  
DT SUFFIX  
CASE 948E



QSOP–20  
QS SUFFIX  
CASE 492A

### MARKING DIAGRAMS



A = Assembly Location  
L, WL = Wafer Lot  
Y = Year  
W, WW = Work Week

### PIN NAMES

Pin	Description
$\overline{OE}_1, \overline{OE}_2$	Bus Switch Enables
1A, 2A	Bus A
1B, 2B	Bus B

### ORDERING INFORMATION

Device	Package	Shipping
74FST3245DW	SO–20	38 Units/Rail
74FST3245DWR2	SO–20	1000 Units/Reel
74FST3245DT	TSSOP–20	75 Units/Rail
74FST3245DTR2	TSSOP–20	2500 Units/Reel
74FST3245QS	QSOP–20	55 Units/Rail
74FST3245QSR	QSOP–20	2500 Units/Reel

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## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0	V
V <sub>I</sub>	DC Input Voltage	-0.5 to +7.0	V
V <sub>O</sub>	DC Output Voltage	-0.5 to +7.0	V
I <sub>IK</sub>	DC Input Diode Current V <sub>I</sub> < GND	-50	mA
I <sub>OK</sub>	DC Output Diode Current V <sub>O</sub> < GND	-50	mA
I <sub>O</sub>	DC Output Sink Current	128	mA
I <sub>CC</sub>	DC Supply Current per Supply Pin	± 100	mA
I <sub>GND</sub>	DC Ground Current per Ground Pin	± 100	mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T <sub>J</sub>	Junction Temperature Under Bias	+150	°C
θ <sub>JA</sub>	Thermal Resistance (Note 1) SOIC TSSOP QSOP	96 128 200	°C/W
MSL	Moisture Sensitivity	Level 1	
F <sub>R</sub>	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V <sub>ESD</sub>	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3)	>2000 >200	V
I <sub>LATCH-UP</sub>	Latch-Up Performance Above V <sub>CC</sub> and Below GND at 85°C (Note 4)	± 500	mA

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to EIA/JESD78.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage Operating, Data Retention Only	4.0	5.5	V
V <sub>I</sub>	Input Voltage (Note )	0	5.5	V
V <sub>O</sub>	Output Voltage (HIGH or LOW State)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Free-Air Temperature	-40	+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate Switch Control Input Switch I/O	0 0	5 DC	ns/V

5. Unused control inputs may not be left open. All control inputs must be tied to a high or low logic input voltage level.

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### DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C			Unit
				Min	Typ*	Max	
V <sub>IK</sub>	Clamp Diode Resistance	I <sub>IN</sub> = -18mA	4.5			-1.2	V
V <sub>IH</sub>	High-Level Input Voltage		4.0 to 5.5	2.0			V
V <sub>IL</sub>	Low-Level Input Voltage		4.0 to 5.5			0.8	V
I <sub>I</sub>	Input Leakage Current	0 ≤ V <sub>IN</sub> ≤ 5.5 V	5.5			±1.0	μA
I <sub>OZ</sub>	OFF-STATE Leakage Current	0 ≤ A, B ≤ V <sub>CC</sub>	5.5			±1.0	μA
R <sub>ON</sub>	Switch On Resistance (Note 6)	V <sub>IN</sub> = 0 V, I <sub>IN</sub> = 64 mA	4.5		4	7	Ω
		V <sub>IN</sub> = 0 V, I <sub>IN</sub> = 30 mA	4.5		4	7	
		V <sub>IN</sub> = 2.4 V, I <sub>IN</sub> = 15 mA	4.5		8	15	
		V <sub>IN</sub> = 2.4 V, I <sub>IN</sub> = 15 mA	4.0		11	20	
I <sub>CC</sub>	Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND, I <sub>OUT</sub> = 0	5.5			3	μA
ΔI <sub>CC</sub>	Increase In I <sub>CC</sub> per Input	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5			2.5	mA

\*Typical values are at V<sub>CC</sub> = 5.0 V and T<sub>A</sub> = 25°C.

6. Measured by the voltage drop between A and B pins at the indicated current through the switch.

### AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Figures	Limits				Unit
				T <sub>A</sub> = -40°C to +85°C				
				V <sub>CC</sub> = 4.5 to 5.5 V		V <sub>CC</sub> = 4.0 V		
Min	Max	Min	Max					
t <sub>PHL</sub> , t <sub>PLH</sub>	Prop Delay Bus to Bus (Note 7)	V <sub>I</sub> = OPEN	3 and 4		0.25		0.25	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Output Enable Time	V <sub>I</sub> = 7 V for t <sub>PZL</sub> V <sub>I</sub> = OPEN for t <sub>PZH</sub>	3 and 4	1.5	5.9		6.4	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time	V <sub>I</sub> = 7 V for t <sub>PLZ</sub> V <sub>I</sub> = OPEN for t <sub>PHZ</sub>	3 and 4	1.5	6.0		5.7	ns

7. This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

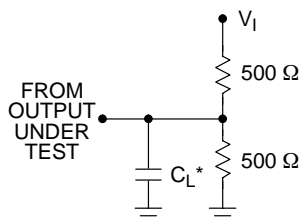
### CAPACITANCE (Note 8)

Symbol	Parameter	Conditions	Typ	Max	Unit
C <sub>IN</sub>	Control Pin Input Capacitance	V <sub>CC</sub> = 5.0 V	3		pF
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>CC</sub> , $\overline{OE}$ = 5.0 V	5		pF

8. T<sub>A</sub> = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

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## AC Loading and Waveforms

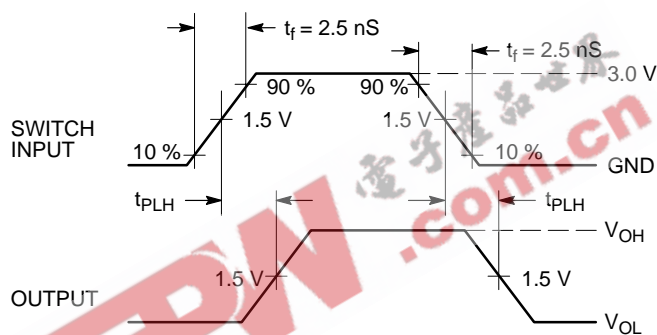


**NOTES:**

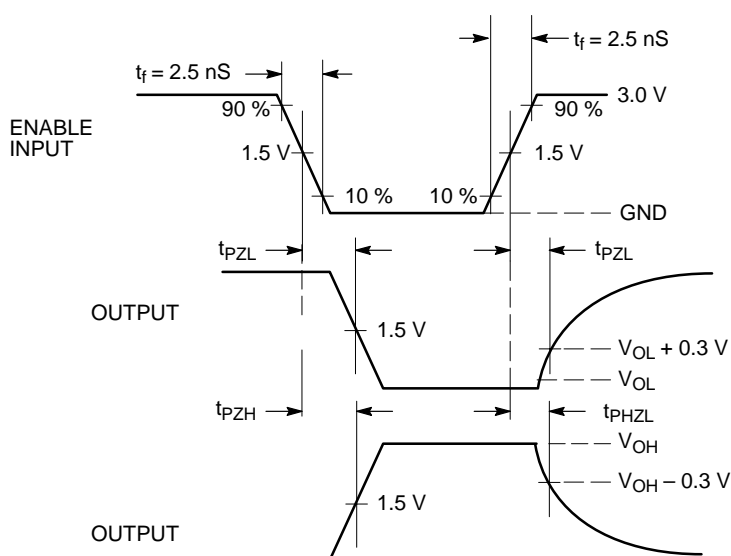
1. Input driven by 50 Ω source terminated in 50 Ω.
2. C<sub>L</sub> includes load and stray capacitance.

\*C<sub>L</sub> = 50 pF

**Figure 3. AC Test Circuit**



**Figure 4. Propagation Delays**

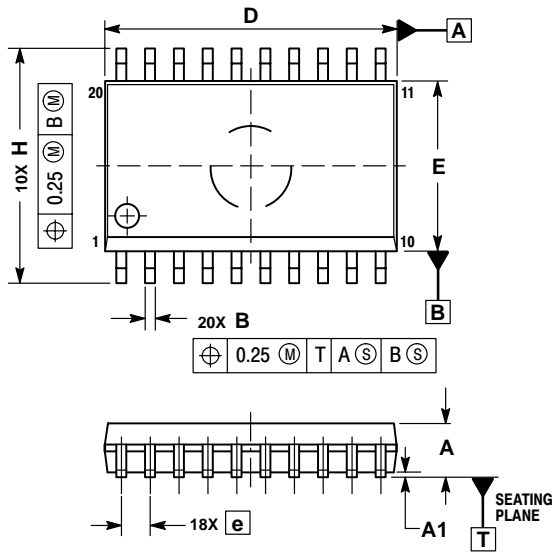


**Figure 5. Enable/Disable Delays**

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## PACKAGE DIMENSIONS

SO-20  
DW SUFFIX  
CASE 751D-05  
ISSUE F



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

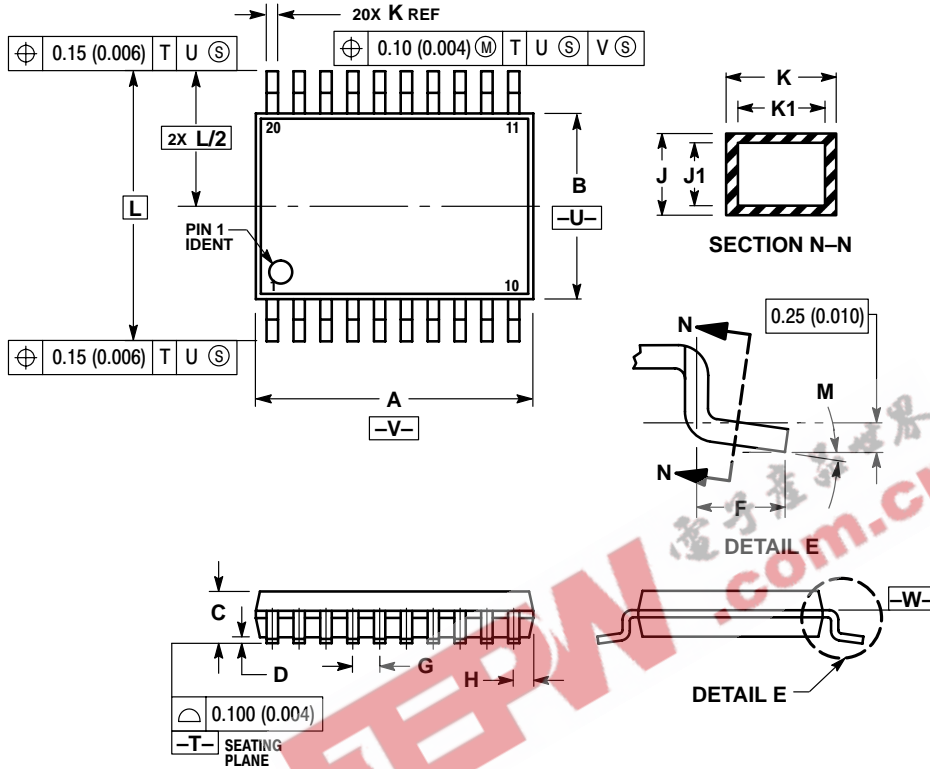
DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
$\theta$	0°	7°

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## PACKAGE DIMENSIONS

TSSOP-20  
DT SUFFIX  
CASE 948E-02  
ISSUE A



### NOTES:

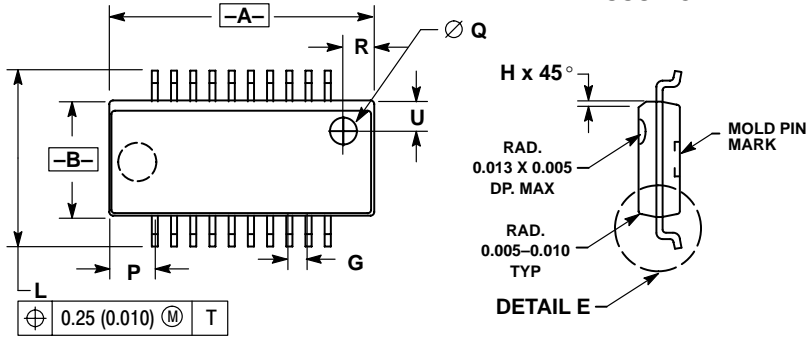
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE  $-W-$ .

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

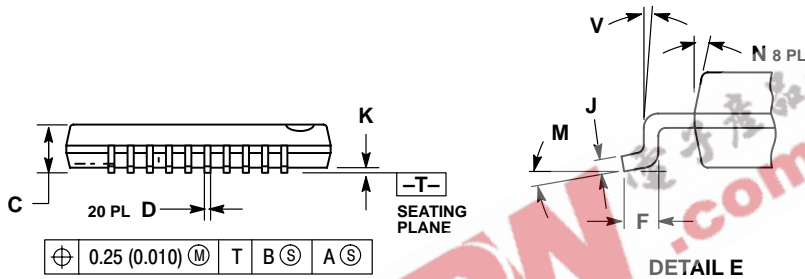
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## PACKAGE DIMENSIONS

QSOP-20  
QS SUFFIX  
CASE 492A-01  
ISSUE O



⊕	0.25 (0.010)	Ⓜ	T
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⊕	0.25 (0.010)	Ⓜ	T	B Ⓢ	A Ⓢ
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### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. THE BOTTOM PACKAGE SHALL BE BIGGER THAN THE TOP PACKAGE BY 4 MILS (NOTE: LEAD SIDE ONLY). BOTTOM PACKAGE DIMENSION SHALL FOLLOW THE DIMENSION STATED IN THIS DRAWING.
4. PLASTIC DIMENSIONS DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 6 MILS PER SIDE.
5. BOTTOM EJECTOR PIN WILL INCLUDE THE COUNTRY OF ORIGIN (COO) AND MOLD CAVITY I.D.

DIM	INCHES		MILLIMETERS	
	MAX	MIN	MAX	MIN
A	0.337	0.344	8.56	8.74
B	0.150	0.157	3.81	3.99
C	0.061	0.068	1.55	1.73
D	0.008	0.012	0.20	0.31
F	0.016	0.035	0.41	0.89
G	0.025 BSC		0.64 BSC	
H	0.008	0.018	0.20	0.46
J	0.0098	0.0075	0.249	0.191
K	0.004	0.010	0.10	0.25
L	0.230	0.244	5.84	6.20
M	0°	8°	0°	8°
N	0°	7°	0°	7°
P	0.052	0.062	1.32	1.58
Q	0.035 DIA		0.89 DIA	
R	0.035	0.045	0.89	1.14
U	0.035	0.045	0.89	1.14
V	0°	8°	0°	8°

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