

54AC/74AC125 • 74ACT125 Quad Buffer with TRI-STATE® Outputs

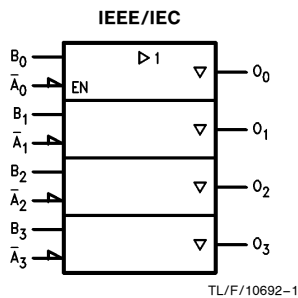
General Description

The 'AC/'ACT125 contains four independent non-inverting buffers with TRI-STATE outputs.

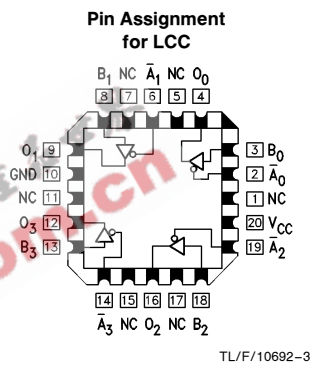
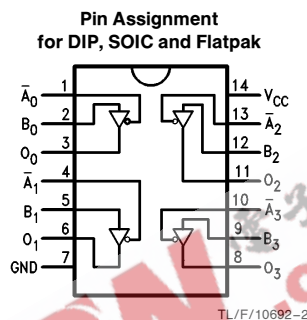
Features

- I_{CC} reduced by 50%
- Outputs source/sink 24 mA
- 'ACT125 has TTL-compatible outputs

Logic Symbol



Connection Diagrams



Pin Names	Description
$\bar{A}_n, B_n$	Inputs
O_n	Outputs

Function Table

Inputs		Output
A_n	B_n	O_n
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
Z = HIGH Impedance
X = Immaterial

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_K)	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V _{CC} (V)	74AC		54AC	74AC	Units	Conditions
			T _A = +25°C		T _A = −55°C to +125°C	T _A = −40°C to +85°C		
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I _{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA
		4.5		3.86	3.7	3.76		
		5.5		4.86	4.7	4.76		
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
		4.5		0.36	0.50	0.44		
		5.5		0.36	0.50	0.44		
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V _I = V _{CC} , GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	74AC		54AC		74AC		Units	Conditions
			T _A = + 25°C		T _A = − 55°C to + 125°C		T _A = − 40°C to + 85°C			
			Typ	Guaranteed Limits						
I _{OZ}	Maximum TRI-STATE Current	5.5		±0.5	±10.0		±5.0		μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5			50		75		mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5			− 50		− 75		mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0		40.0		μA	V _{IN} = V _{CC} or GND

†Maximum test duration 2.0 ms, one output loaded at a time.

Note : I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT	Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C		
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} −24 mA
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND
I _{OZ}	Maximum TRI-STATE Current	5.5		±0.5	±5.0	μA	V _I = V _{IL} , V _{IH} V _O = V _{CC} , GND
I _{CC} T	Maximum I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} − 2.1V‡
I _{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

‡May be measured per the JEDEC Alternate Method.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} * (V)	74AC			54AC		74AC		Units
			T _A = + 25°C C _L = 50 pF			T _A = −55°C to + 125°C C _L = 50 pF		T _A = −40°C to + 85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay Data to Output	3.3 5.0	1.0 1.0	6.5 5.5	9.0 7.0			1.0 1.0	10.0 7.5	ns
t _{PHL}	Propagation Delay Data to Output	3.3 5.0	1.0 1.0	6.5 5.0	9.0 7.0			1.0 1.0	10.0 7.5	ns
t _{PZH}	Output Enable Time	3.3 5.0	1.0 1.0	6.0 5.0	10.5 7.0			1.0 1.0	11.0 8.0	ns
t _{PZL}	Output Enable Time	3.3 5.0	1.0 1.0	7.5 5.5	10.0 8.0			1.0 1.0	11.0 8.5	ns
t _{PHZ}	Output Disable Time	3.3 5.0	1.0 1.0	7.5 6.5	10.0 9.0			1.0 1.0	10.5 9.5	ns
t _{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	7.5 6.5	10.5 9.0			1.0 1.0	11.5 9.5	ns

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay Data to Output	5.0	1.0	6.5	9.0	1.0	10.0	ns
t _{PHL}	Propagation Delay Data to Output	5.0	1.0	7.0	9.0	1.0	10.0	ns
t _{PZH}	Output Enable Time	5.0	1.0	6.0	8.5	1.0	9.5	ns
t _{PZL}	Output Enable Time	5.0	1.0	7.0	9.5	1.0	10.5	ns
t _{PHZ}	Output Disable Time	5.0	1.0	7.0	9.5	1.0	10.5	ns
t _{PLZ}	Output Disable Time	5.0	1.0	7.5	10.0	1.0	10.5	ns

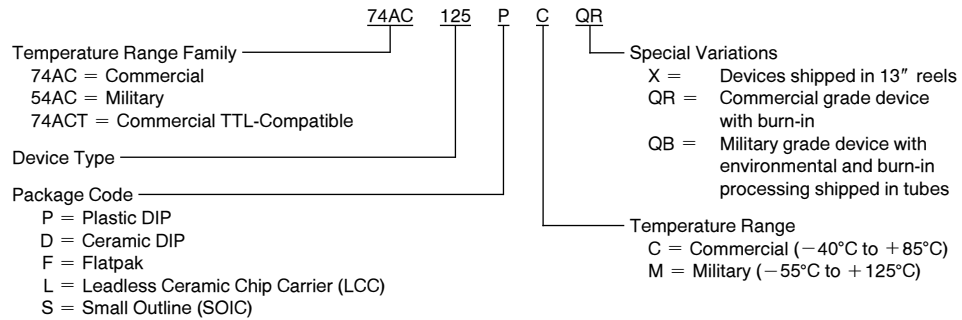
*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT	Units	Conditions
		Typ		
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	45.0	pF	V _{CC} = 5.0V

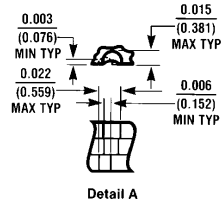
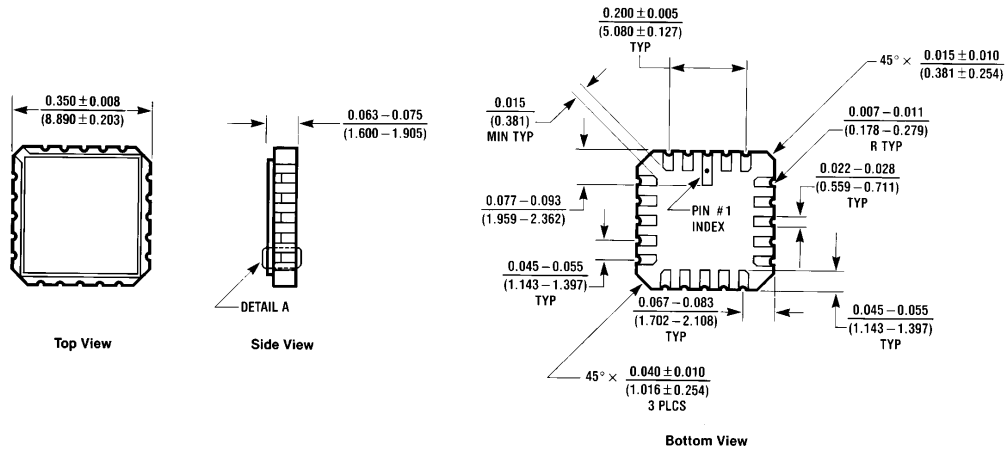
Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



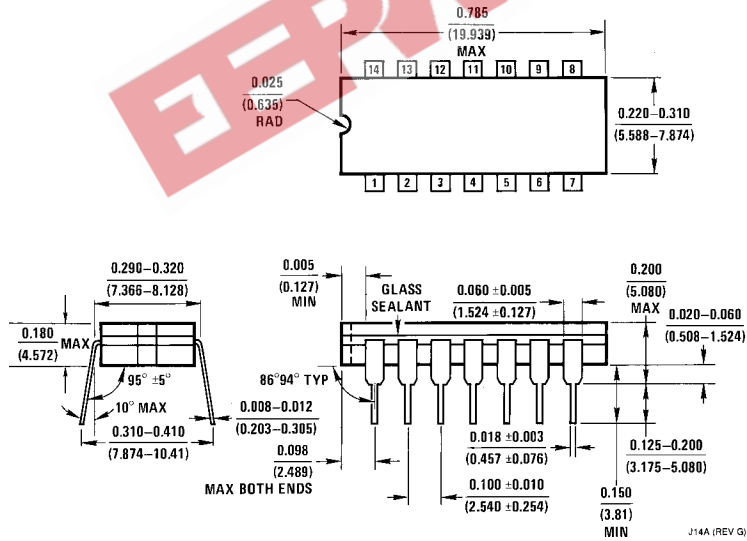
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Physical Dimensions inches (millimeters)



20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

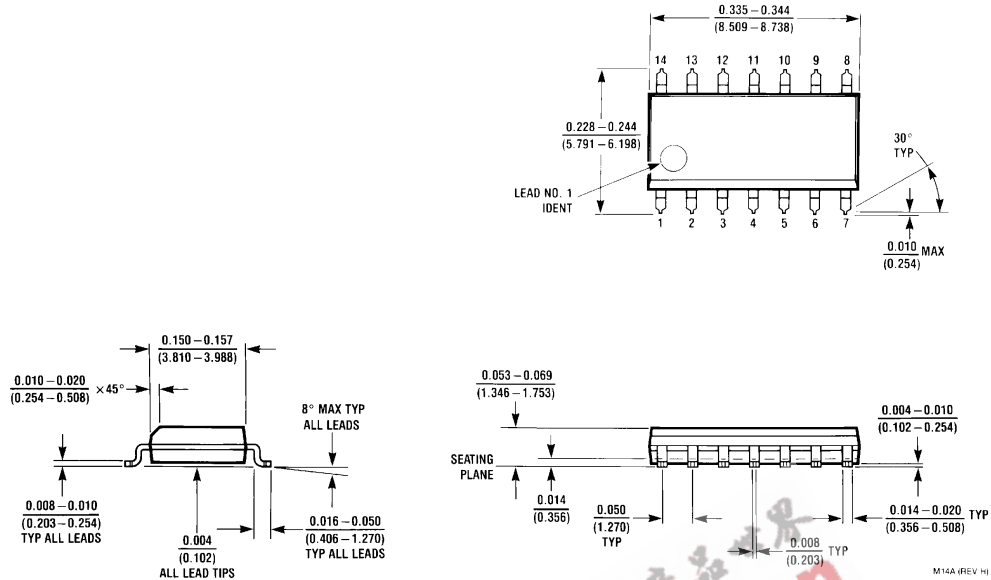
E20A (REV D)



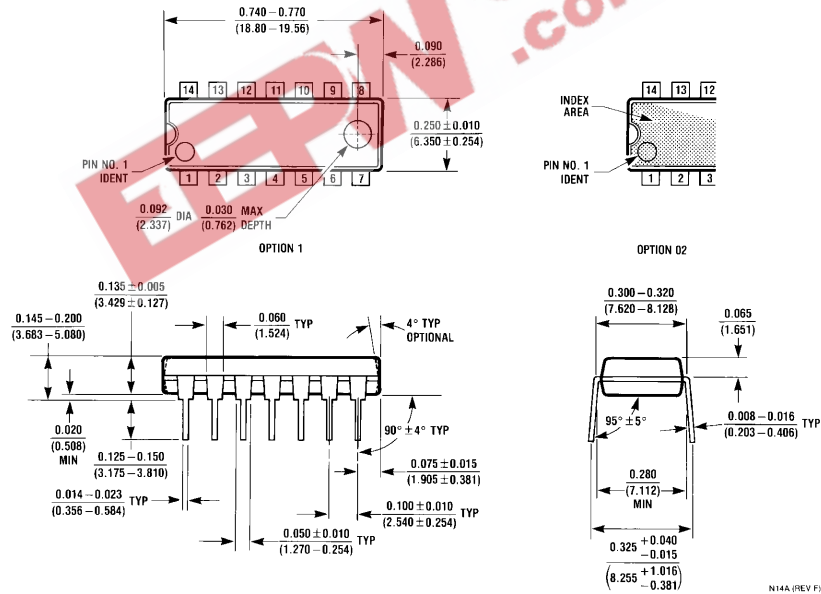
14-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J14A

J14A (REV G)

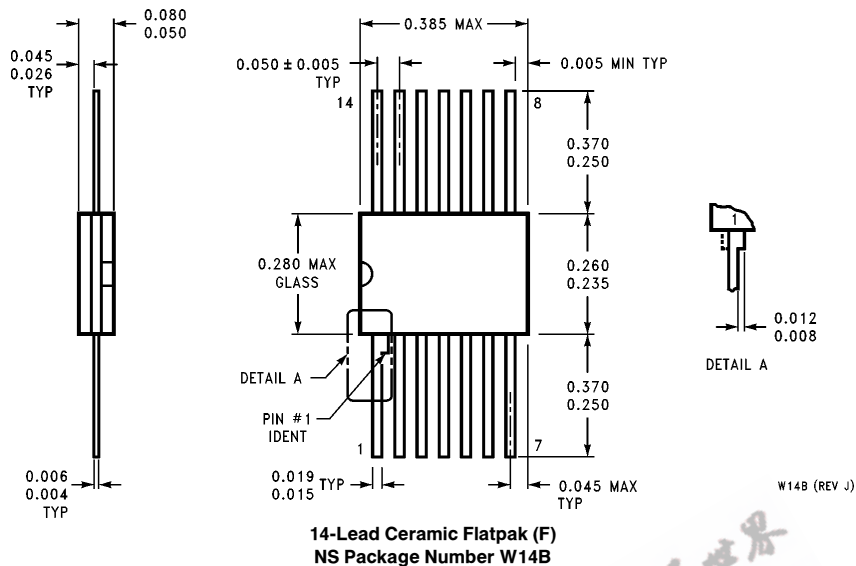
Physical Dimensions inches (millimeters) (Continued)



14-Lead Small Outline Integrated Circuit (S)
NS Package Number M14A



14-Lead Plastic Dual-In-Line Package (P)
NS Package Number N14A

Physical Dimensions inches (millimeters) (Continued)**LIFE SUPPORT POLICY**

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