

## 54F/74F573 Octal D-Type Latch with TRI-STATE® Outputs

### General Description

The 'F573 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ( $\overline{OE}$ ) inputs.

This device is functionally identical to the 'F373 but has different pinouts.

### Features

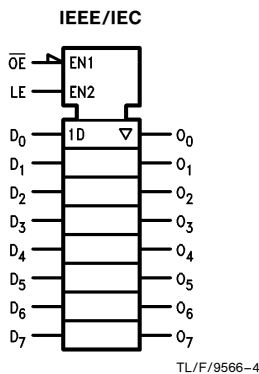
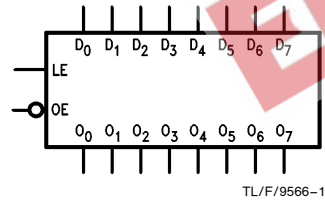
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'F373
- TRI-STATE outputs for bus interfacing
- Guaranteed 4000V minimum ESD protection

| Commercial        | Military          | Package Number | Package Description                               |
|-------------------|-------------------|----------------|---|
| 74F573PC          |                   | N20A           | 20-Lead (0.300" Wide) Molded Dual-In-Line         |
|                   | 54F573DM (Note 2) | J20A           | 20-Lead Ceramic Dual-In-Line                      |
| 74F573SC (Note 1) |                   | M20B           | 20-Lead (0.300" Wide) Molded Small Outline, JEDEC |
| 74F573SJ (Note 1) |                   | M20D           | 20-Lead (0.300" Wide) Molded Small Outline, EIAJ  |
|                   | 54F573FM (Note 2) | W20A           | 20-Lead Cerpak                                    |
|                   | 54F573LM (Note 2) | E20A           | 20-Lead Ceramic Leadless Chip Carrier, Type C     |

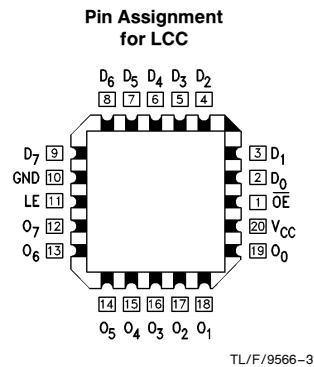
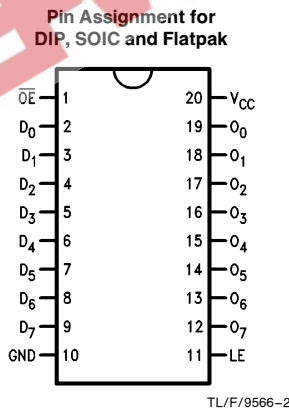
**Note 1:** Devices also available in 13" reel. Use suffix = SCX and SJX.

**Note 2:** Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

### Logic Symbols



### Connection Diagrams



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## Unit Loading/Fan Out

| Pin Names       | Description                                   | 54F/74F          |   |
|-----------------|---|------------------|---|
|                 |   | U.L.<br>HIGH/LOW | Input $I_{IH}/I_{IL}$<br>Output $I_{OH}/I_{OL}$ |
| $D_0$ – $D_7$   | Data Inputs                                   | 1.0/1.0          | $20\ \mu\text{A}/-0.6\ \text{mA}$               |
| LE              | Latch Enable Input (Active HIGH)              | 1.0/1.0          | $20\ \mu\text{A}/-0.6\ \text{mA}$               |
| $\overline{OE}$ | TRI-STATE Output Enable Input<br>(Active LOW) | 1.0/1.0          | $20\ \mu\text{A}/-0.6\ \text{mA}$               |
| $O_0$ – $O_7$   | TRI-STATE Latch Outputs                       | 150/40(33.3)     | $-3\ \text{mA}/24\ \text{mA}$ (20 mA)           |

## Functional Description

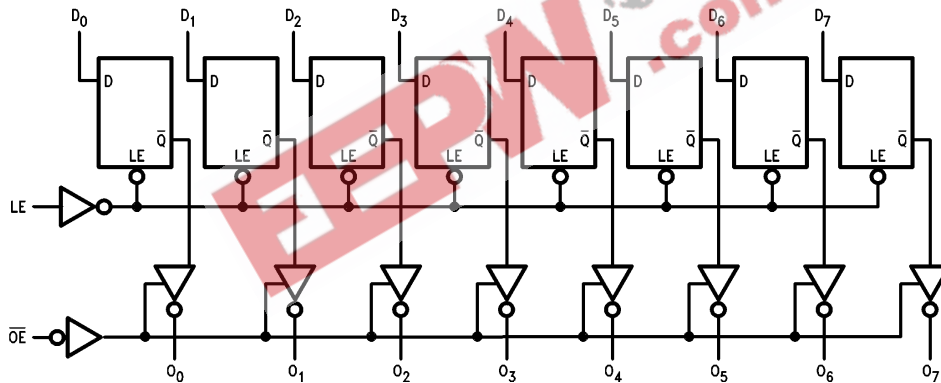
The 'F573 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable ( $\overline{OE}$ ) input. When  $\overline{OE}$  is LOW, the buffers are in the bi-state mode. When  $\overline{OE}$  is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Function Table

| Inputs          |    |   | Outputs |
|-----------------|----|---|---------|
| $\overline{OE}$ | LE | D | O       |
| L               | H  | H | H       |
| L               | H  | L | L       |
| L               | L  | X | $O_0$   |
| H               | X  | X | Z       |

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
 $O_0$  = Value stored from previous clock cycle

## Logic Diagram



TL/F/9566-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|   |                                      |
|---|--------------------------------------|
| Storage Temperature   | -65°C to +150°C                      |
| Ambient Temperature under Bias                                      | -55°C to +125°C                      |
| Junction Temperature under Bias                                     | -55°C to +175°C                      |
| Plastic   | -55°C to +150°C                      |
| V <sub>CC</sub> Pin Potential to Ground Pin                         | -0.5V to +7.0V                       |
| Input Voltage (Note 2)  | -0.5V to +7.0V                       |
| Input Current (Note 2)  | -30 mA to +5.0 mA                    |
| Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V) |                                      |
| Standard Output   | -0.5V to V <sub>CC</sub>             |
| TRI-STATE Output  | -0.5V to +5.5V                       |
| Current Applied to Output in LOW State (Max)                        | twice the rated I <sub>OL</sub> (mA) |
| ESD Last Passing Voltage (Min)                                      | 4000V                                |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

|                              |                 |
|------------------------------|-----------------|
| Free Air Ambient Temperature |                 |
| Military                     | -55°C to +125°C |
| Commercial                   | 0°C to +70°C    |
| Supply Voltage               |                 |
| Military                     | +4.5V to +5.5V  |
| Commercial                   | +4.5V to +5.5V  |

## DC Electrical Characteristics

| Symbol            | Parameter                         | 54F/74F  |  |             | Units | V <sub>CC</sub> | Conditions   |
|-------------------|-----------------------------------|--|--|-------------|-------|-----------------|--|
|                   |                                   | Min  | Typ                                    | Max         |       |                 |  |
| V <sub>IH</sub>   | Input HIGH Voltage                | 2.0  |  |             | V     |                 | Recognized as a HIGH Signal  |
| V <sub>IL</sub>   | Input LOW Voltage                 |  |  | 0.8         | V     |                 | Recognized as a LOW Signal   |
| V <sub>CD</sub>   | Input Clamp Diode Voltage         |  |  | -1.2        | V     | Min             | I <sub>IN</sub> = -18 mA   |
| V <sub>OH</sub>   | Output HIGH Voltage               | 54F 10% V <sub>CC</sub><br>54F 10% V <sub>CC</sub><br>74F 10% V <sub>CC</sub><br>74F 10% V <sub>CC</sub><br>74F 5% V <sub>CC</sub><br>74F 5% V <sub>CC</sub> | 2.5<br>2.4<br>2.5<br>2.4<br>2.7<br>2.7 |             | V     | Min             | I <sub>OH</sub> = -1 mA<br>I <sub>OH</sub> = -3 mA<br>I <sub>OH</sub> = -1 mA<br>I <sub>OH</sub> = -3 mA<br>I <sub>OH</sub> = -1 mA<br>I <sub>OH</sub> = -3 mA |
| V <sub>OL</sub>   | Output LOW Voltage                | 54F 10% V <sub>CC</sub><br>74F 10% V <sub>CC</sub>   |  | 0.5<br>0.5  | V     | Min             | I <sub>OL</sub> = 20 mA<br>I <sub>OL</sub> = 24 mA   |
| I <sub>IH</sub>   | Input HIGH Current                | 54F<br>74F   |  | 20.0<br>5.0 | μA    | Max             | V <sub>IN</sub> = 2.7V   |
| I <sub>BVI</sub>  | Input HIGH Current Breakdown Test | 54F<br>74F   |  | 100<br>7.0  | μA    | Max             | V <sub>IN</sub> = 7.0V   |
| I <sub>CEX</sub>  | Output HIGH Leakage Current       | 54F<br>74F   |  | 250<br>50   | μA    | Max             | V <sub>OUT</sub> = V <sub>CC</sub>   |
| V <sub>ID</sub>   | Input Leakage Test                | 74F  | 4.75                                   |             | V     | 0.0             | I <sub>ID</sub> = 1.9 μA<br>All Other Pins Grounded  |
| I <sub>OD</sub>   | Output Leakage Circuit Current    | 74F  |  | 3.75        | μA    | 0.0             | V <sub>IOD</sub> = 150 mV<br>All Other Pins Grounded   |
| I <sub>IL</sub>   | Input LOW Current                 |  |  | -0.6        | mA    | Max             | V <sub>IN</sub> = 0.5V   |
| I <sub>OZH</sub>  | Output Leakage Current            |  |  | 50          | μA    | Max             | V <sub>OUT</sub> = 2.7V  |
| I <sub>OZL</sub>  | Output Leakage Current            |  |  | -50         | μA    | Max             | V <sub>OUT</sub> = 0.5V  |
| I <sub>OS</sub>   | Output Short-Circuit Current      |  |  | -60         | mA    | Max             | V <sub>OUT</sub> = 0V  |
| I <sub>ZZ</sub>   | Bus Drainage Test                 |  |  | 500         | μA    | 0.0V            | V <sub>OUT</sub> = 5.25V   |
| I <sub>CCCL</sub> | Power Supply Current              |  | 35                                     | 55          | mA    | Max             | V <sub>O</sub> = LOW   |
| I <sub>CCZ</sub>  | Power Supply Current              |  | 35                                     | 55          | mA    | Max             | V <sub>O</sub> = HIGH Z  |

### AC Electrical Characteristics

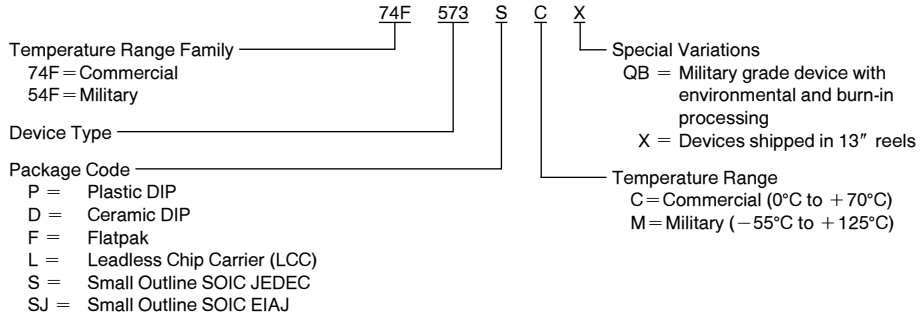
| Symbol                               | Parameter   | 74F   |            |             | 54F  |              | 74F  |             | Units |
|--------------------------------------|---|---|------------|-------------|--|--------------|--|-------------|-------|
|                                      |   | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50 pF |            |             | T <sub>A</sub> , V <sub>CC</sub> = Mil<br>C <sub>L</sub> = 50 pF |              | T <sub>A</sub> , V <sub>CC</sub> = Com<br>C <sub>L</sub> = 50 pF |             |       |
|                                      |   | Min   | Typ        | Max         | Min  | Max          | Min  | Max         |       |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>D <sub>n</sub> to O <sub>n</sub> | 3.0<br>2.0  | 5.3<br>3.7 | 7.0<br>6.0  | 3.0<br>2.0   | 9.0<br>7.0   | 3.0<br>2.0   | 8.0<br>6.5  | ns    |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>LE to O <sub>n</sub>             | 5.0<br>3.0  | 9.0<br>5.2 | 11.0<br>7.0 | 5.0<br>3.0   | 13.5<br>7.5  | 5.0<br>3.0   | 12.0<br>7.0 | ns    |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output Enable Time                                    | 2.0<br>2.0  | 5.0<br>5.6 | 8.0<br>8.5  | 2.0<br>2.0   | 10.0<br>10.0 | 2.0<br>2.0   | 9.0<br>9.5  | ns    |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Output Disable Time                                   | 1.5<br>1.5  | 4.5<br>3.8 | 5.5<br>5.5  | 1.5<br>1.5   | 7.0<br>5.5   | 1.5<br>1.5   | 6.5<br>5.5  | ns    |

### AC Operating Requirements

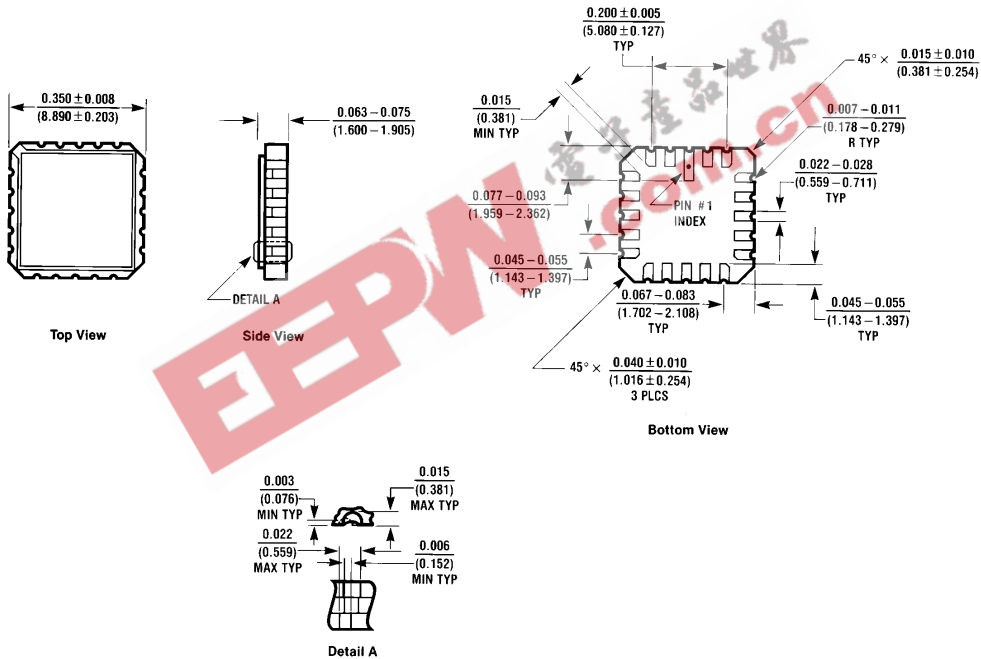
| Symbol                                   | Parameter                                       | 74F   |     | 54F                                    |     | 74F                                    |     | Units |
|--|---|---|-----|--|-----|--|-----|-------|
|  |   | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = +5.0V |     | T <sub>A</sub> , V <sub>CC</sub> = Mil |     | T <sub>A</sub> , V <sub>CC</sub> = Com |     |       |
|  |   | Min   | Max | Min                                    | Max | Min                                    | Max |       |
| t <sub>s</sub> (H)<br>t <sub>s</sub> (L) | Setup Time, HIGH or LOW<br>D <sub>n</sub> to LE | 2.0<br>2.0  |     | 2.0<br>2.0                             |     | 2.0<br>2.0                             |     | ns    |
| t <sub>h</sub> (H)<br>t <sub>h</sub> (L) | Hold Time, HIGH or LOW<br>D <sub>n</sub> to LE  | 3.0<br>3.5  |     | 3.0<br>4.0                             |     | 3.0<br>3.5                             |     | ns    |
| t <sub>w</sub> (H)                       | LE Pulse Width, HIGH                            | 4.0   |     | 4.0                                    |     | 4.0                                    |     | ns    |

## Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



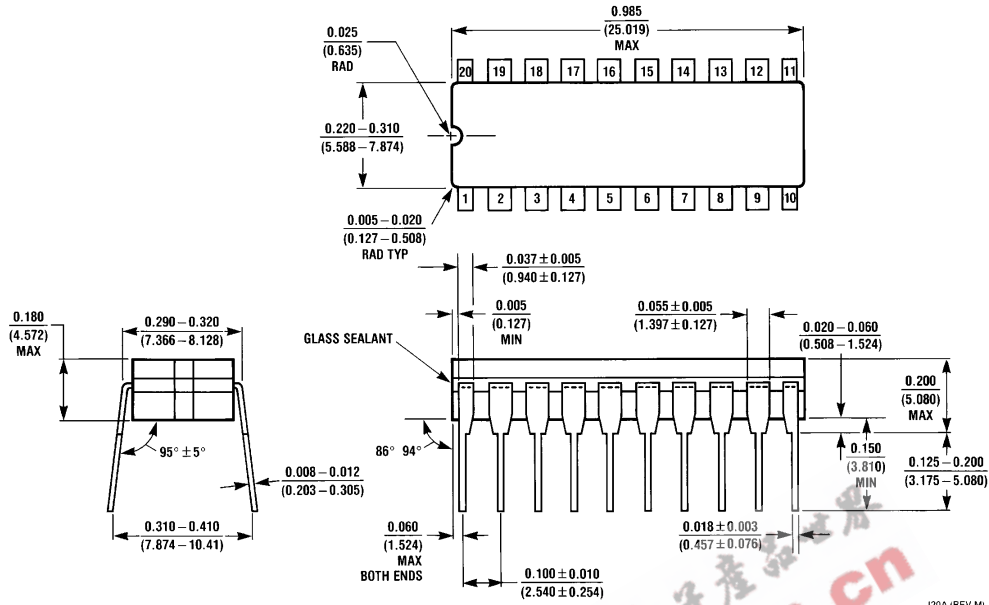
## Physical Dimensions inches (millimeters)



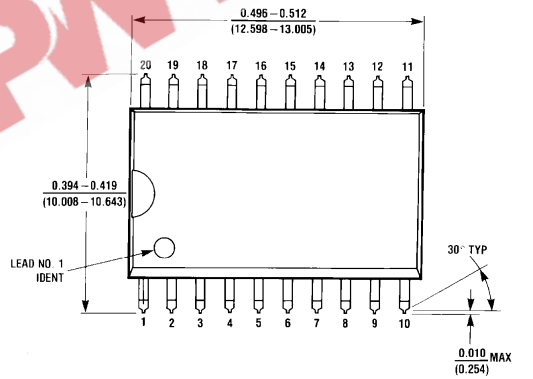
20-Lead Ceramic Leadless Chip Carrier (L)  
NS Package Number E20A

E20A (REV D)

**Physical Dimensions** inches (millimeters) (Continued)

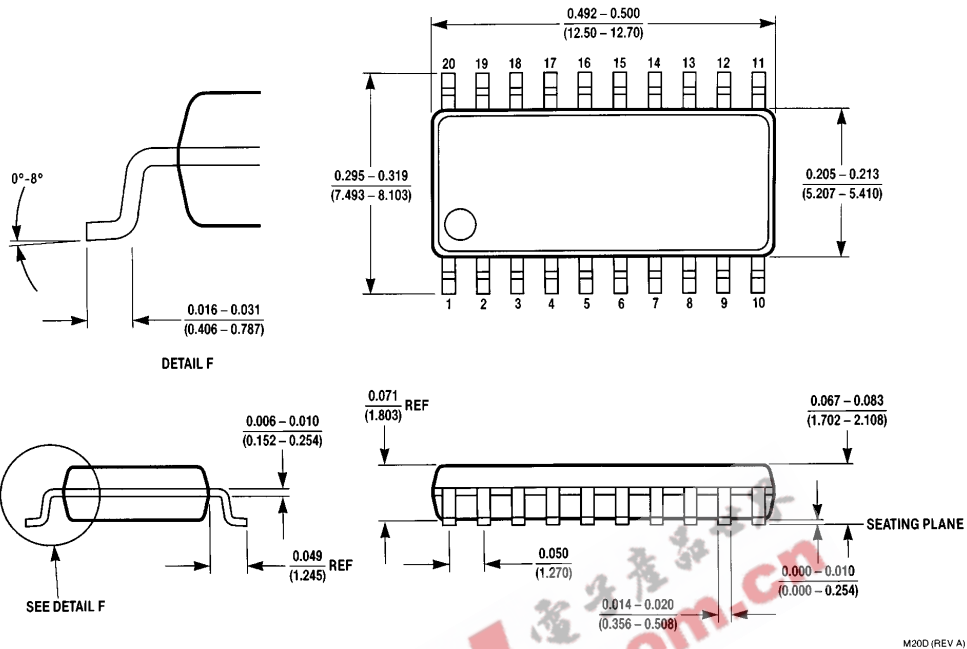


**20-Lead Ceramic Dual-In-Line Package (D)**  
NS Package Number J20A



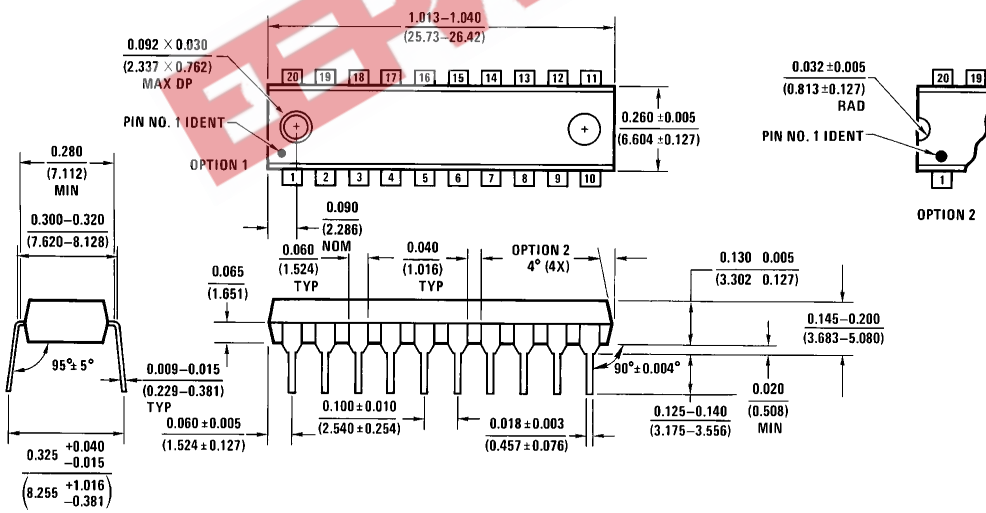
**20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)**  
NS Package Number M20B

**Physical Dimensions** inches (millimeters) (Continued)



M20D (REV A)

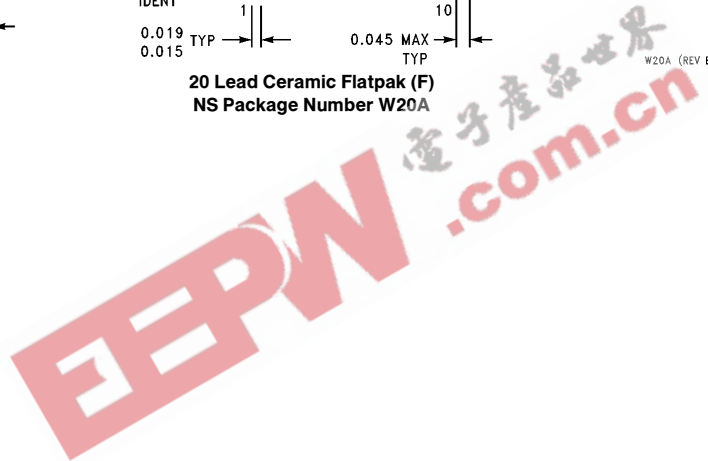
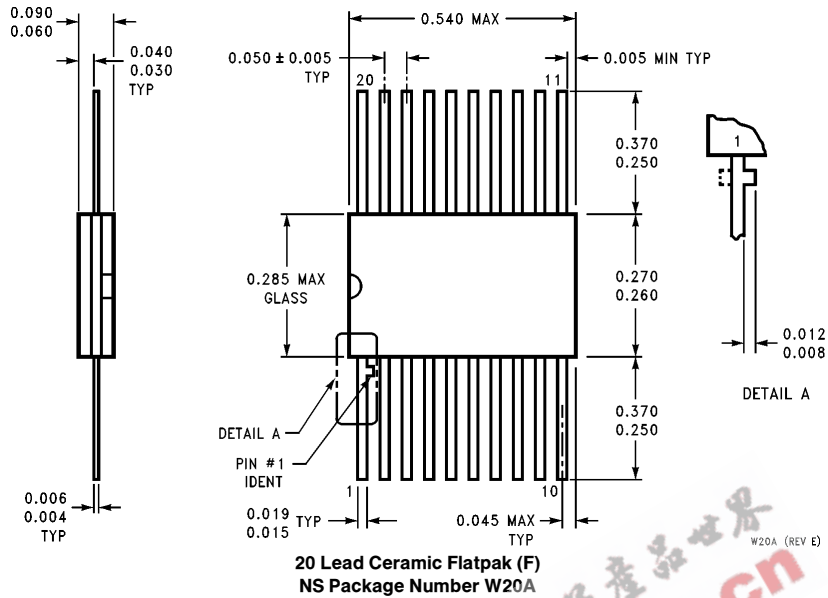
**20-Lead (0.300" Wide) Small Outline Package, EIAJ (SJ)**  
NS Package Number M20D



N20A (REV G)

**20-Lead (0.300" Wide) Molded Dual-In-Line Package (P)**  
NS Package Number N20A

**Physical Dimensions** inches (millimeters) (Continued)



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