

# DATA SHEET

**74ABT162240**

**74ABTH162240**

16-bit inverting buffer/driver with 30Ω  
series termination resistors

Product specification  
Supersedes data of 1998 Jan 16  
IC23 Data Handbook

1998 Feb 25

# 16-bit inverting buffer/driver with 30Ω series termination resistors (3-State)

## 74ABT162240 74ABTH162240

### FEATURES

- 16-bit bus interface
- 3-State buffers
- Output capability: +12mA/-32mA
- TTL input and output switching levels
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- 74ABTH162240 incorporates bus hold data inputs which eliminate the need for external pull up resistors to hold unused inputs
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

### DESCRIPTION

The 74ABT162240 is a high-performance BiCMOS device which combines low static and dynamic power dissipation with high speed.

This device is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables (1OE, 2OE, 3OE, 4OE), each controlling four of the 3-State outputs.

Two options are available, 74ABT162240 which does not have the bus hold feature and 74ABTH162240 which incorporates the bus hold feature.

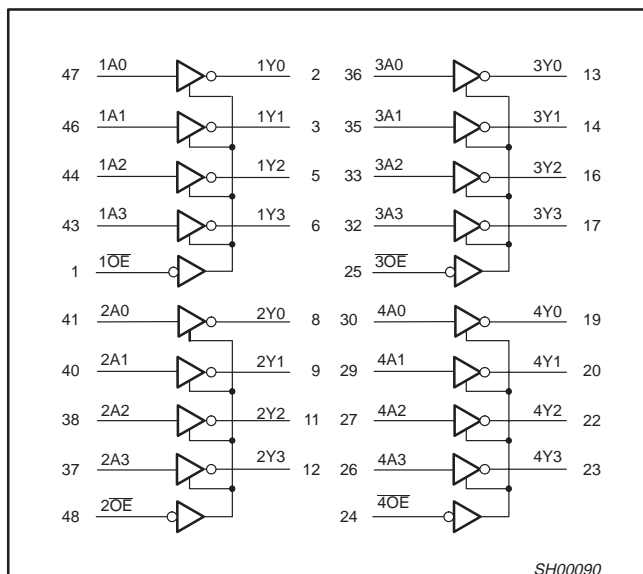
### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay nAx to nYx	$C_L = 50\text{pF}$ ; $V_{CC} =$	2.7 2.6	ns
$C_{IN}$	Input capacitance nOE	$V_I = 0\text{V}$ or $3.0\text{V}$	4	pF
$C_{OUT}$	Output capacitance	Outputs disabled; $V_O = 0\text{V}$ or	6	pF
$I_{CCZ}$	Quiescent supply current	Outputs disabled; $V_{CC} =$	500	$\mu\text{A}$
$I_{CCL}$		Outputs low; $V_{CC} = 5.5\text{V}$	8	mA

### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	-40°C to +85°C	74ABT162240 DL	BT162240 DL	SOT370-1
48-Pin Plastic TSSOP Type II	-40°C to +85°C	74ABT162240 DGG	BT162240 DGG	SOT362-1
48-Pin Plastic SSOP Type III	-40°C to +85°C	74ABTH162240 DL	BH162240 DL	SOT370-1
48-Pin Plastic TSSOP Type II	-40°C to +85°C	74ABTH162240 DGG	BH162240 DGG	SOT362-1

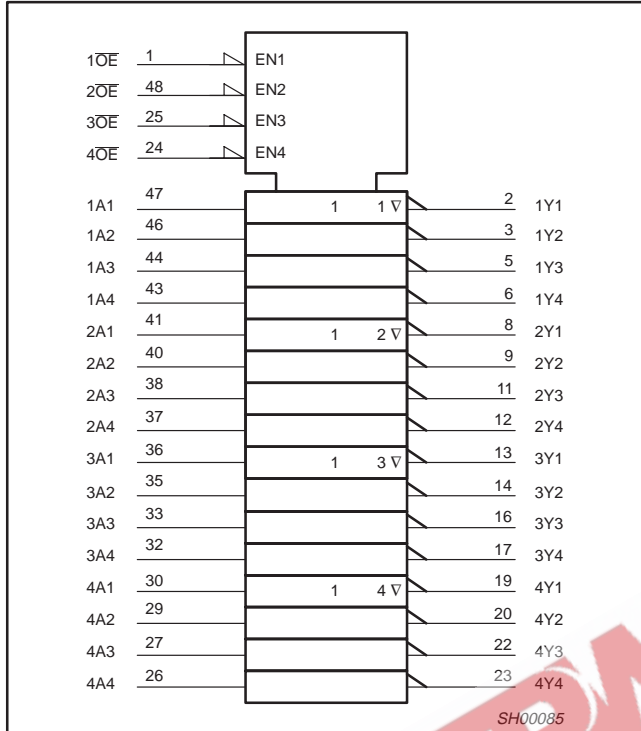
### LOGIC SYMBOL



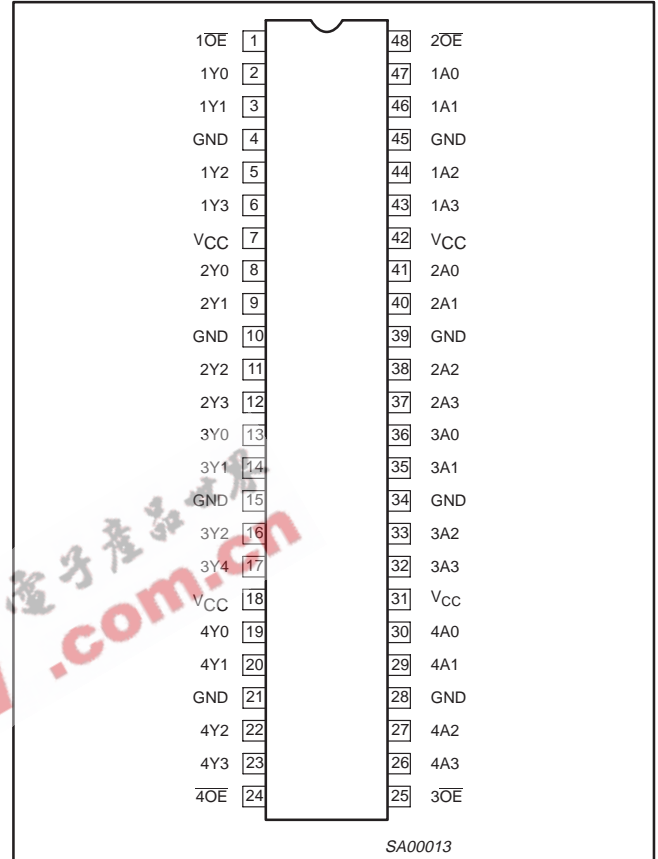
16-bit inverting buffer/driver with 30Ω series termination resistors (3-State)

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LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



FUNCTION TABLE

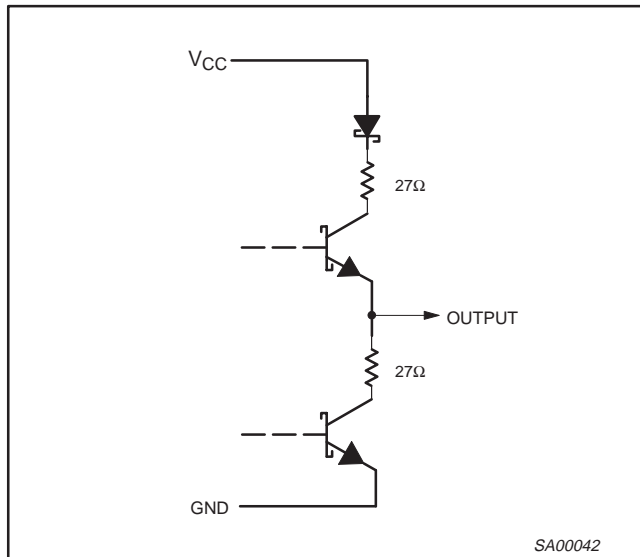
Inputs		Outputs
nOE	nAx	nYx
L	L	H
L	H	L
H	X	Z

H = High voltage level  
L = Low voltage level  
X = Don't care  
Z = High Impedance "off" state

# 16-bit inverting buffer/driver with 30Ω series termination resistors (3-State)

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## SCHEMATIC OF Y OUTPUTS



## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0-1A3 2A0-2A3 3A0-3A3 4A0-4A3	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Y0-1Y3 2Y0-2Y3 3Y0-3Y3 4Y0-4Y3	Data outputs
1, 48, 25, 24	1OE, 2OE, 3OE, 4OE	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V <sub>CC</sub>	Positive supply voltage

# 16-bit inverting buffer/driver with 30Ω series termination resistors (3-State)

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## ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +7.0	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	-18	mA
V <sub>I</sub>	DC input voltage <sup>3</sup>		-1.2 to +7.0	V
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> < 0	-50	mA
V <sub>OUT</sub>	DC output voltage <sup>3</sup>	Output in Off or High state	-0.5 to +5.5	V
I <sub>OUT</sub>	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T <sub>stg</sub>	Storage temperature range		-65 to +150	°C

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V <sub>CC</sub>	DC supply voltage	4.5	5.5	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>IH</sub>	High-level input voltage	2.0		V
V <sub>IL</sub>	Input voltage		0.8	V
I <sub>OH</sub>	High-level output current		-32	mA
I <sub>OL</sub>	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		12	
Δt/Δv	Input transition rise or fall rate; Outputs enabled	0	10	ns/V
T <sub>amb</sub>	Operating free-air temperature range	-40	+85	°C

# 16-bit inverting buffer/driver with 30Ω series termination resistors (3-State)

# 74ABT162240 74ABTH162240

## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 4.5V; I <sub>IK</sub> = -18mA		-0.9	-1.2		-1.2	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	2.5	2.9		2.5		V
		V <sub>CC</sub> = 5.0V; I <sub>OH</sub> = -3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	3.0	3.4		3.0		V
		V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -32mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	2.0	2.4		2.0		V
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = 4.5V; I <sub>OL</sub> = 8mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>			0.65		0.65	V
		V <sub>CC</sub> = 4.5V; I <sub>OL</sub> = 12mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>			0.80		0.80	V
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 5.5V; V <sub>I</sub> = GND or 5.5V		±0.01	±1.0		±1.0	μA
I <sub>I</sub>	Input leakage current 74ABTH162240	V <sub>CC</sub> = 5.5V; V <sub>I</sub> = V <sub>CC</sub> or GND		±0.01	±1		±1	μA
		V <sub>CC</sub> = 5.5V; V <sub>I</sub> = V <sub>CC</sub>		0.01	1		1	μA
		V <sub>CC</sub> = 5.5V; V <sub>I</sub> = 0		-2	-3		-5	μA
I <sub>HOLD</sub>	Bus Hold current A inputs <sup>3</sup> 74ABTH162240	V <sub>CC</sub> = 4.5V; V <sub>I</sub> = 0.8V	50			50		μA
		V <sub>CC</sub> = 4.5V; V <sub>I</sub> = 2.0V	-75			-75		
		V <sub>CC</sub> = 5.5V; V <sub>I</sub> = 0 to 5.5V	±500					
I <sub>OFF</sub>	Power-off leakage current	V <sub>CC</sub> = 0.0V; V <sub>O</sub> or V <sub>I</sub> ≤ 4.5V		±5.0	±100		±100	μA
I <sub>PU</sub> /I <sub>PD</sub>	Power-up/down 3-State output current	V <sub>CC</sub> = 2.0V; V <sub>O</sub> = 0.5V; V <sub>I</sub> = GND or V <sub>CC</sub> ; V <sub>OE</sub> = V <sub>CC</sub>		±5.0	±50		±50	μA
I <sub>OZH</sub>	3-State output High current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 2.7V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		1.0	10		10	μA
I <sub>OZL</sub>	3-State output Low current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 0.5V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		-1.0	-10		-10	μA
I <sub>CEx</sub>	Output high leakage current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 5.5V; V <sub>I</sub> = GND or V <sub>CC</sub>		1.0	50		50	μA
I <sub>O</sub>	Output current <sup>1</sup>	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 2.5V	-50	-70	-180	-50	-180	mA
I <sub>CCH</sub>	Quiescent supply current	V <sub>CC</sub> = 5.5V; Outputs High, V <sub>I</sub> = GND or V <sub>CC</sub>		0.5	1.0		1.0	mA
I <sub>CCL</sub>		V <sub>CC</sub> = 5.5V; Outputs Low, V <sub>I</sub> = GND or V <sub>CC</sub>		8	19		19	mA
I <sub>CCZ</sub>		V <sub>CC</sub> = 5.5V; Outputs 3-State; V <sub>I</sub> = GND or V <sub>CC</sub>		0.5	1.0		1.0	mA
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup> 74ABT162240	Outputs enabled, one input at 3.4V, other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5V		10	200		200	μA
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup> 74ABTH162240	Outputs enabled, one input at 3.4V, other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5V		0.2	1.0		1.0	mA

### NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

16-bit inverting buffer/driver with 30Ω series termination resistors (3-State)

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74ABTH162240

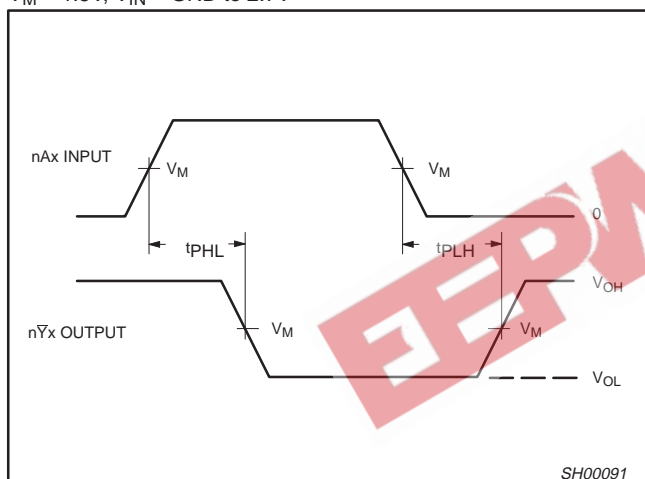
**AC CHARACTERISTICS**

GND = 0V;  $t_R = t_F = 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 500\Omega$ ;  $T_{\text{amb}} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

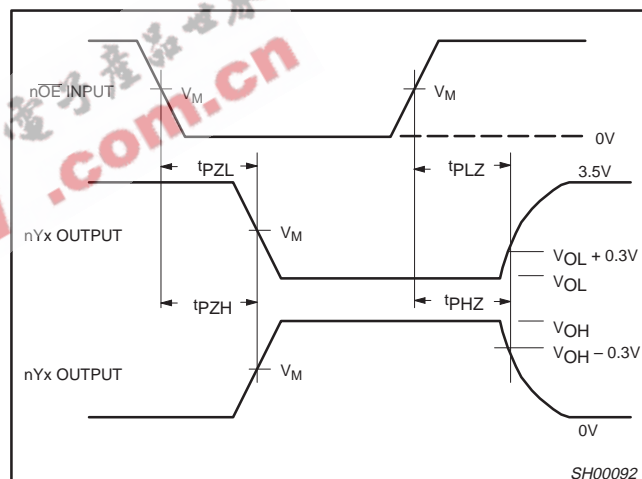
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$			$T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$		
			Min	Typ	Max	Min	Max	
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay nAx to nYx	1	1.0 1.0	2.7 2.6	3.8 3.2	1.0 1.0	4.2 3.7	ns
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output enable time to High and Low level	2	1.2 1.0	2.3 2.9	3.2 3.8	1.2 1.0	4.0 4.7	ns
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output disable time from High and Low level	2	1.6 1.4	3.0 2.8	4.1 3.8	1.6 1.4	4.7 4.0	ns

**AC WAVEFORMS**

$V_M = 1.5\text{V}$ ,  $V_{\text{IN}} = \text{GND}$  to  $2.7\text{V}$



Waveform 1. Input (nAx) to Output (nYx) Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

16-bit inverting buffer/driver with 30Ω series termination resistors (3-State)

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TEST CIRCUIT AND WAVEFORMS

**Test Circuit for 3-State Outputs**

The diagram shows a pulse generator connected to the input of a D.U.T. (Device Under Test) through a termination resistor  $R_T$ . The input voltage is  $V_{IN}$ . The output of the D.U.T. is  $V_{OUT}$ , which is connected to a load capacitor  $C_L$  and a load resistor  $R_L$ . A switch is connected to the output, which can be set to 7.0V or GND. The D.U.T. is powered by  $V_{CC}$ .

**Input Pulse Definition**

The waveforms show a negative pulse and a positive pulse. The pulse amplitude is  $V_M = 1.5V$ . The pulse width is  $t_W$ . The rise and fall times are  $t_{TLH} (t_R)$  and  $t_{THL} (t_F)$  respectively. The pulse levels are defined at 10% and 90% of the pulse amplitude.

**SWITCH POSITION**

TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	7V
All other	open

**DEFINITIONS**

$R_L$  = Load resistor; see AC CHARACTERISTICS for value.  
 $C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	$t_W$	$t_R$	$t_F$
74ABT16	3.0V	1MHz	500ns	2.5ns	2.5ns

SH00093

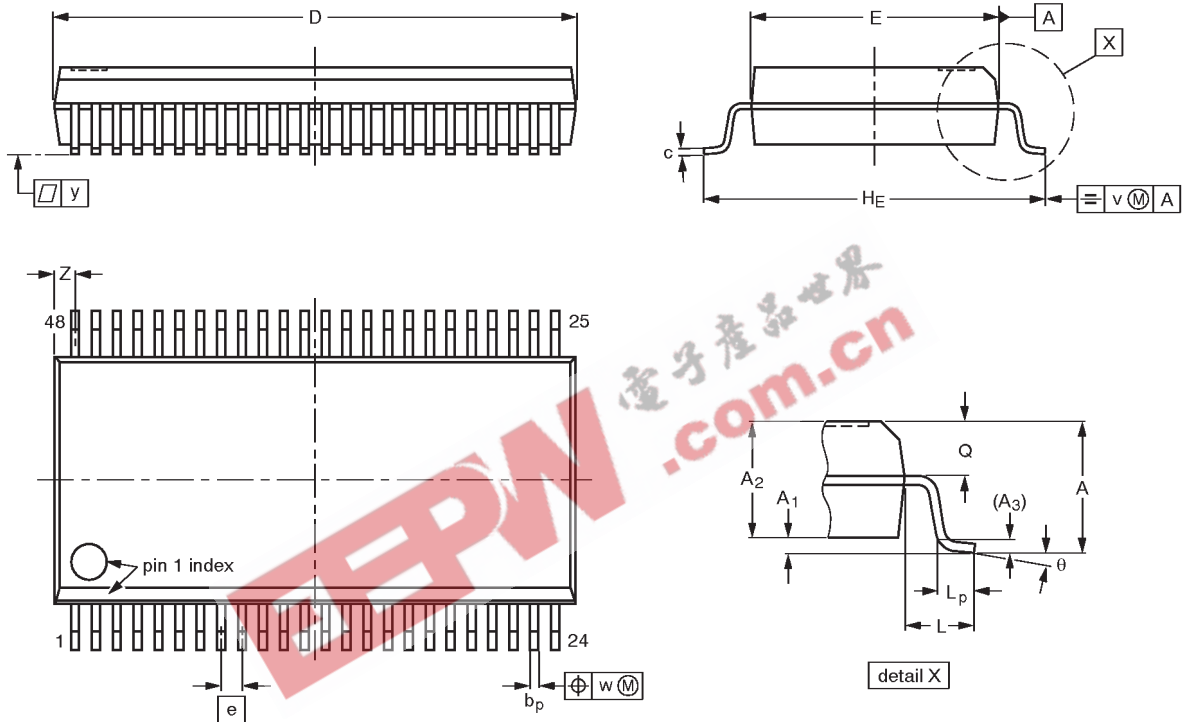


16-bit inverting buffer/driver with 30Ω Series Termination Resistors (3-State)

74ABT162240  
74ABTH162240

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

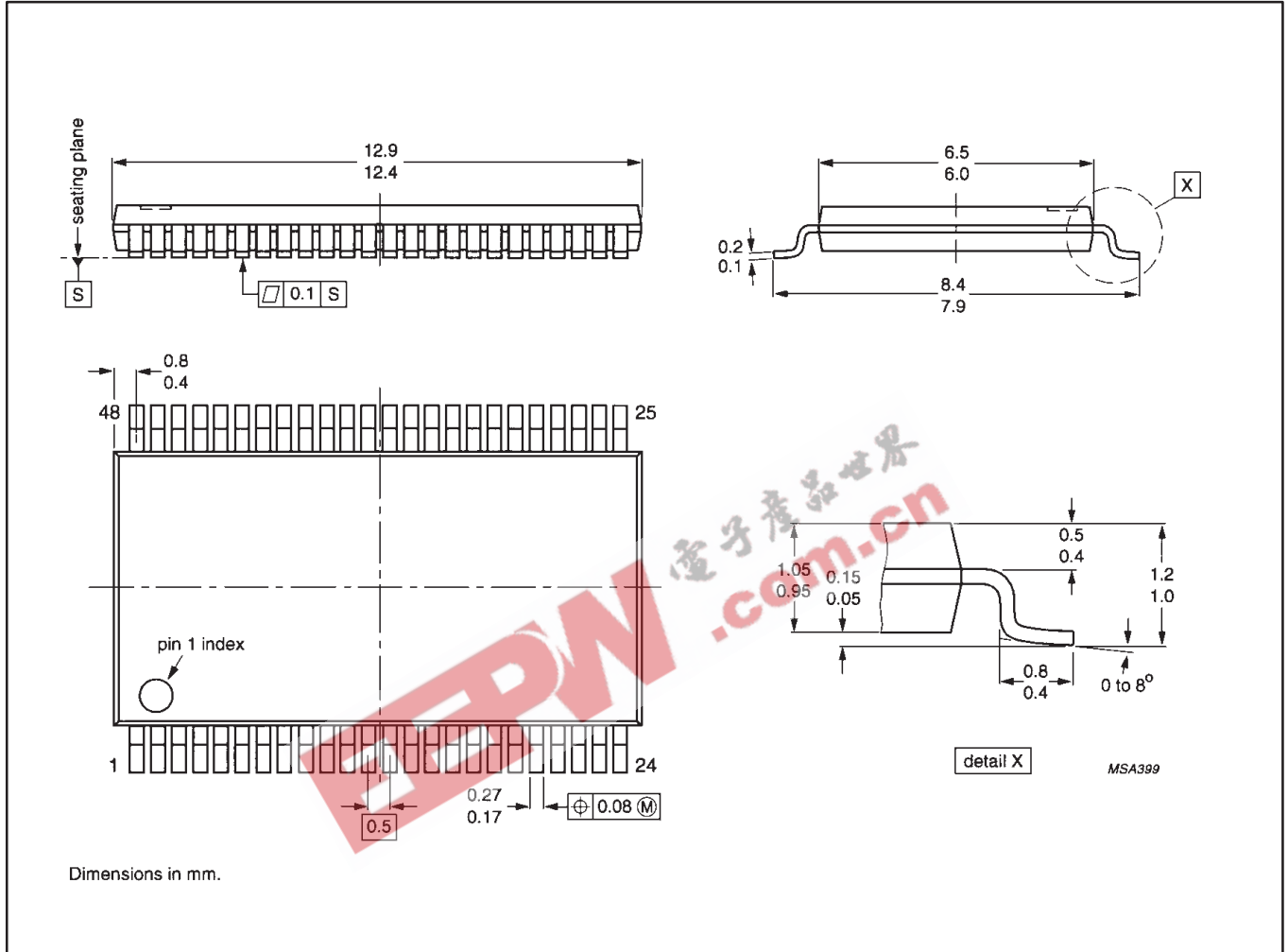
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				93-11-02 95-02-04

16-bit inverting buffer/driver with 30Ω Series Termination Resistors (3-State)

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74ABTH162240

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm

SOT362-1



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16-bit inverting buffer/driver with 30Ω Series  
Termination Resistors (3-State)

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74ABT162240  
74ABTH162240

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NOTES



# 16-bit inverting buffer/driver with 30 $\Omega$ series termination resistors (3-State)

74ABT162240  
74ABTH162240

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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