

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

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74HC/HCT166

8-bit parallel-in/serial-out shift register

Product specification
File under Integrated Circuits, IC06

December 1990

8-bit parallel-in/serial-out shift register

74HC/HCT166

FEATURES

- Synchronous parallel-to-serial applications
- Synchronous serial data input for easy expansion
- Clock enable for “do nothing” mode
- Asynchronous master reset
- For asynchronous parallel data load see “165”
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT166 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT166 are 8-bit shift registers which have a fully synchronous serial or parallel data entry selected by

an active LOW parallel enable (\overline{PE}) input. When \overline{PE} is LOW one set-up time prior to the LOW-to-HIGH clock transition, parallel data is entered into the register. When \overline{PE} is HIGH, data is entered into the internal bit position Q_0 from serial data input (D_s), and the remaining bits are shifted one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition.

This feature allows parallel-to-serial converter expansion by tying the Q_7 output to the D_s input of the succeeding stage.

The clock input is a gated-OR structure which allows one input to be used as an active LOW clock enable (\overline{CE}) input. The pin assignment for the CP and \overline{CE} inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of input \overline{CE} should only take place while CP is HIGH for predictable operation. A LOW on the master reset (\overline{MR}) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^\circ\text{C}$; $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_7 \overline{MR} to Q_7	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	15	20	ns
			14	19	ns
f_{max}	maximum clock frequency		63	50	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	41	41	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = \text{GND to } V_{CC}$
For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

ORDERING INFORMATION

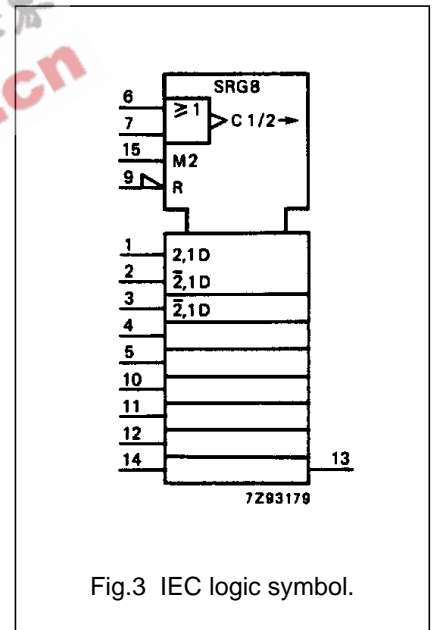
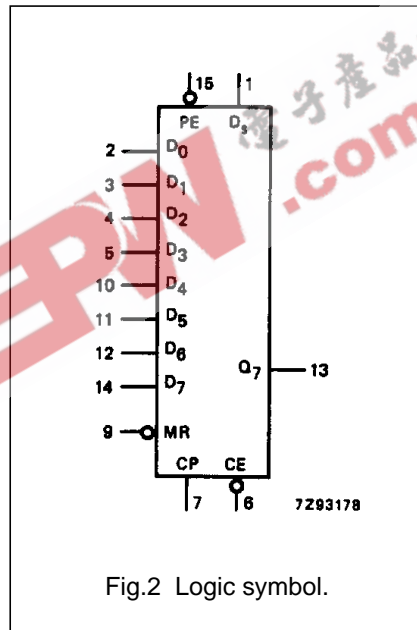
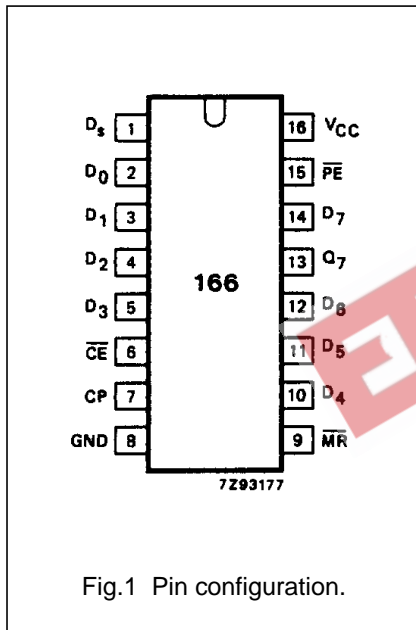
See “74HC/HCT/HCU/HCMOS Logic Package Information”.

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	D_s	serial data input
2, 3, 4, 5, 10, 11, 12, 14	D_0 to D_7	parallel data inputs
6	\overline{CE}	clock enable input (active LOW)
7	CP	clock input (LOW-to-HIGH edge-triggered)
8	GND	ground (0 V)
9	\overline{MR}	asynchronous master reset (active LOW)
13	Q_7	serial output from the last stage
15	\overline{PE}	parallel enable input (active LOW)
16	V_{CC}	positive supply voltage



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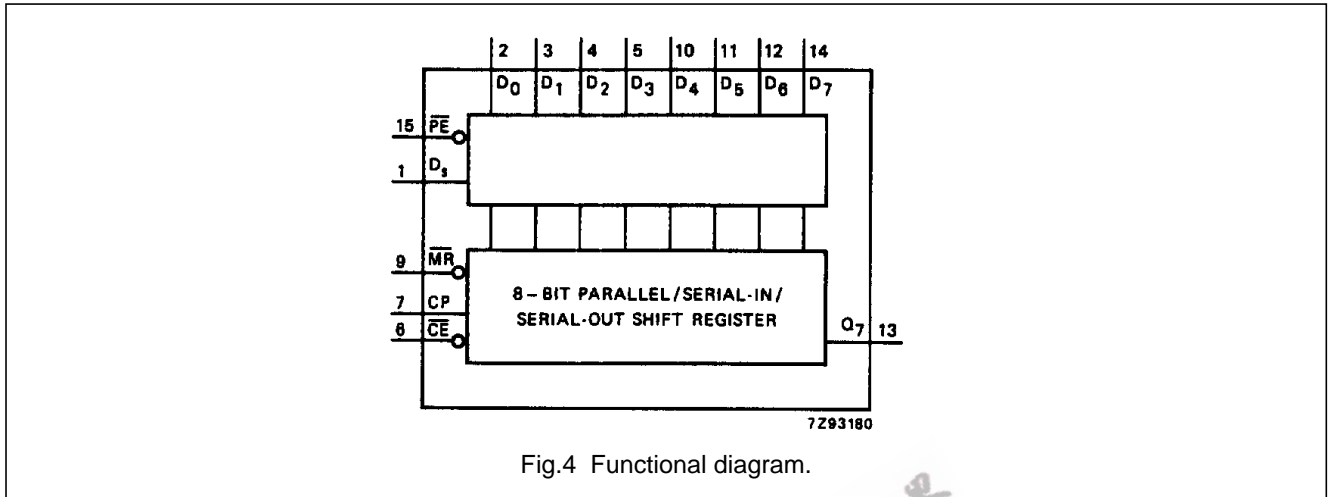


Fig.4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS					Q _n REGISTER		OUTPUT
	\overline{PE}	\overline{CE}	CP	D _s	D ₀ -D ₇	Q ₀	Q ₁ -Q ₆	Q ₇
parallel load	L	L	↑	X	L - L	L	L - L	L
	L	L	↑	X	h - h	H	H - H	H
serial shift	h	L	↑	L	X - X	L	q ₀ - q ₅	q ₆
	h	L	↑	h	X - X	H	q ₀ - q ₅	q ₆
hold "do nothing"	X	h	X	X	X - X	q ₀	q ₁ - q ₆	q ₇

Notes

- H = HIGH voltage level
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
 L = LOW voltage level
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
 q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
 X = don't care
 ↑ = LOW-to-HIGH CP transition

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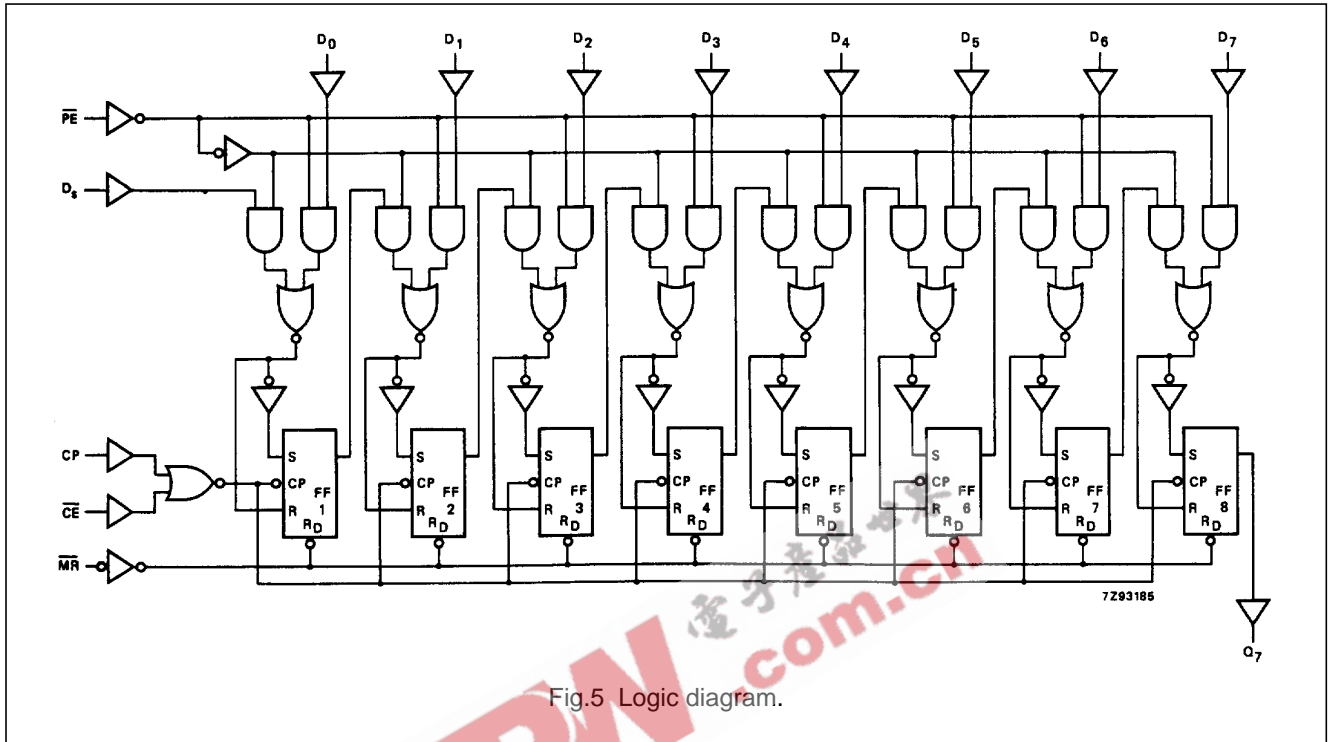


Fig.5 Logic diagram.

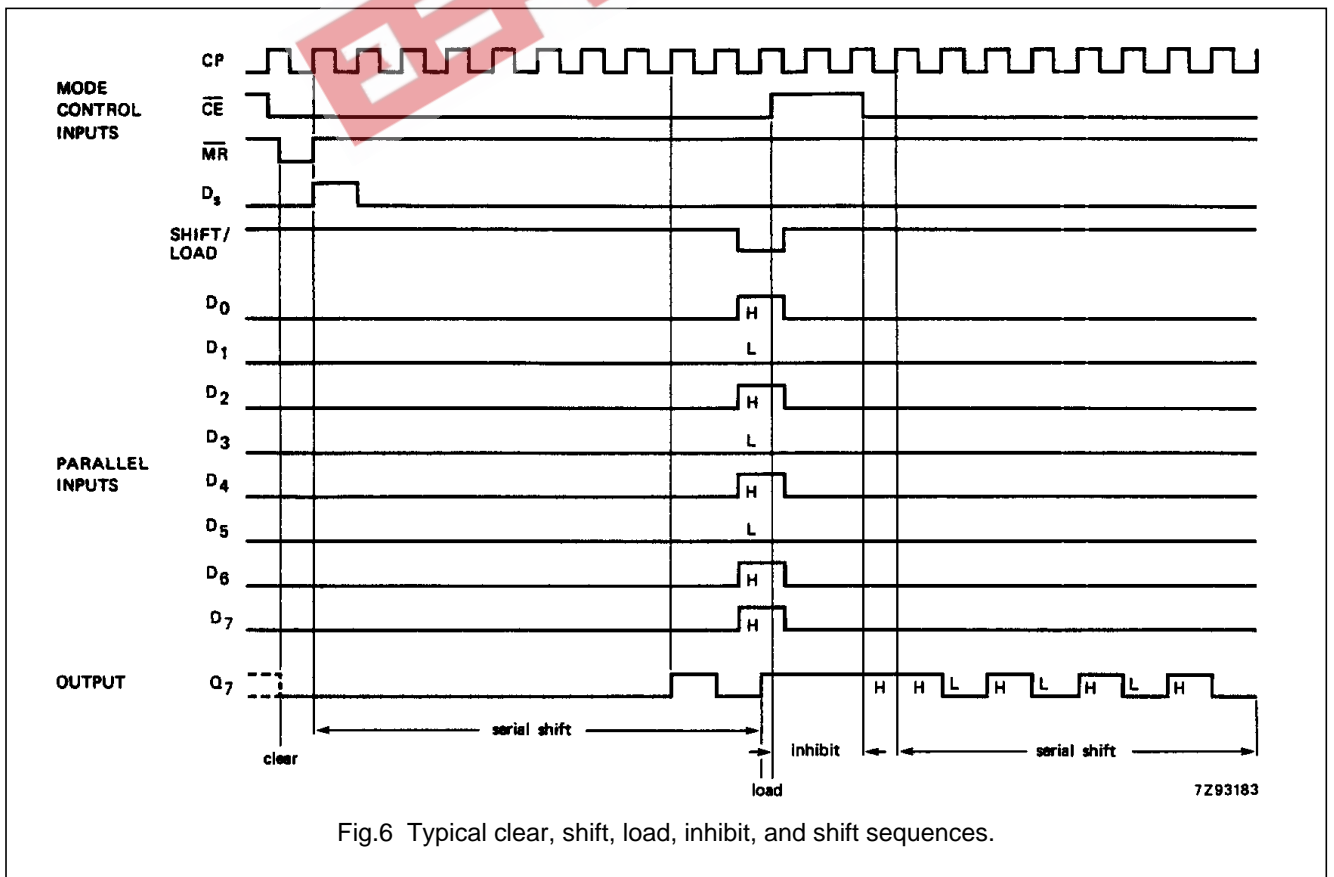


Fig.6 Typical clear, shift, load, inhibit, and shift sequences.

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay CP to Q ₇		50 18 14	150 30 26		190 38 33	225 45 38	ns	2.0 4.5 6.0	Fig.7	
t _{PHL}	propagation delay MR to Q ₇		47 17 14	160 32 27		200 40 34	240 48 41	ns	2.0 4.5 6.0	Fig.8	
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16	110 22 19	ns	2.0 4.5 6.0	Fig.7	
t _w	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig.7	
t _w	master reset pulse width LOW	100 20 17	25 9 7		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig.8	
t _{rem}	removal time MR to CP	0 0 0	-19 -7 -6		0 0 0		0 0 0	ns	2.0 4.5 6.0	Fig.8	
t _{su}	set-up time D _n , CE to CP	80 16 14	14 5 4		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig.9	
t _{su}	set-up time PE to CP	100 20 17	33 12 10		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig.8	
t _h	hold time D _n , CE to CP	2 2 2	-8 -3 -2		2 2 2		2 2 2	ns	2.0 4.5 6.0	Fig.8	
t _h	hold time PE to CP	0 0 0	-28 -10 -8		0 0 0		0 0 0	ns	2.0 4.5 6.0	Fig.9	
f _{max}	maximum clock pulse frequency	6.0 30 35	19 57 68		4.8 24 28		4.0 20 24	MHz	2.0 4.5 6.0	Fig.7	

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "*74HC/HCT/HCU/HCMOS Logic Family Specifications*".

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D ₀ to D ₇	0.35
D _s	0.35
CP	0.80
\overline{CE}	0.80
\overline{MR}	0.40
\overline{PE}	0.60

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AC CHARACTERISTICS FOR 74HCT

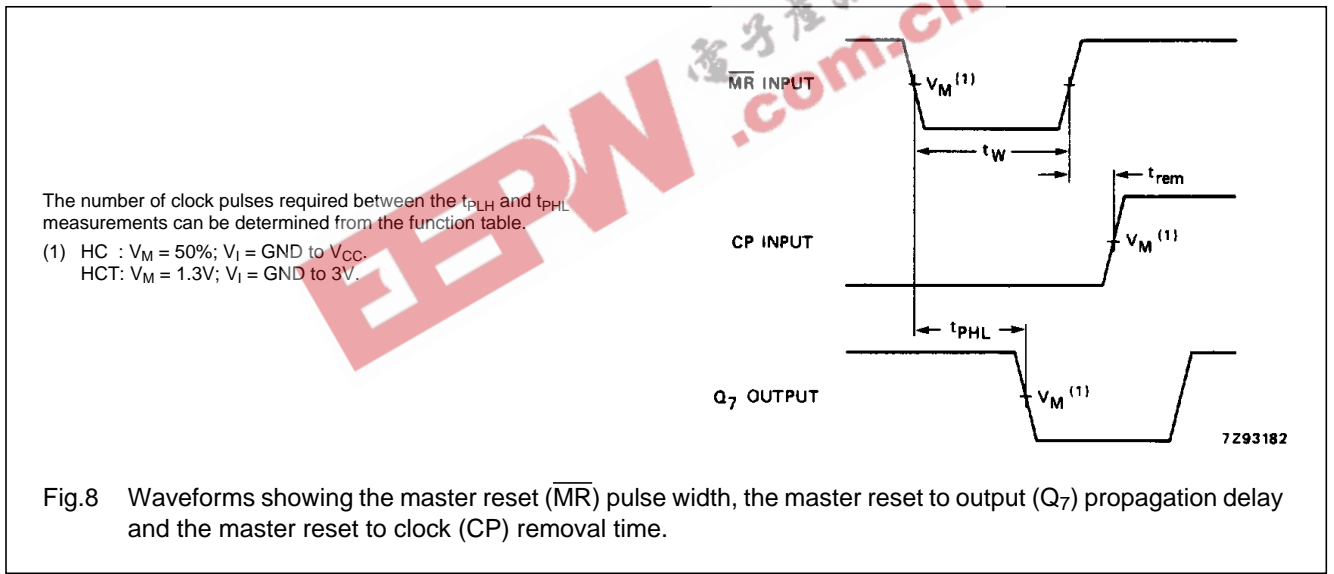
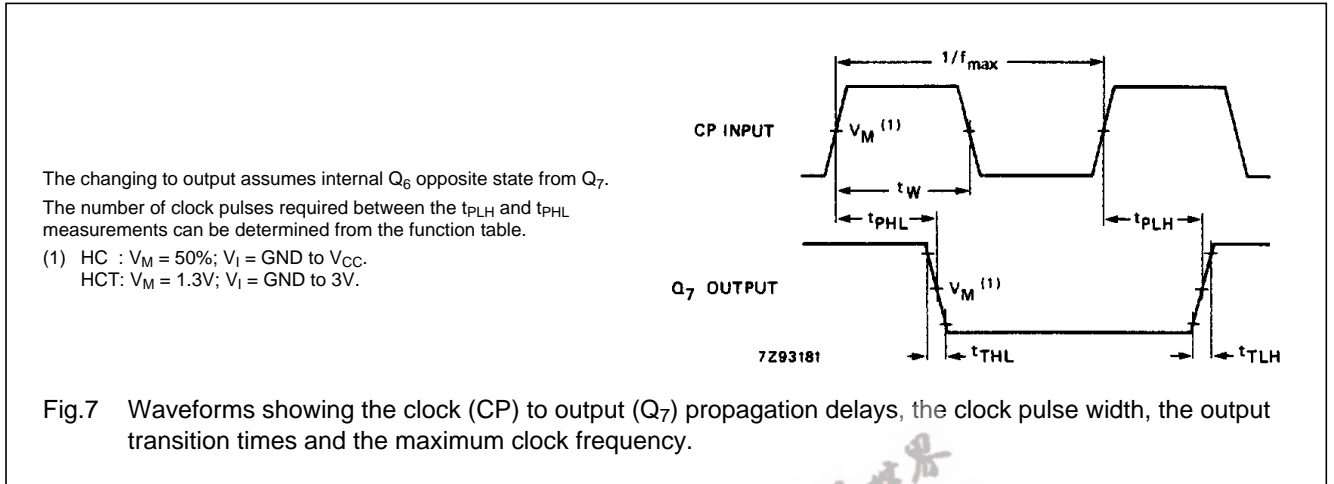
GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HCT							V _{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay CP to Q ₇		23	40		50		60	ns	4.5	Fig.7
t _{PHL}	propagation delay MR to Q ₇		22	40		50		60	ns	4.5	Fig.8
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.7
t _W	clock pulse width HIGH or LOW	20	9		25		30		ns	4.5	Fig.7
t _W	master reset pulse width LOW	25	11		31		38		ns	4.5	Fig.8
t _{rem}	removal time MR to CP	0	-7		0		0		ns	4.5	Fig.8
t _{su}	set-up time D _n , \overline{CE} to CP	16	8		20		24		ns	4.5	Fig.9
t _{su}	set-up time \overline{PE} to CP	30	15		38		45		ns	4.5	Fig.8
t _h	hold time D _n , \overline{CE} to CP	0	-3		0		0		ns	4.5	Fig.9
t _h	hold time \overline{PE} to CP	0	-13		0		0		ns	4.5	Fig.9
f _{max}	maximum clock pulse width	25	45		20		17		MHz	4.5	Fig.7

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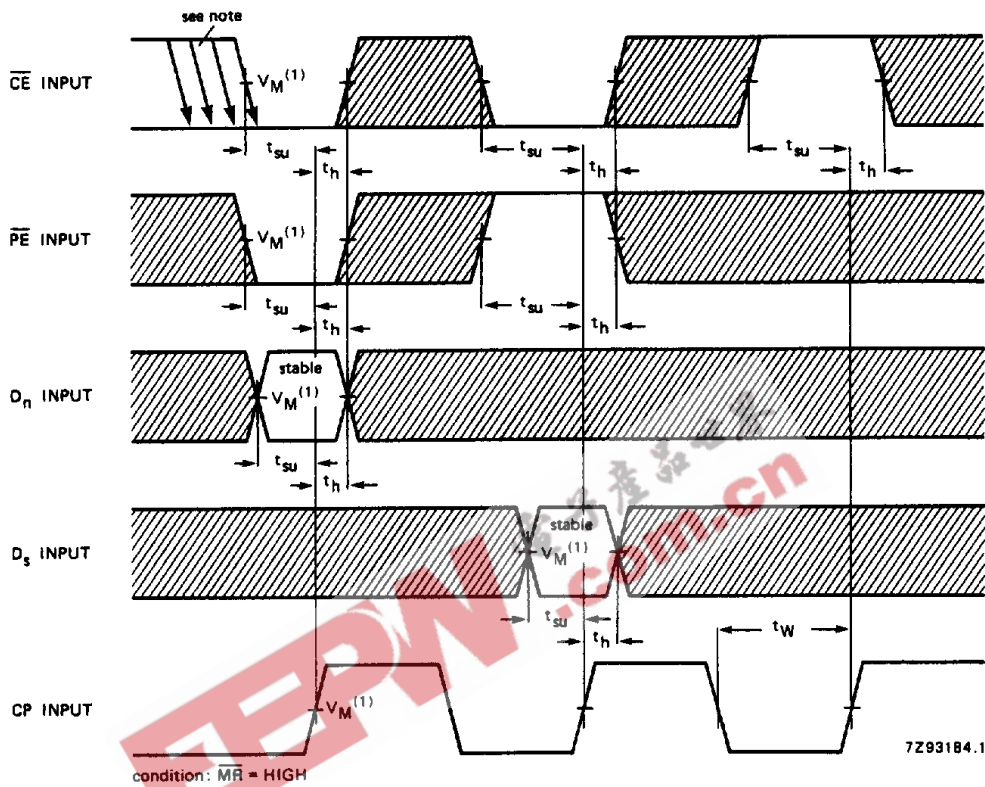
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AC WAVEFORMS



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The number of clock pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the function table.

\overline{CE} may change only from HIGH-to-LOW while CP is LOW.

The shaded areas indicate when the input is permitted to change for predictable output performance.

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
- HCT: $V_M = 1.3V$; $V_I = \text{GND to } 3V$.

Fig.9 Waveforms showing the set-up and hold times from the serial data input (D_s), the data inputs (D_n), the clock enable input (LOW \overline{CE}), the clock enable input CE and the parallel enable input to the clock (CP).

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".