

## 74VHC541 Octal Buffer/Line Driver with TRI-STATE® Outputs

### General Description

The VHC541 is an advanced high-speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The VHC541 is an octal buffer/line driver designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers.

This device is similar in function to the VHC244 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes this device especially useful as an output port for microprocessors, allowing ease of layout and greater PC board density.

An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

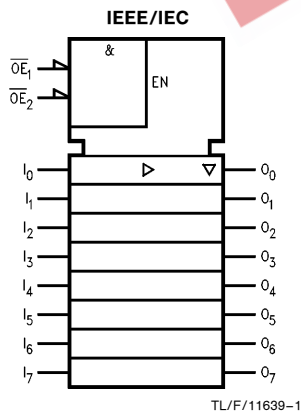
### Features

- Low power dissipation:  
 $I_{CC} = 4 \mu A$  (max) at  $T_A = 25^\circ C$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (min)
- All inputs are equipped with a power down protection function
- Balanced propagation delays:  $t_{PLH} \cong t_{PHL}$
- Low noise:  $V_{OLP} = 0.9V$  (typ)
- Pin and function compatible with 74HC541

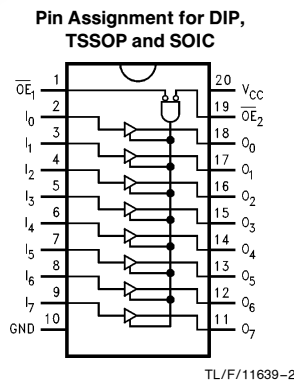
Commercial	Package Number	Package Description
74VHC541M	M20B	20-Lead Molded JEDEC SOIC
74VHC541SJ	M20D	20-Lead Molded EIAJ SOIC
74VHC541MTC	MTC20	20-Lead Molded JEDEC Type 1 TSSOP
74VHC541N	N20A	20-Lead Molded DIP

Note: Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbol



### Connection Diagram



### Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

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### Absolute Maximum Ratings (Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_{IN}$ )	-0.5V to +7.0V
DC Output Voltage ( $V_{OUT}$ )	-0.5V to $V_{CC} + 0.5V$
Input Diode Current ( $I_{IK}$ )	-20 mA
Output Diode Current ( $I_{OK}$ )	±20 mA
DC Output Current ( $I_{OUT}$ )	±25 mA
DC $V_{CC}$ /GND Current ( $I_{CC}$ )	±75 mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Lead Temperature ( $T_L$ ) (Soldering, 10 seconds)	260°C

Note 1: *Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside databook specifications.*

### Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	2.0V to +5.5V
Input Voltage ( $V_{IN}$ )	0V to +5.5V
Output Voltage ( $V_{OUT}$ )	0V to $V_{CC}$
Operating Temperature ( $T_{OPR}$ )	-40°C to +85°C
Input Rise and Fall Time ( $t_r, t_f$ )	0 ~ 100 ns/V
	$V_{CC} = 3.3V \pm 0.3V$
	0 ~ 20 ns/V
	$V_{CC} = 5.0V \pm 0.5V$

### DC Characteristics for 'VHC Family Devices

Symbol	Parameter	$V_{CC}$ (V)	74VHC				Units	Conditions	
			$T_A = 25^\circ C$			$T_A = -40^\circ C$ to $+85^\circ C$			
			Min	Typ	Max	Min			Max
$V_{IH}$	High Level Input Voltage	2.0 3.0-5.5	1.50 $0.7 V_{CC}$			1.50 $0.7 V_{CC}$	V		
$V_{IL}$	Low Level Input Voltage	2.0 3.0-5.5		0.50 $0.3 V_{CC}$		0.50 $0.3 V_{CC}$	V		
$V_{OH}$	High Level Output Voltage	2.0	1.9	2.0		1.9	V	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu A$
		3.0	2.9	3.0		2.9			
		4.5	4.4	4.5		4.4	V		$I_{OH} = -4 mA$ $I_{OH} = -8 mA$
		3.0	2.58			2.48			
		4.5	3.94			3.80	V		
$V_{OL}$	Low Level Output Voltage	2.0		0.0	0.1		V	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50 \mu A$
		3.0		0.0	0.1				
		4.5		0.0	0.1		V		$I_{OL} = 4 mA$ $I_{OL} = 8 mA$
		3.0			0.36				
		4.5			0.36				0.44
$I_{OZ}$	TRI-STATE Output Off-State Current	5.5		±0.25		±2.5	$\mu A$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND	
$I_{IN}$	Input Leakage Current	0-5.5		±0.1		±1.0	$\mu A$	$V_{IN} = 5.5V$ or GND	
$I_{CC}$	Quiescent Supply Current	5.5		4.0		40.0	$\mu A$	$V_{IN} = V_{CC}$ or GND	

### DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V <sub>CC</sub> (V)	74VHC		Units	Conditions
			T <sub>A</sub> = 25°C			
			Typ	Limits		
V <sub>OLP</sub> **	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0	0.9	1.2	V	C <sub>L</sub> = 50 pF
V <sub>OLV</sub> **	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0	-0.8	-1.0	V	C <sub>L</sub> = 50 pF
V <sub>IHD</sub> **	Minimum High Level Dynamic Input Voltage	5.0		3.5	V	C <sub>L</sub> = 50 pF
V <sub>ILD</sub> **	Maximum High Level Dynamic Input Voltage	5.0		1.5	V	C <sub>L</sub> = 50 pF

\*\*Parameter guaranteed by design.


  
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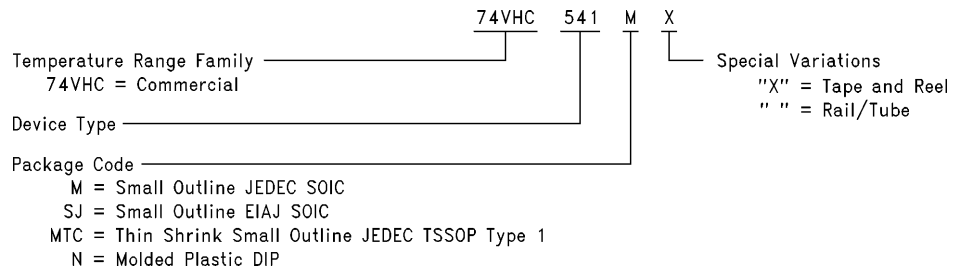
### AC Electrical Characteristics for 'VHC Family Devices:

Symbol	Parameter	V <sub>CC</sub> (V)	74VHC		74VHC		Units	Conditions		
			T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C				
			Min	Typ	Max	Min				Max
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time	3.3 ± 0.3	5.0	7.0	1.0	8.5	ns	C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF		
			7.5	10.5	1.0	12.0				
		5.0 ± 0.5	3.5	5.0	1.0	6.0	ns			
			5.0	7.0	1.0	8.0				
t <sub>PZL</sub> , t <sub>PZH</sub>	TRI-STATE Output Enable Time	3.3 ± 0.3	6.8	10.5	1.0	12.5	ns	R <sub>L</sub> = 1 kΩ C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF		
			9.3	14.0	1.0	16.0				
		5.0 ± 0.5	4.7	7.2	1.0	8.5	ns			
			6.2	9.2	1.0	10.5				
t <sub>PLZ</sub> , t <sub>PHZ</sub>	TRI-STATE Output Disable Time	3.3 ± 0.3	11.2	15.4	1.0	17.5	ns	R <sub>L</sub> = 1 kΩ C <sub>L</sub> = 50 pF C <sub>L</sub> = 50 pF		
		5.0 ± 0.5	6.0	8.8	1.0	10.0				
t <sub>OSLH</sub> , t <sub>OSSL</sub>	Output to Output Skew	3.3 ± 0.3		1.5		1.5	ns	(Note 1) C <sub>L</sub> = 50 pF C <sub>L</sub> = 50 pF		
		5.0 ± 0.5		1.0		1.0				
C <sub>IN</sub>	Input Capacitance		4	10		10	pF	V <sub>CC</sub> = Open		
C <sub>OUT</sub>	Output Capacitance		6				pF	V <sub>CC</sub> = 5.0V		
C <sub>PD</sub>	Power Dissipation Capacitance		18				pF	(Note 2)		

**Note 1:** Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHmax</sub> - t<sub>PLHmin</sub>|; t<sub>OSSL</sub> = |t<sub>PHLmax</sub> - t<sub>PHLmin</sub>|.

**Note 2:** C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC</sub> (OPR.) = C<sub>PD</sub> \* V<sub>CC</sub> \* f<sub>IN</sub> + I<sub>CC</sub>/8 (per bit).

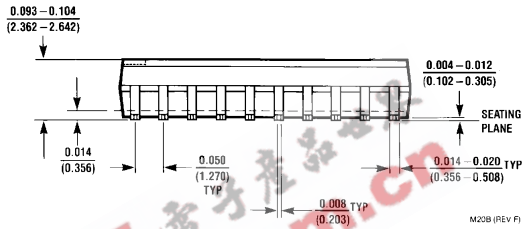
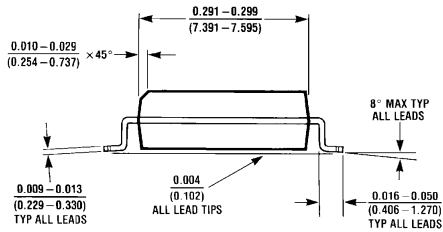
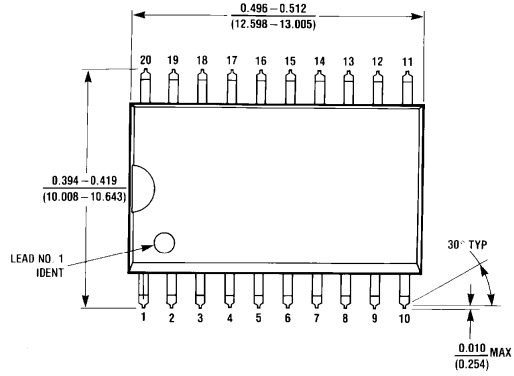
## Ordering Information



TL/F/11639-3

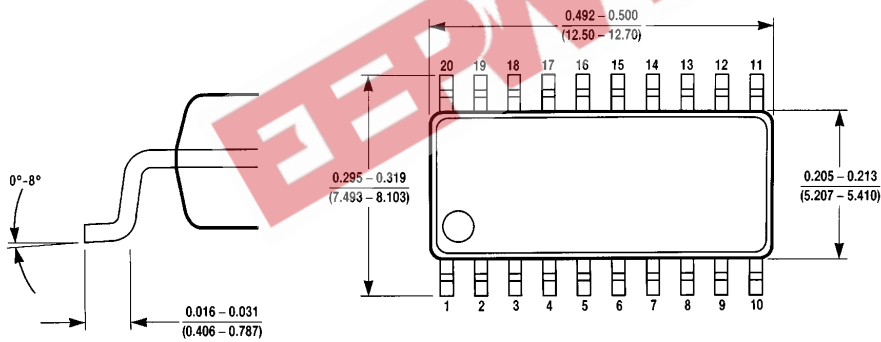
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**Physical Dimensions** inches (millimeters)

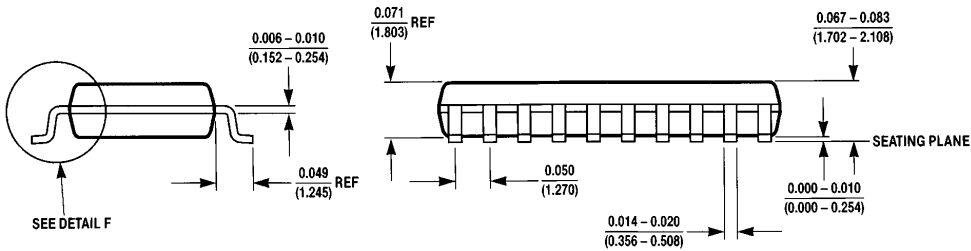


**20-Lead Small Outline Integrated Circuit—JEDEC SOIC (M)**  
NS Package Number M20B

M20B (REV F)



DETAIL F

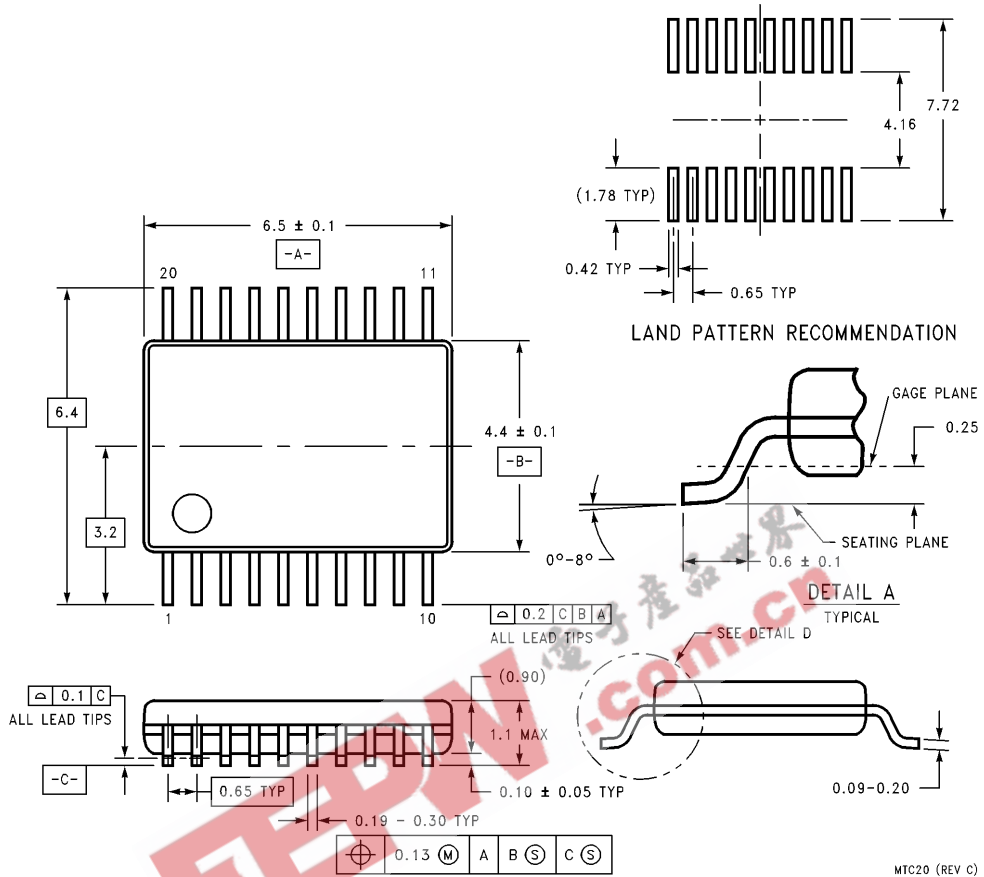


SEE DETAIL F

**20-Lead Plastic EIAJ SOIC (SJ)**  
NS Package Number M20D

M20D (REV A)

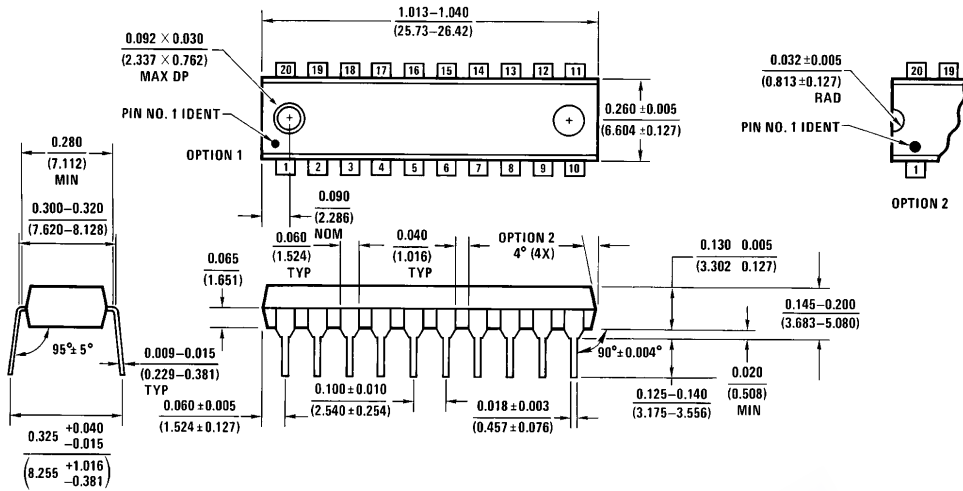
**Physical Dimensions** inches (millimeters) (Continued)



**20-Lead Molded Thin Shrink Small Outline JEDEC Type 1 TSSOP**  
**Order Number 74VHC541MTC**  
**NS Package Number MTC20**

MTC20 (REV C)

**Physical Dimensions** millimeters (Continued)



20-Lead (0.300" Wide) Molded Dual-In-Line Package  
 Order Number 74VHC541N  
 NS Package Number N20A



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**National Semiconductor Corporation**  
 1111 West Bardin Road  
 Arlington, TX 76017  
 Tel: 1(800) 272-9959  
 Fax: 1(800) 737-7018

**National Semiconductor Europe**  
 Fax: (+49) 0-180-530 85 86  
 Email: cnjwge@levm2.nsc.com  
 Deutsch Tel: (+49) 0-180-530 85 85  
 English Tel: (+49) 0-180-532 78 32  
 Français Tel: (+49) 0-180-532 93 58  
 Italiano Tel: (+49) 0-180-534 16 80

**National Semiconductor Hong Kong Ltd.**  
 13th Floor, Straight Block,  
 Ocean Centre, 5 Canton Rd.  
 Tsimshatsui, Kowloon  
 Hong Kong  
 Tel: (852) 2737-1600  
 Fax: (852) 2736-9960

**National Semiconductor Japan Ltd.**  
 Tel: 81-043-299-2309  
 Fax: 81-043-299-2408

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