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74ACT1284
IEEE 1284 Transceiver

General Description

The 74ACT1284 contains four non-inverting bidirectional buffers and three non-inverting buffers with open Drain outputs and high drive capability on the B Ports. It is intended to provide a standard signaling method for a bi-direction parallel peripheral in an Extended Capabilities Port mode (ECP).

The HD (active HIGH) input pin enables the B Ports to switch from open Drain to a high drive totem pole output, capable of sourcing 14 mA on all seven buffers. The DIR input determines the direction of data flow on the bidirectional buffers. DIR (active HIGH) enables data flow from A Ports to B Ports. DIR (active LOW) enables data flow from B Ports to A Ports.

Features

■ TTL-compatible inputs
■ A Ports have standard 4 mA totem pole outputs
■ Typical input hysteresis of 0.5V
■ B Port high drive source/sink capability of 14 mA
■ Bidirectional non-inverting buffers
■ Supports IEEE P1284 Level 1 and Level 2 signaling standards for bidirectional parallel communications between personal computers and printing peripherals
■ B Port outputs in High Impedance mode during power down
■ Guaranteed 4000V minimum ESD protection

Ordering Code:

Order Number	Package Number	Package Description
74ACT1284SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74ACT1284MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74ACT1284MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol
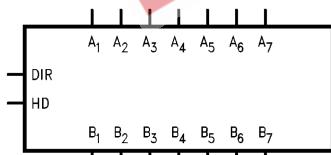
Connection Diagram
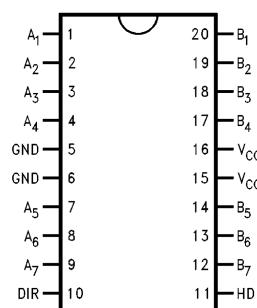
Pin Descriptions

Pin Names	Description
HD	High Drive Enable input (Active HIGH)
DIR	Direction Control Input
$A_1 - A_4$	Side A Inputs or Outputs
$B_1 - B_4$	Side B Inputs or Outputs
$A_5 - A_7$	Side A Inputs
$B_5 - B_7$	Side B Outputs

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Truth Table

Inputs		Outputs
DIR	HD	
L	L	B_1- B_4 Data to A_1 - A_4, and A_5 - A_7 Data to B_5 - B_7 (Note 1)
L	H	B_1- B_4 Data to A_1 - A_4, and A_5 - A_7 Data to B_5 - B_7
H	L	A_1 - A_7 Data to B_1 - B_7 (Note 2)
H	H	A_1 - A_7 Data to B_1 - B_7

Note 1: B_5 - B_7 Open Drain Outputs

Note 2: B_1 - B_7 Open Drain Outputs

Logic Diagram
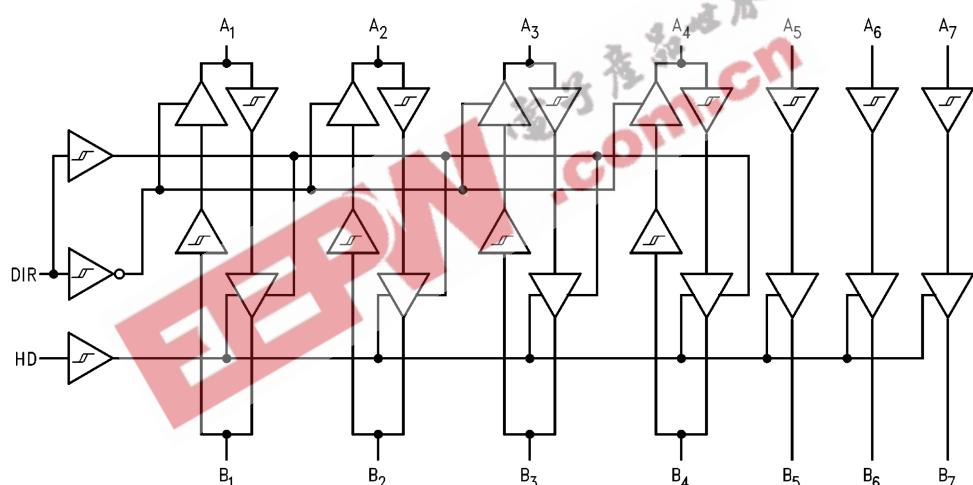
Absolute Maximum Ratings (Note 3)

(Note 4)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = −0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I) A Side	−0.5V to $V_{CC} + 0.5V$
DC Input Voltage (V_I) B Side	−2V to +7V
DC Output Diode Current (I_{OK})	
$V_O = −0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O) A Side	−0.5V to $V_{CC} + 0.5V$
DC Output Voltage (V_O) B Side	−2V to +7V
DC Output Source	
or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	± 50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.7V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C

Note 3: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

Note 4: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Guaranteed Limits			Units	Conditions
			$T_A = +25°C$	$T_A = 0°C$ to +70°C	$T_A = −40°C$ to +85°C		
V_{IH}	Minimum HIGH Level Input Voltage	4.7	2.0	2.0	2.0	V	Recognized High Signal
		5.5	2.0	2.0	2.0		
V_{IL}	Maximum LOW Level Input Voltage	4.7	0.8	0.8	0.8	V	Recognized Low Signal
		5.5	0.8	0.8	0.8		
V_{OH}	Minimum HIGH Level Output Voltage	4.7	4.5	4.5	4.5	V	$I_{OUT} = −50$ µA (An) $V_{IN} = V_{IL}$ or V_{IH} (Note 5)
		4.7	3.7	3.7	3.7		$I_{OH} = −4$ mA (A_n)
		4.7	2.4	2.4	2.4	V	$I_{OH} = −14$ mA (B_n)
V_{OL}	Maximum LOW Level Output Voltage	4.7	0.2	0.2	0.2	V	$I_{OUT} = 50$ µA (An) $V_{IN} = V_{IL}$ or V_{IH} (Note 5)
		4.7	0.4	0.4	0.4		$I_{OH} = 4$ mA (A_n)
						V	$I_{OH} = 14$ mA (B_n)
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	µA	$V_I = V_{CC}$, GND (DIR, A5, A6, A7, HD)
I_{CCT}	Maximum I_{CC}/Input	5.5		1.5	1.5	mA	$V_I = V_{CC} − 2.1V$
I_{CC}	Maximum Quiescent Supply Current	5.5	400	400	500	µA	$V_{IN} = V_{CC}$ or GND
I_{OZ}	Maximum Output Leakage Current	5.5	±20	±20	±20	µA	$V_O = V_{CC}$, GND
I_{OFF}	Maximum B-Side Power Down Leakage Current	0.0	100	100	100	µA	$V_{OUT} = 5.25V$
Δ_{VT}	Input Hysteresis	5.0	0.4	0.4	0.35	V	$V_T + − V_{T^-}$
R_D	Maximum Output Impedance	5.0	22	22	24	Ω	B_n (Note 6)
	Minimum Output Impedance	5.0	8	8	6	Ω	B_n (Note 6)

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: This parameter is guaranteed but not tested, characterized only: RD is the measure of the B-Side output impedance with the output in the HIGH state.

AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$ $V_{CC} = 4.7V - 5.5V$		$T_A = 0°C$ to $+70°C$ $V_{CC} = 4.7V - 5.5V$		$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.7V - 5.5V$		Units	Figure Number
		Min	Max	Min	Max	Min	Max		
t_{PHL}	$A_1 - A_7$ to $B_1 - B_7$	2.0	20.0	2.0	20.0	2.0	24.0	ns	Figure 1
t_{PLH}	$A_1 - A_7$ to $B_1 - B_7$	2.0	20.0	2.0	20.0	2.0	24.0	ns	Figure 2
t_{PHL}	$B_1 - B_4$ to $A_1 - A_4$	2.0	20.0	2.0	20.0	2.0	24.0	ns	Figure 3
t_{PLH}	$B_1 - B_4$ to $A_1 - A_4$	2.0	20.0	2.0	20.0	2.0	24.0	ns	Figure 3
$t_{pEnable}$	Output Enable Time HD to $B_1 - B_7$	2.0	20.0	2.0	20.0	2.0	24.0	ns	Figure 2
$t_{pDisable}$	Output Disable Time HD to $B_1 - B_7$	2.0	20.0	2.0	20.0	2.0	24.0	ns	Figure 2
t_{SKEW} t_{PLH} t_{PHL}	Output Slew Rate $B_1 - B_7$	0.05	0.40	0.05	0.40	0.05	0.40	V/ns	Figure 1 Figure 2
t_r, t_f	t_{RISE} and t_{FALL} $B_1 - B_7$ (Note 7)		120		120		120	ns	Figure 4 (Note 8)

Note 7: Open Drain

Note 8: This parameter is guaranteed but not tested, characterized only.

Note: Pulse Generator for all pulses; Rate $\leq$ 1.0 MHz; $A_O \leq 50\Omega$; $t_f \leq 2.5$ ns, $t_r \leq 2.5$ ns.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.0	pF	V_{CC} = OPEN (HD, DIR $A_5 - A_7$)
$C_{I/O}$	I/O Pin Capacitance	12.0	pF	V_{CC} = 5.0V

AC Loading and Waveforms
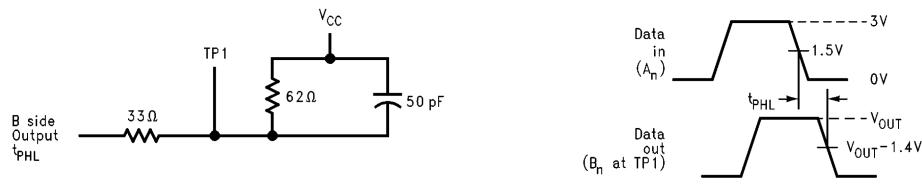
t_{SLEW} measures between 10% to 90% on the t_{PHL} Transition

FIGURE 1. A to B Direction Test Load and Waveforms
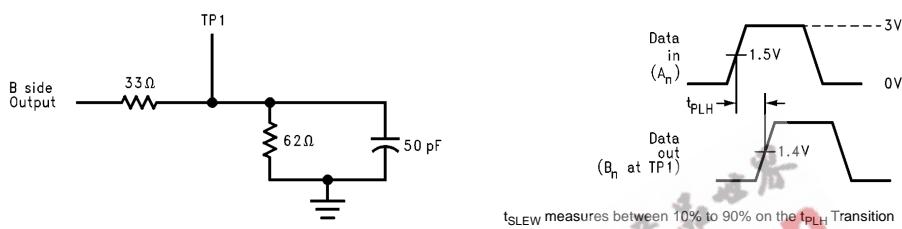
t_{SLEW} measures between 10% to 90% on the t_{PLH} Transition

FIGURE 2. B Output Test Load and Waveforms
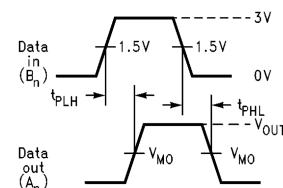
FIGURE 3. B to A Direction Test Load and Waveforms for Outputs A_1 - A_4

FIGURE 4. A to B Direction Test Load and Waveforms for Open Drain B_1 - B_7

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Physical Dimensions inches (millimeters) unless otherwise noted

0.496 – 0.512
(12.598 – 13.005)

0.394 – 0.419
(10.008 – 10.643)

LEAD NO 1
IDENT

30° TYP

0.010 MAX
(0.254)

0.291 – 0.299
(7.391 – 7.595)

0.010 – 0.029
(0.254 – 0.737) × 45°

0.009 – 0.013
(0.229 – 0.330)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

8° MAX TYP
ALL LEADS

0.016 – 0.050
(0.406 – 1.270)
TYP ALL LEADS

0.093 – 0.104
(2.362 – 2.642)

0.014
(0.356)

0.050
(1.270)
TYP

0.008 TYP
(0.203)

0.004 – 0.012
(0.102 – 0.305)

SEATING
PLANE

0.014 – 0.020 TYP
(0.356 – 0.508)

M20B (REV F)
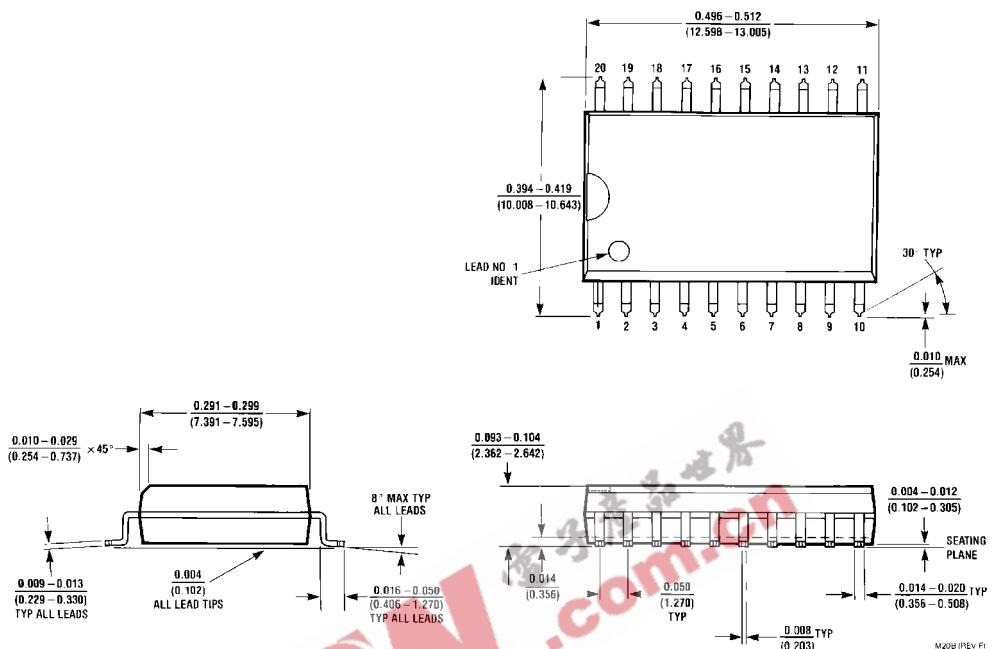
20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B

20   11

1.50

Ø1.2

1   2.35   10

7.40 MAX

7.20 ± 0.05
-A-

0.68 ± 0.12

1.80 ± 0.05

0.800 ± 0.025

0.30 ± 0.10 TYP

0.65 TYP

0.15 +0.05 −0.10
TYP

⌂ 0.10
-C-

⊕ 0.12 Ⓜ C A Ⓢ B Ⓢ

7.90 ± 0.20

5.30 ± 0.05
-B-

0.20 ± 0.05
L/F THICKNESS

4° ± 3°
TYP

0.60 ± 0.15
TYP

MSA20 (REV A)
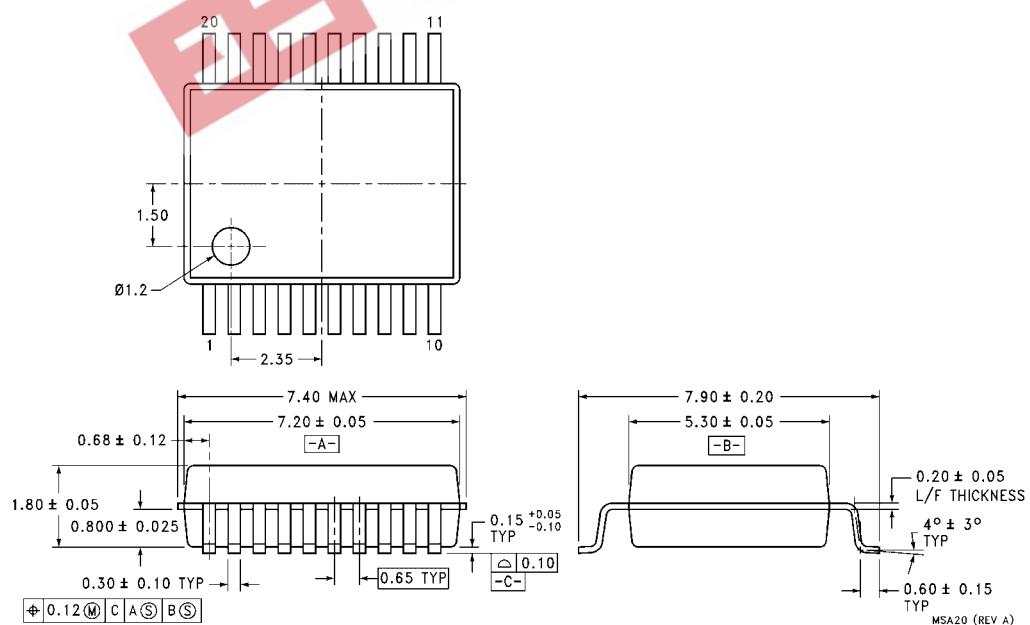
20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

6.5±0.1
-A-
0.20
20   11
-C-
6.4
4.4±0.1 -B-
3.2
0.2 C B A
ALL LEAD TIPS
1   10
PIN #1 IDENT.

4.16   7.72
1.78
0.42
0.65
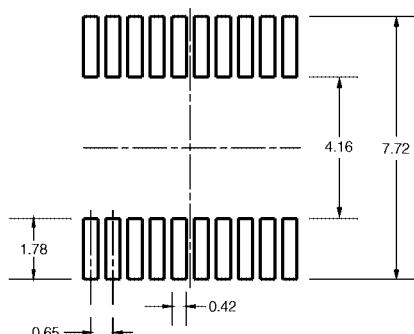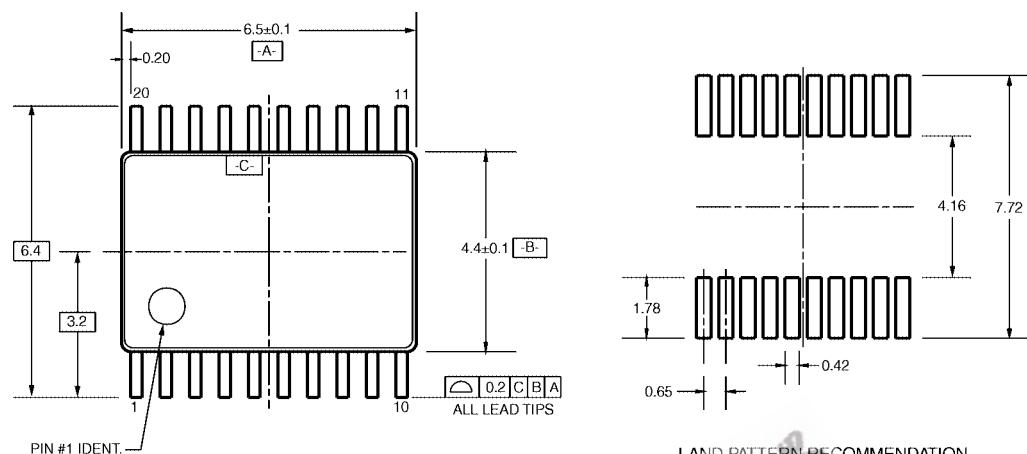
LAND PATTERN RECOMMENDATION

0.1 C
ALL LEAD TIPS
1.2 MAX
0.90 +0.15 -0.10
SEE DETAIL A
0.09-0.20
-C-
0.1±0.05
0.65
0.19-0.30
0.10 M A B S C S

DIMENSIONS ARE IN MILLIMETERS

12.00°
R0.09 MIN
GAGE PLANE
0.25
0 - 8°
SEATING PLANE
R0.09 MIN
0.6 ±0.1
1.00
DETAIL A
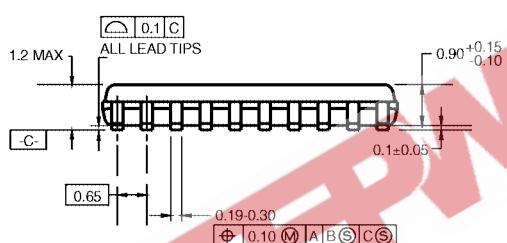
NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1
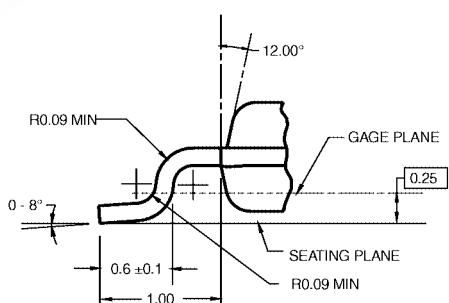
20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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