FAIRCHILD SEMICONDUCTOR™

April 1988
Revised August 1999

74F676
16-Bit Serial/Parallel-In, Serial-Out Shift Register

General Description

The 74F676 contains 16 flip-flops with provision for synchronous parallel or serial entry and serial output. When the Mode (M) input is HIGH, information present on the parallel data (P_0–P_{15}) inputs is entered on the falling edge of the Clock Pulse ($\overline{CP}$) input signal. When M is LOW, data is shifted out of the most significant bit position while information present on the Serial (SI) input shifts into the least significant bit position. A HIGH signal on the Chip Select ($\overline{CS}$) input prevents both parallel and serial operations.

Features

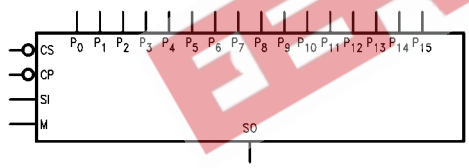
- 16-bit parallel-to-serial conversion
- 16-bit serial-in, serial-out
- Chip select control
- Slim 24 lead 300 mil package

Ordering Code:

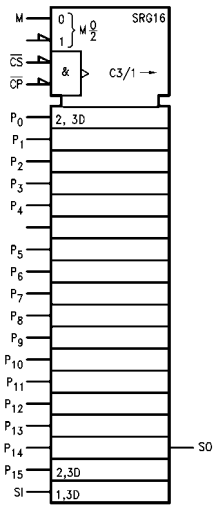
Order Number	Package Number	Package Description
74F676SC	M24B	28-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F676PC	N24A	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600 Wide
74F676SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

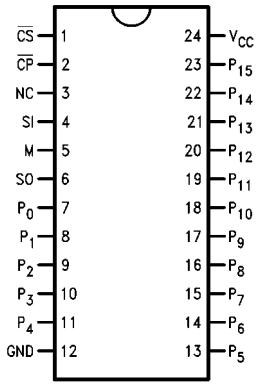
Logic Symbols



IEEE/IEC



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
P_0–P_{15}	Parallel Data Inputs	1.0/1.0	20 µA/–0.6 mA
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
$\overline{CP}$	Clock Pulse Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
M	Mode Select Input	1.0/1.0	20 µA/–0.6 mA
SI	Serial Data Input	1.0/1.0	20 µA/–0.6 mA
SO	Serial Output	50/33.3	–1 mA/20 mA

Functional Description

The 16-bit shift register operates in one of three modes, as indicated in the Shift Register Operations Table.

HOLD— a HIGH signal on the Chip Select ($\overline{CS}$) input prevents clocking, and data is stored in the sixteen registers.

Shift/Serial Load— data present on the SI pin shifts into the register on the falling edge of $\overline{CP}$. Data enters the Q_0 position and shifts toward Q_{15} on successive clocks, finally appearing on the SO pin.

Parallel Load— data present on P_0–P_{15} are entered into the register on the falling edge of $\overline{CP}$. The SO output represents the Q_{15} register output.

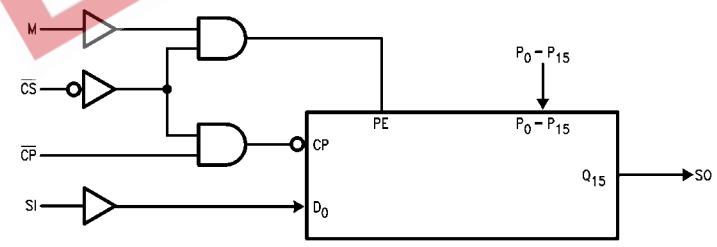
To prevent false clocking, $\overline{CP}$ must be LOW during a LOW-to-HIGH transition of $\overline{CS}$.

Shift Register Operations Table

Control Input			Operating Mode
$\overline{CS}$	M	$\overline{CP}$	
H	X	X	Hold
L	L	⌐	Shift/Serial Load
L	H	⌐	Parallel Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = HIGH-to-LOW Transition

Block Diagram



Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
I_{IH}	Input HIGH Current				5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				7.0	µA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA, All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV, All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CC}	Power Supply Current				72	mA	Max	

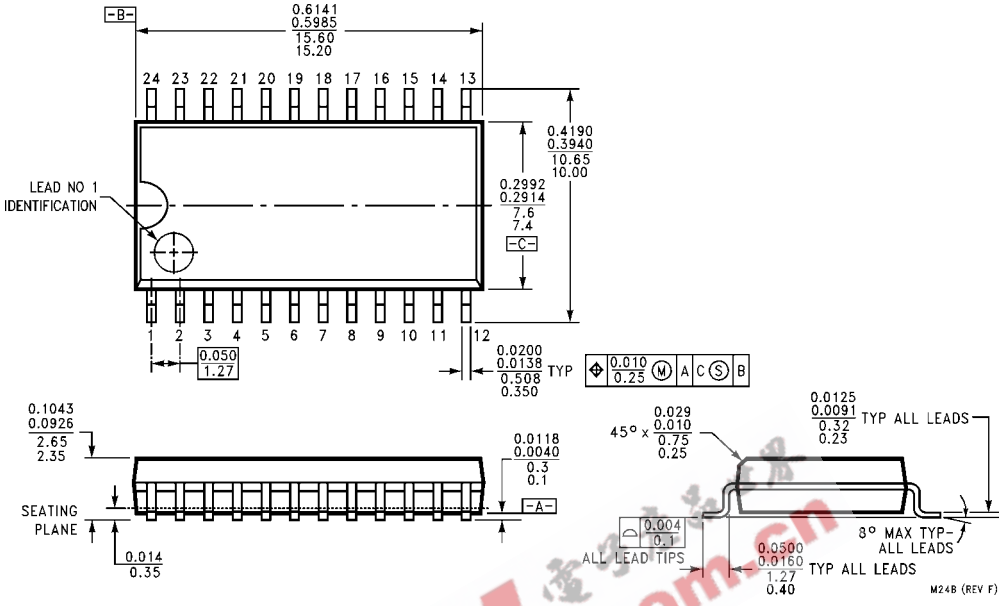
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = -55°C$ to $125°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	100	110		45		90		MHz
t_{PLH}	Propagation Delay	4.5	9.0	11.0	4.5	17.0	4.5	12.0	ns
t_{PHL}	$\overline{CP}$ to SO	5.0	9.0	12.5	5.0	14.5	5.0	13.5	

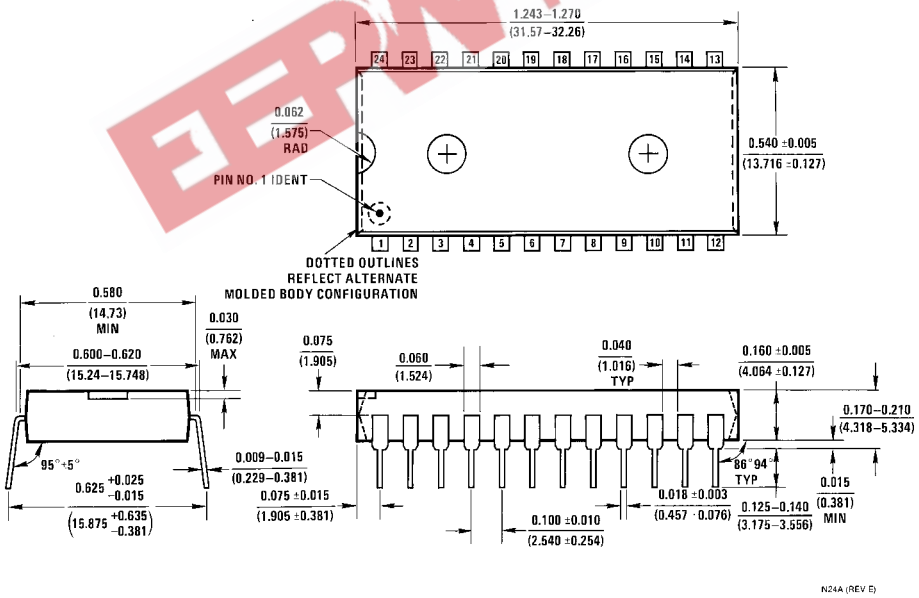
AC Operating Requirements

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$		$T_A = -55°C$ to $125°C$, $V_{CC} = +5.0V$		T_A, V_{CC} = ____, $V_{CC} = +5.0V$		Units
		Min	Max	Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW	4.0		4.0		4.0		ns
$t_S(L)$	SI to $\overline{CP}$	4.0		4.0		4.0		
$t_H(H)$	Hold Time, HIGH or LOW	4.0		4.0		4.0		
$t_H(L)$	SI to $\overline{CP}$	4.0		4.0		4.0		
$t_S(H)$	Setup Time, HIGH or LOW	3.0		3.0		3.0		ns
$t_S(L)$	P_n to $\overline{CP}$	3.0		3.0		3.0		
$t_H(H)$	Hold Time, HIGH or LOW	4.0		4.0		4.0		
$t_H(L)$	P_n to $\overline{CP}$	4.0		4.0		4.0		
$t_S(H)$	Setup Time, HIGH or LOW	8.0		8.0		8.0		ns
$t_S(L)$	M to $\overline{CP}$	8.0		8.0		8.0		
$t_H(H)$	Hold Time, HIGH or LOW	2.0		2.0		2.0		
$t_H(L)$	M to $\overline{CP}$	2.0		2.0		2.0		
$t_S(L)$	Setup Time, LOW $\overline{CS}$ to $\overline{CP}$	10.0		12.0		10.0		ns
$t_H(H)$	Hold Time, HIGH $\overline{CS}$ to $\overline{CP}$	10.0		10.0		10.0		
$t_W(H)$	$\overline{CP}$ Pulse Width	4.0		5.0		4.0		ns
$t_W(L)$	HIGH or LOW	6.0		9.0		6.0		

Physical Dimensions inches (millimeters) unless otherwise noted

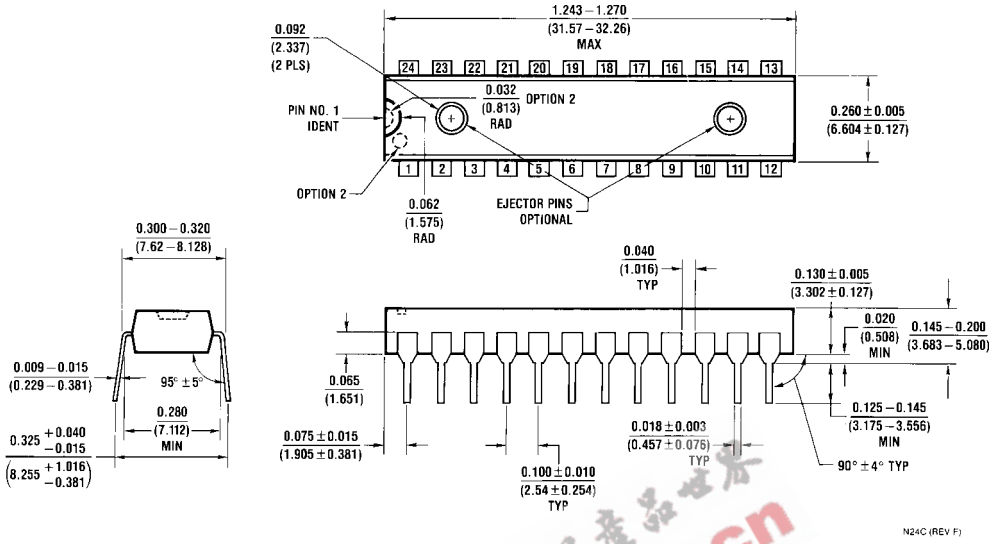


28-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600 Wide
Package Number N24A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide
Package Number N24C

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com