

74AHC594; 74AHCT594

8-bit shift register with output register

Rev. 01 — 4 July 2006

Product data sheet

1. General description

The 74AHC594; 74AHCT594 is a high-speed Si-gate CMOS device and is pin compatible with Low-Power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7A.

The 74AHC594; 74AHCT594 is an 8-bit, non-inverting, serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks (SHCP and STCP) and direct overriding clears (SHR and STR) are provided on both the shift and storage registers. A serial output (Q7S) is provided for cascading purposes.

Both the shift and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register will always be one count pulse ahead of the storage register.

2. Features

- Wide supply voltage range from 2.0 V to 5.5 V
- 8-bit serial-in, parallel-out shift register with storage
- Independent direct overriding clears on shift and storage registers
- Independent clocks for shift and storage registers
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Input levels:
 - ◆ CMOS levels: 74AHC594 only
 - ◆ TTL levels: 74AHCT594 only
- ESD protection:
 - ◆ HBM JESD22-A114-C exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
 - ◆ CDM JESD22-C101-C exceeds 1000 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Applications

- Serial-to parallel data conversion
- Remote control holding register

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4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74AHC594D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AHC594DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74AHC594PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74AHC594BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74AHCT594D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AHCT594DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74AHCT594PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74AHCT594BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

5. Functional diagram

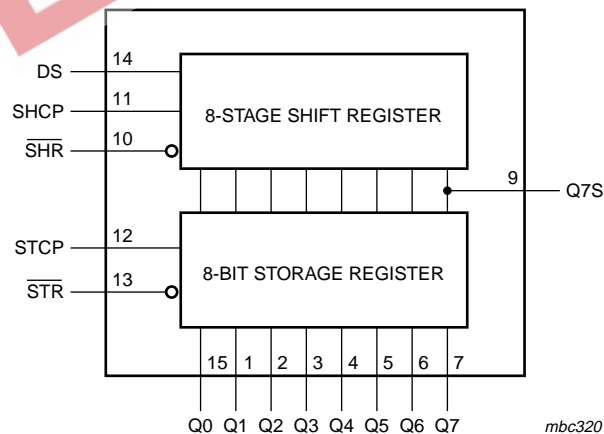


Fig 1. Functional diagram

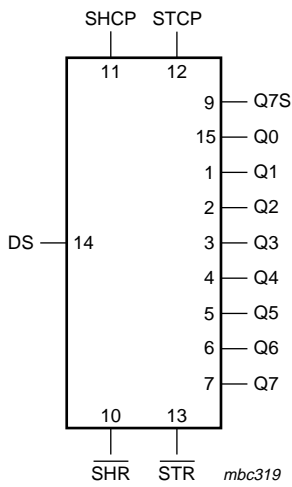


Fig 2. Logic symbol

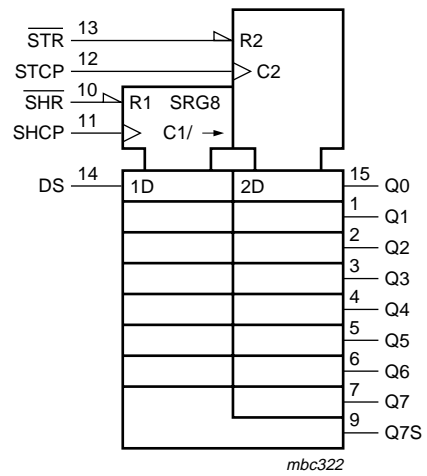


Fig 3. IEC logic symbol

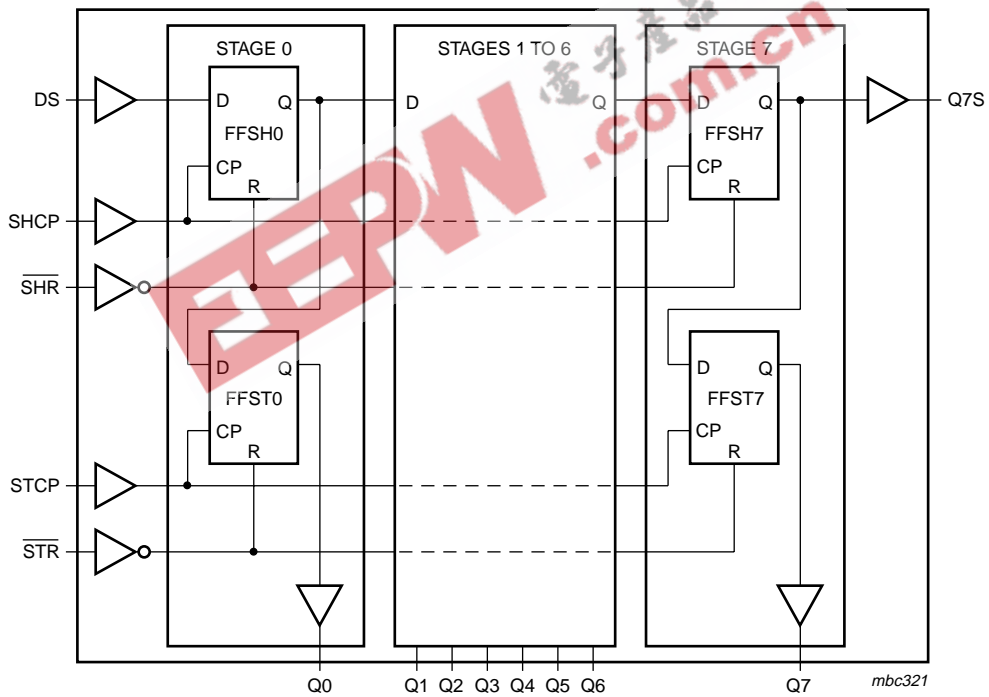
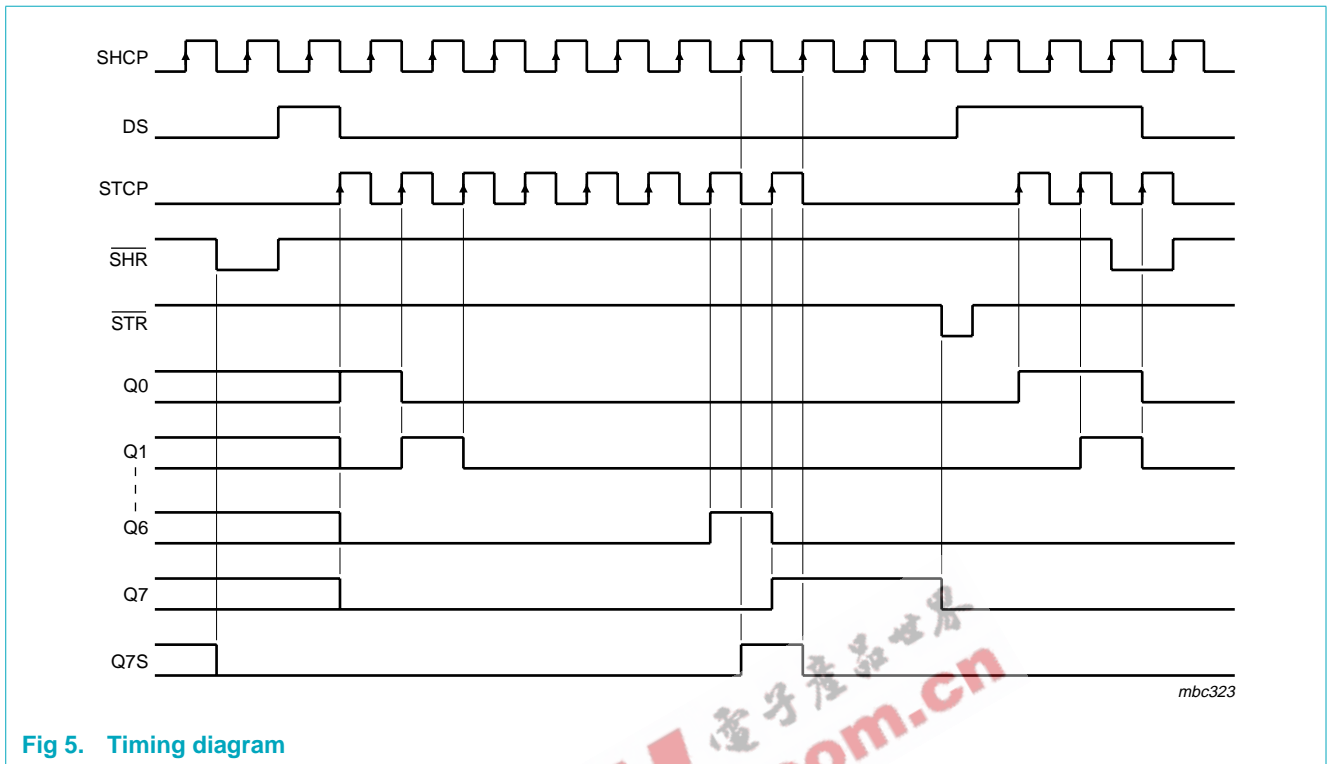
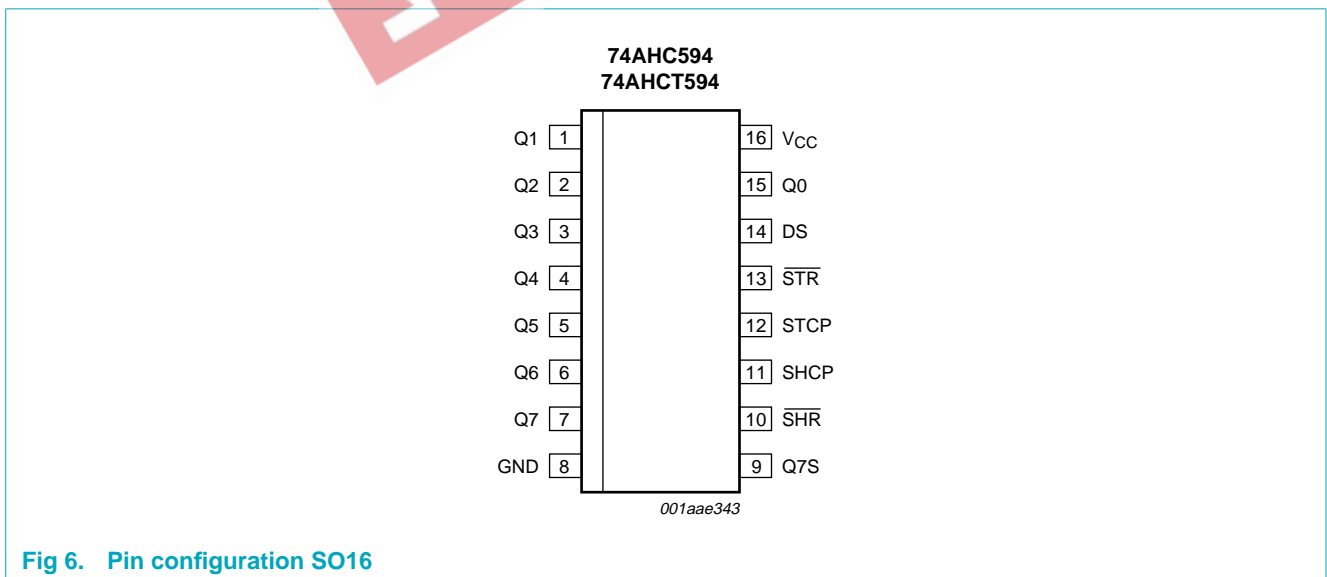


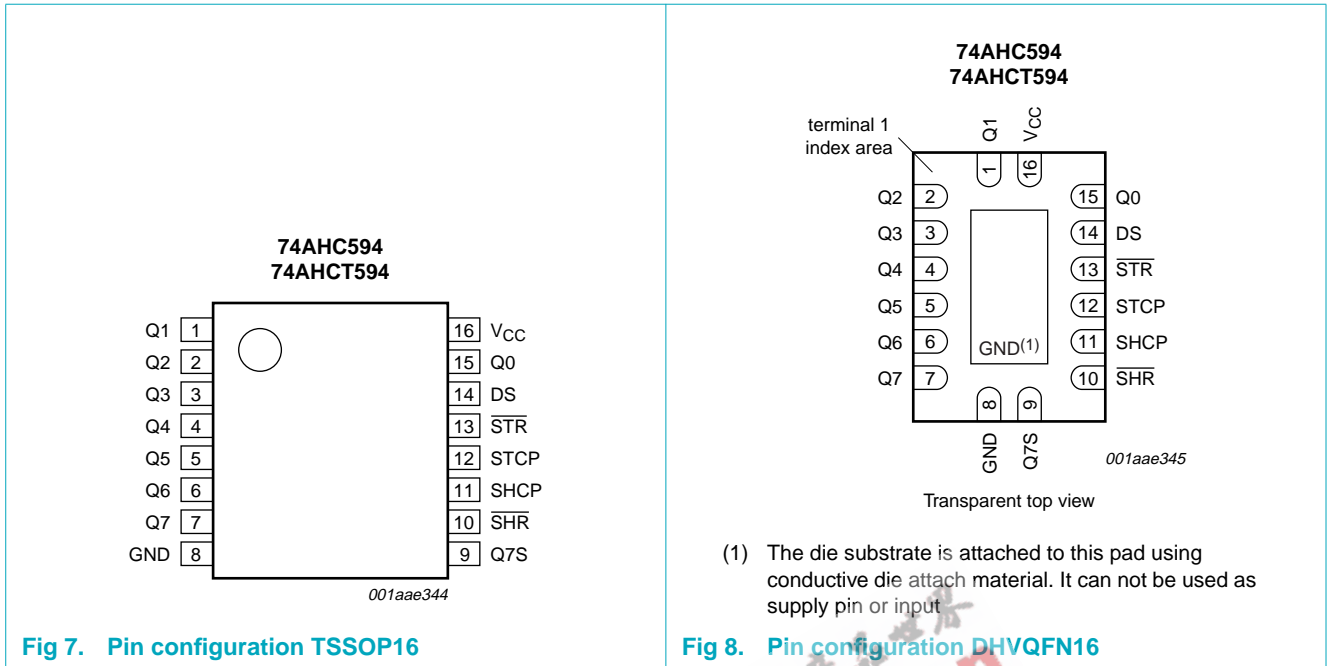
Fig 4. Logic diagram



6. Pinning information

6.1 Pinning





6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Q1	1	parallel data output Q1
Q2	2	parallel data output Q2
Q3	3	parallel data output Q3
Q4	4	parallel data output Q4
Q5	5	parallel data output Q5
Q6	6	parallel data output Q6
Q7	7	parallel data output Q7
GND	8	ground (0 V)
Q7S	9	serial data output Q7S
SHR	10	shift register reset SHR (active LOW)
SHCP	11	shift register clock input SHCP
STCP	12	storage register clock input STCP
STR	13	storage register reset STR (active LOW)
DS	14	serial data input DS
Q0	15	parallel data output Q0
V _{CC}	16	supply voltage

7. Functional description

Table 3. Function table^[1]

Function	Inputs				
	SHR	STR	SHCP	STCP	DS
Clear shift register	L	X	X	X	X
Clear storage register	X	L	X	X	X
Load DS into shift register stage 0, advance previous stage data to the next stage	H	X	↑	X	H or L
Transfer shift register data to storage register and outputs Qn	X	H	X	↑	X

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 ↑ = LOW-to-HIGH transition;
 X = don't care.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V	[1] -	-20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1] -	±20	mA
I_O	output current	$V_O = -0.5$ V to $V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	quiescent supply current		-	75	mA
I_{GND}	ground current		-	-75	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[2] -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 [2] For SO16 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
 For (T)SSOP16 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
 For DHVQFN16 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Type 74AHC594						
V_{CC}	supply voltage		2.0	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	-	-	100	ns/V
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$	-	-	20	ns/V
Type 74AHCT594						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	-	-	20	ns/V

10. Static characteristics

Table 6. Static characteristics type 74AHC594

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25 \text{ °C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0 \text{ V}$	1.5	-	-	V
		$V_{CC} = 3.0 \text{ V}$	2.1	-	-	V
		$V_{CC} = 5.5 \text{ V}$	3.85	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0 \text{ V}$	-	-	0.5	V
		$V_{CC} = 3.0 \text{ V}$	-	-	0.9	V
		$V_{CC} = 5.5 \text{ V}$	-	-	1.65	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -50 \text{ } \mu\text{A}$; $V_{CC} = 2.0 \text{ V}$	1.9	2.0	-	V
		$I_O = -50 \text{ } \mu\text{A}$; $V_{CC} = 3.0 \text{ V}$	2.9	3.0	-	V
		$I_O = -50 \text{ } \mu\text{A}$; $V_{CC} = 4.5 \text{ V}$	4.4	4.5	-	V
		$I_O = -4.0 \text{ mA}$; $V_{CC} = 3.0 \text{ V}$	2.58	-	-	V
	$I_O = -8.0 \text{ mA}$; $V_{CC} = 4.5 \text{ V}$	3.94	-	-	V	
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 50 \text{ } \mu\text{A}$; $V_{CC} = 2.0 \text{ V}$	-	0	0.1	V
		$I_O = 50 \text{ } \mu\text{A}$; $V_{CC} = 3.0 \text{ V}$	-	0	0.1	V
		$I_O = 50 \text{ } \mu\text{A}$; $V_{CC} = 4.5 \text{ V}$	-	0	0.1	V
		$I_O = 4 \text{ mA}$; $V_{CC} = 3.0 \text{ V}$	-	-	0.36	V
	$I_O = 8 \text{ mA}$; $V_{CC} = 4.5 \text{ V}$	-	-	0.36	V	
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	0.1	μA

Table 6. Static characteristics type 74AHC594 ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	4.0	μ A
C_I	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	pF
$T_{amb} = -40$ °C to $+85$ °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0$ V	1.5	-	-	V
		$V_{CC} = 3.0$ V	2.1	-	-	V
		$V_{CC} = 5.5$ V	3.85	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0$ V	-	-	0.5	V
		$V_{CC} = 3.0$ V	-	-	0.9	V
		$V_{CC} = 5.5$ V	-	-	1.65	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -50$ μ A; $V_{CC} = 2.0$ V	1.9	-	-	V
		$I_O = -50$ μ A; $V_{CC} = 3.0$ V	2.9	-	-	V
		$I_O = -50$ μ A; $V_{CC} = 4.5$ V	4.4	-	-	V
		$I_O = -4.0$ mA; $V_{CC} = 3.0$ V	2.48	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 50$ μ A; $V_{CC} = 2.0$ V	-	-	0.1	V
		$I_O = 50$ μ A; $V_{CC} = 3.0$ V	-	-	0.1	V
		$I_O = 50$ μ A; $V_{CC} = 4.5$ V	-	-	0.1	V
		$I_O = 4$ mA; $V_{CC} = 3.0$ V	-	-	0.44	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	1.0	μ A
		$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	40	μ A
$T_{amb} = -40$ °C to $+125$ °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0$ V	1.5	-	-	V
		$V_{CC} = 3.0$ V	2.1	-	-	V
		$V_{CC} = 5.5$ V	3.85	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0$ V	-	-	0.5	V
		$V_{CC} = 3.0$ V	-	-	0.9	V
		$V_{CC} = 5.5$ V	-	-	1.65	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -50$ μ A; $V_{CC} = 2.0$ V	1.9	-	-	V
		$I_O = -50$ μ A; $V_{CC} = 3.0$ V	2.9	-	-	V
		$I_O = -50$ μ A; $V_{CC} = 4.5$ V	4.4	-	-	V
		$I_O = -4.0$ mA; $V_{CC} = 3.0$ V	2.40	-	-	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	1.0	μ A
		$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	40	μ A

Table 6. Static characteristics type 74AHC594 ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 50 \mu\text{A}; V_{CC} = 2.0 \text{ V}$	-	-	0.1	V
		$I_O = 50 \mu\text{A}; V_{CC} = 3.0 \text{ V}$	-	-	0.1	V
		$I_O = 50 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	-	-	0.1	V
		$I_O = 4 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.55	V
		$I_O = 8 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.55	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}; V_{CC} = 5.5 \text{ V}$	-	-	80	μA

Table 7. Static characteristics type 74AHCT594

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25 \text{ }^\circ\text{C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -50 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	4.4	4.5	-	V
		$I_O = -8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.94	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 50 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	-	0	0.1	V
		$I_O = 8 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.36	V
I_I	input leakage current	$V_I = V_{IH}$ or $V_{IL}; V_{CC} = 5.5 \text{ V}$	-	-	0.1	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}; V_{CC} = 5.5 \text{ V}$	-	-	4.0	μA
ΔI_{CC}	additional quiescent supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$; other inputs at V_{CC} or GND; $I_O = 0 \text{ A}; V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	1.35	mA
C_I	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	pF
$T_{amb} = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -50 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	4.4	-	-	V
		$I_O = -8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.8	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 50 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	-	-	0.1	V
		$I_O = 8 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.44	V
I_I	input leakage current	$V_I = V_{IH}$ or $V_{IL}; V_{CC} = 5.5 \text{ V}$	-	-	1.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}; V_{CC} = 5.5 \text{ V}$	-	-	40	μA

Table 7. Static characteristics type 74AHCT594 ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔI_{CC}	additional quiescent supply current	per input pin; $V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND; $I_O = 0$ A; $V_{CC} = 4.5$ V to 5.5 V	-	-	1.5	mA
$T_{amb} = -40$ °C to $+125$ °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -50$ μ A; $V_{CC} = 4.5$ V	4.4	-	-	V
		$I_O = -8.0$ mA; $V_{CC} = 4.5$ V	3.70	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 50$ μ A; $V_{CC} = 4.5$ V	-	-	0.1	V
		$I_O = 8$ mA; $V_{CC} = 4.5$ V	-	-	0.55	V
I_I	input leakage current	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 5.5$ V	-	-	2.0	μ A
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	80	μ A
ΔI_{CC}	additional quiescent supply current	per input pin; $V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND; $I_O = 0$ A; $V_{CC} = 4.5$ V to 5.5 V	-	-	1.5	mA

11. Dynamic characteristics

Table 8. Dynamic characteristics type 74AHC594GND = 0 V; $t_r = t_f \leq 3.0$ ns; see Figure 15.

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$T_{amb} = 25$ °C						
t_{PLH}	LOW-to-HIGH propagation delay SHCP to Q7S	$V_{CC} = 3.0$ V to 3.6 V; see Figure 9				
		$C_L = 15$ pF	-	5.2	8.5	ns
		$C_L = 50$ pF	-	7.4	11.5	ns
		$V_{CC} = 4.5$ V to 5.5 V; see Figure 9				
		$C_L = 15$ pF	-	3.8	6.3	ns
		$C_L = 50$ pF	-	4.8	8.0	ns
t_{PHL}	HIGH-to-LOW propagation delay SHCP to Q7S	$V_{CC} = 3.0$ V to 3.6 V; see Figure 9				
		$C_L = 15$ pF	-	5.5	8.9	ns
		$C_L = 50$ pF	-	7.4	12.1	ns
		$V_{CC} = 4.5$ V to 5.5 V; see Figure 9				
		$C_L = 15$ pF	-	4.1	6.7	ns
		$C_L = 50$ pF	-	5.4	8.8	ns

Table 8. Dynamic characteristics type 74AHC594 ...continuedGND = 0 V; $t_r = t_f \leq 3.0$ ns; see [Figure 15](#).

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{PLH}	LOW-to-HIGH propagation delay STCP to Qn	$V_{CC} = 3.0$ V to 3.6 V; see Figure 10				
		$C_L = 15$ pF	-	5.1	8.3	ns
		$C_L = 50$ pF	-	7.3	11.9	ns
		$V_{CC} = 4.5$ V to 5.5 V; see Figure 10				
		$C_L = 15$ pF	-	3.5	5.7	ns
		$C_L = 50$ pF	-	4.8	7.8	ns
t_{PHL}	HIGH-to-LOW propagation delay STCP to Qn	$V_{CC} = 3.0$ V to 3.6 V; see Figure 10				
		$C_L = 15$ pF	-	5.5	9.1	ns
		$C_L = 50$ pF	-	7.3	12.0	ns
		$V_{CC} = 4.5$ V to 5.5 V; see Figure 10				
		$C_L = 15$ pF	-	3.7	6.0	ns
		$C_L = 50$ pF	-	5.2	8.5	ns
t_{PHL}	HIGH-to-LOW propagation delay SHR to Q7S	$V_{CC} = 3.0$ V to 3.6 V; see Figure 13				
		$C_L = 15$ pF	-	5.7	9.5	ns
		$C_L = 50$ pF	-	7.5	12.2	ns
		$V_{CC} = 4.5$ V to 5.5 V; see Figure 13				
		$C_L = 15$ pF	-	4.1	6.7	ns
		$C_L = 50$ pF	-	5.4	8.8	ns
	HIGH-to-LOW propagation delay STR to Qn	$V_{CC} = 3.0$ V to 3.6 V; see Figure 14				
		$C_L = 15$ pF	-	5.8	9.6	ns
		$C_L = 50$ pF	-	7.7	12.5	ns
		$V_{CC} = 4.5$ V to 5.5 V; see Figure 14				
	$C_L = 15$ pF	-	4.1	7.2	ns	
	$C_L = 50$ pF	-	5.4	9.4	ns	
t_w	pulse width HIGH or LOW SHCP and STCP	$C_L = 50$ pF; see Figure 9 and Figure 10				
		$V_{CC} = 3.0$ V to 3.6 V	6.0	-	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	5.5	-	-	ns
	pulse width HIGH or LOW SHR and STR	$C_L = 50$ pF; see Figure 13 and Figure 14				
		$V_{CC} = 3.0$ V to 3.6 V	5.0	-	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	5.0	-	-	ns
t_{su}	set-up time DS to SHCP	$C_L = 50$ pF; see Figure 11				
		$V_{CC} = 3.0$ V to 3.6 V	3.5	-	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	3.0	-	-	ns
	set-up time SHR to STCP	$C_L = 50$ pF; see Figure 12				
		$V_{CC} = 3.0$ V to 3.6 V	8.0	-	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	5.0	-	-	ns
	set-up time SHCP to STCP	$C_L = 50$ pF; see Figure 10				
		$V_{CC} = 3.0$ V to 3.6 V	8.0	-	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	5.0	-	-	ns

Table 8. Dynamic characteristics type 74AHC594 ...continuedGND = 0 V; $t_r = t_f \leq 3.0$ ns; see [Figure 15](#).

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_h	hold time DS to SHCP	$C_L = 50$ pF; see Figure 11				
		$V_{CC} = 3.0$ V to 3.6 V	1.5	-	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	2.0	-	-	ns
t_{rec}	recovery time SHR to SHCP	$C_L = 50$ pF; see Figure 13				
		$V_{CC} = 3.0$ V to 3.6 V	4.2	-	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	2.9	-	-	ns
	recovery time STR to STCP	$C_L = 50$ pF; see Figure 14				
		$V_{CC} = 3.0$ V to 3.6 V	4.6	-	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	3.2	-	-	ns
f_{max}	maximum frequency SHCP or STCP	$C_L = 50$ pF; see Figure 9 and Figure 10				
		$V_{CC} = 3.0$ V to 3.6 V	80	125	-	MHz
		$V_{CC} = 4.5$ V to 5.5 V	90	170	-	MHz
C_{PD}	power dissipation capacitance	$V_I = \text{GND to } V_{CC}$; $V_{CC} = 5$ V; $C_L = 50$ pF; $f_i = 1$ MHz	2	55	-	pF
$T_{amb} = -40$ °C to $+85$ °C						
t_{PLH}	LOW-to-HIGH propagation delay SHCP to Q7S	$V_{CC} = 3.0$ V to 3.6 V; see Figure 9				
		$C_L = 15$ pF	2.2	-	9.7	ns
		$C_L = 50$ pF	3.0	-	13.2	ns
		$V_{CC} = 4.5$ V to 5.5 V; see Figure 9				
		$C_L = 15$ pF	1.7	-	7.2	ns
		$C_L = 50$ pF	2.4	-	9.1	ns
t_{PHL}	HIGH-to-LOW propagation delay SHCP to Q7S	$V_{CC} = 3.0$ V to 3.6 V; see Figure 9				
		$C_L = 15$ pF	2.3	-	10.2	ns
		$C_L = 50$ pF	3.0	-	13.9	ns
		$V_{CC} = 4.5$ V to 5.5 V; see Figure 9				
		$C_L = 15$ pF	1.9	-	7.6	ns
		$C_L = 50$ pF	2.5	-	10.1	ns
t_{PLH}	LOW-to-HIGH propagation delay STCP to Qn	$V_{CC} = 3.0$ V to 3.6 V; see Figure 10				
		$C_L = 15$ pF	2.3	-	9.5	ns
		$C_L = 50$ pF	3.3	-	13.6	ns
		$V_{CC} = 4.5$ V to 5.5 V; see Figure 10				
		$C_L = 15$ pF	1.8	-	6.5	ns
		$C_L = 50$ pF	2.6	-	9.0	ns
t_{PHL}	HIGH-to-LOW propagation delay STCP to Qn	$V_{CC} = 3.0$ V to 3.6 V; see Figure 10				
		$C_L = 15$ pF	2.4	-	10.4	ns
		$C_L = 50$ pF	3.2	-	13.8	ns
		$V_{CC} = 4.5$ V to 5.5 V; see Figure 10				
		$C_L = 15$ pF	1.9	-	6.9	ns
		$C_L = 50$ pF	2.6	-	9.7	ns

Table 8. Dynamic characteristics type 74AHC594 ...continuedGND = 0 V; $t_r = t_f \leq 3.0$ ns; see [Figure 15](#).

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{PHL}	HIGH-to-LOW propagation delay SHR to Q7S	$V_{CC} = 3.0$ V to 3.6 V; see Figure 13				
		$C_L = 15$ pF	2.3	-	10.8	ns
		$C_L = 50$ pF	3.6	-	14.0	ns
		$V_{CC} = 4.5$ V to 5.5 V; see Figure 13				
		$C_L = 15$ pF	2.0	-	7.6	ns
		$C_L = 50$ pF	2.8	-	10.1	ns
	HIGH-to-LOW propagation delay STR to Qn	$V_{CC} = 3.0$ V to 3.6 V; see Figure 14				
		$C_L = 15$ pF	2.8	-	11.0	ns
		$C_L = 50$ pF	3.8	-	14.4	ns
		$V_{CC} = 4.5$ V to 5.5 V; see Figure 14				
$C_L = 15$ pF		2.2	-	8.2	ns	
$C_L = 50$ pF		3.0	-	10.7	ns	
t_W	pulse width HIGH or LOW SHCP and STCP	$C_L = 50$ pF; see Figure 9 and Figure 10				
		$V_{CC} = 3.0$ V to 3.6 V	6.5	-	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	6.0	-	-	ns
	pulse width HIGH or LOW SHR and STR	$C_L = 50$ pF; see Figure 13 and Figure 14				
		$V_{CC} = 3.0$ V to 3.6 V	5.0	-	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	5.2	-	-	ns
t_{su}	set-up time DS to SHCP	$C_L = 50$ pF; see Figure 11				
		$V_{CC} = 3.0$ V to 3.6 V	3.5	-	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	3.0	-	-	ns
	set-up time SHR to STCP	$C_L = 50$ pF; see Figure 12				
		$V_{CC} = 3.0$ V to 3.6 V	9.0	-	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	5.0	-	-	ns
	set-up time SHCP to STCP	$C_L = 50$ pF; see Figure 10				
		$V_{CC} = 3.0$ V to 3.6 V	8.5	-	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	5.0	-	-	ns
t_h	hold time DS to SHCP	$C_L = 50$ pF; see Figure 11				
		$V_{CC} = 3.0$ V to 3.6 V	1.5	-	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	2.0	-	-	ns
t_{rec}	recovery time SHR to SHCP	$C_L = 50$ pF; see Figure 13				
		$V_{CC} = 3.0$ V to 3.6 V	4.8	-	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	3.3	-	-	ns
	recovery time STR to STCP	$C_L = 50$ pF; see Figure 14				
		$V_{CC} = 3.0$ V to 3.6 V	5.3	-	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	3.7	-	-	ns

Table 8. Dynamic characteristics type 74AHC594 ...continuedGND = 0 V; $t_r = t_f \leq 3.0$ ns; see [Figure 15](#).

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
f_{\max}	maximum frequency SHCP or STCP	$C_L = 50$ pF; see Figure 9 and Figure 10				
		$V_{CC} = 3.0$ V to 3.6 V	70	-	-	MHz
		$V_{CC} = 4.5$ V to 5.5 V	80	-	-	MHz
$T_{\text{amb}} = -40$ °C to $+125$ °C						
t_{PLH}	LOW-to-HIGH propagation delay SHCP to Q7S	$V_{CC} = 3.0$ V to 3.6 V; see Figure 9				
		$C_L = 15$ pF	2.2	-	10.6	ns
		$C_L = 50$ pF	3.0	-	14.3	ns
		$V_{CC} = 4.5$ V to 5.5 V; see Figure 9				
		$C_L = 15$ pF	1.7	-	7.8	ns
t_{PHL}	HIGH-to-LOW propagation delay SHCP to Q7S	$V_{CC} = 3.0$ V to 3.6 V; see Figure 9				
		$C_L = 15$ pF	2.3	-	11.0	ns
		$C_L = 50$ pF	3.0	-	15.1	ns
		$V_{CC} = 4.5$ V to 5.5 V; see Figure 9				
		$C_L = 15$ pF	1.9	-	8.2	ns
t_{PLH}	LOW-to-HIGH propagation delay STCP to Qn	$V_{CC} = 3.0$ V to 3.6 V; see Figure 10				
		$C_L = 15$ pF	2.3	-	10.6	ns
		$C_L = 50$ pF	3.3	-	14.7	ns
		$V_{CC} = 4.5$ V to 5.5 V; see Figure 10				
		$C_L = 15$ pF	1.8	-	7.1	ns
t_{PHL}	HIGH-to-LOW propagation delay STCP to Qn	$V_{CC} = 3.0$ V to 3.6 V; see Figure 10				
		$C_L = 15$ pF	2.4	-	11.3	ns
		$C_L = 50$ pF	3.2	-	15.0	ns
		$V_{CC} = 4.5$ V to 5.5 V; see Figure 10				
		$C_L = 15$ pF	1.9	-	7.5	ns
		$C_L = 50$ pF	2.6	-	10.5	ns

Table 8. Dynamic characteristics type 74AHC594 ...continuedGND = 0 V; $t_r = t_f \leq 3.0$ ns; see [Figure 15](#).

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{PHL}	HIGH-to-LOW propagation delay SHR to Q7S	$V_{CC} = 3.0$ V to 3.6 V; see Figure 13				
		$C_L = 15$ pF	2.3	-	11.7	ns
		$C_L = 50$ pF	3.6	-	15.2	ns
		$V_{CC} = 4.5$ V to 5.5 V; see Figure 13				
		$C_L = 15$ pF	2.0	-	8.2	ns
		$C_L = 50$ pF	2.8	-	11.0	ns
	HIGH-to-LOW propagation delay STR to Qn	$V_{CC} = 3.0$ V to 3.6 V; see Figure 14				
		$C_L = 15$ pF	2.8	-	12.0	ns
		$C_L = 50$ pF	3.8	-	15.6	ns
		$V_{CC} = 4.5$ V to 5.5 V; see Figure 14				
$C_L = 15$ pF		2.2	-	8.9	ns	
$C_L = 50$ pF		3.0	-	11.6	ns	
t_W	pulse width HIGH or LOW SHCP and STCP	$C_L = 50$ pF; see Figure 9 and Figure 10				
		$V_{CC} = 3.0$ V to 3.6 V	7.0	-	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	6.5	-	-	ns
	pulse width HIGH or LOW SHR and STR	$C_L = 50$ pF; see Figure 13 and Figure 14				
		$V_{CC} = 3.0$ V to 3.6 V	5.5	-	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	5.7	-	-	ns
t_{su}	set-up time DS to SHCP	$C_L = 50$ pF; see Figure 11				
		$V_{CC} = 3.0$ V to 3.6 V	4.0	-	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	3.5	-	-	ns
	set-up time SHR to STCP	$C_L = 50$ pF; see Figure 12				
		$V_{CC} = 3.0$ V to 3.6 V	9.5	-	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	5.5	-	-	ns
	set-up time SHCP to STCP	$C_L = 50$ pF; see Figure 10				
		$V_{CC} = 3.0$ V to 3.6 V	9.0	-	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	5.5	-	-	ns
t_h	hold time DS to SHCP	$C_L = 50$ pF; see Figure 11				
		$V_{CC} = 3.0$ V to 3.6 V	2.0	-	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	2.5	-	-	ns
t_{rec}	recovery time SHR to SHCP	$C_L = 50$ pF; see Figure 13				
		$V_{CC} = 3.0$ V to 3.6 V	5.3	-	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	3.8	-	-	ns
	recovery time STR to STCP	$C_L = 50$ pF; see Figure 14				
		$V_{CC} = 3.0$ V to 3.6 V	5.8	-	-	ns
		$V_{CC} = 4.5$ V to 5.5 V	4.3	-	-	ns

Table 8. Dynamic characteristics type 74AHC594 ...continuedGND = 0 V; $t_r = t_f \leq 3.0$ ns; see [Figure 15](#).

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
f_{\max}	maximum frequency SHCP or STCP	$C_L = 50$ pF; see Figure 9 and Figure 10				
		$V_{CC} = 3.0$ V to 3.6 V	65	-	-	MHz
		$V_{CC} = 4.5$ V to 5.5 V	70	-	-	MHz

[1] Typical values are measured at nominal V_{CC} .[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

 f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.**Table 9.** Dynamic characteristics type 74AHCT594GND = 0 V; $t_r = t_f \leq 3.0$ ns; $V_{CC} = 4.5$ V to 5.5 V; see [Figure 15](#)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$T_{\text{amb}} = 25$ °C [1]						
t_{PLH}	LOW-to-HIGH propagation delay SHCP to Q7S	see Figure 9				
		$C_L = 15$ pF	-	3.8	6.3	ns
		$C_L = 50$ pF	-	4.8	8.0	ns
t_{PHL}	HIGH-to-LOW and LOW-to-HIGH propagation delay SHCP to Q7S	see Figure 9				
		$C_L = 15$ pF	-	4.1	6.7	ns
		$C_L = 50$ pF	-	5.4	8.8	ns
t_{PLH}	LOW-to-HIGH propagation delay STCP to Qn	see Figure 10				
		$C_L = 15$ pF	-	3.5	5.7	ns
		$C_L = 50$ pF	-	4.6	7.7	ns
t_{PHL}	HIGH-to-LOW propagation delay STCP to Qn	see Figure 10				
		$C_L = 15$ pF	-	3.7	6.1	ns
		$C_L = 50$ pF	-	5.2	8.5	ns
t_{PHL}	HIGH-to-LOW propagation delay SHR to Q7S	see Figure 13				
		$C_L = 15$ pF	-	4.3	7.0	ns
		$C_L = 50$ pF	-	5.4	8.8	ns
	HIGH-to-LOW propagation delay STR to Qn	see Figure 14				
		$C_L = 15$ pF	-	4.5	7.4	ns
		$C_L = 50$ pF	-	5.7	9.4	ns
t_W	pulse width HIGH or LOW SHCP and STCP	$C_L = 50$ pF; see Figure 9 and Figure 10	5.5	-	-	ns
	pulse width HIGH or LOW SHR and STR	$C_L = 50$ pF; see Figure 13 and Figure 14	5.2	-	-	ns

Table 9. Dynamic characteristics type 74AHCT594 ...continuedGND = 0 V; $t_r = t_f \leq 3.0$ ns; $V_{CC} = 4.5$ V to 5.5 V; see [Figure 15](#)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{su}	set-up time DS to SHCP	$C_L = 50$ pF; see Figure 11	3.0	-	-	ns
	set-up time SHR to STCP	$C_L = 50$ pF; see Figure 12	5.0	-	-	ns
	set-up time SHCP to STCP	$C_L = 50$ pF; see Figure 10	5.0	-	-	ns
t_h	hold time DS to SHCP	see Figure 11	2.0	-	-	ns
t_{rec}	recovery time SHR to SHCP	$C_L = 50$ pF; see Figure 13	2.9	-	-	ns
	recovery time STR to STCP	$C_L = 50$ pF; see Figure 14	3.4	-	-	ns
f_{max}	maximum frequency SHCP or STCP	$C_L = 50$ pF; see Figure 9 and Figure 10	90	160	-	MHz
C_{PD}	power dissipation capacitance	$V_I = \text{GND}$ to V_{CC} ; $V_{CC} = 5$ V; $C_L = 50$ pF; $f_i = 1$ MHz	2	55	-	pF
$T_{amb} = -40$ °C to $+85$ °C						
t_{PLH}	LOW-to-HIGH propagation delay SHCP to Q7S	see Figure 9				
		$C_L = 15$ pF	1.7	-	7.2	ns
t_{PHL}	HIGH-to-LOW propagation delay SHCP to Q7S	$C_L = 50$ pF	2.2	-	9.1	ns
		see Figure 9				
t_{PLH}	LOW-to-HIGH propagation delay STCP to Qn	$C_L = 15$ pF	1.8	-	7.6	ns
		$C_L = 50$ pF	2.4	-	10.1	ns
t_{PHL}	HIGH-to-LOW propagation delay STCP to Qn	see Figure 10				
		$C_L = 15$ pF	1.8	-	6.5	ns
t_{PHL}	HIGH-to-LOW propagation delay STR to Qn	$C_L = 50$ pF	2.6	-	8.8	ns
		see Figure 10				
t_{PHL}	HIGH-to-LOW propagation delay SHR to Q7S	$C_L = 15$ pF	1.9	-	6.9	ns
		$C_L = 50$ pF	2.6	-	9.7	ns
t_{PHL}	HIGH-to-LOW propagation delay STR to Qn	see Figure 13				
		$C_L = 15$ pF	2.4	-	8.0	ns
t_{PHL}	HIGH-to-LOW propagation delay STR to Qn	$C_L = 50$ pF	2.7	-	10.1	ns
		see Figure 14				
t_w	pulse width HIGH or LOW SHCP and STCP	$C_L = 15$ pF	2.3	-	8.4	ns
		$C_L = 50$ pF	3.1	-	10.7	ns
t_w	pulse width HIGH or LOW SHR and STR	$C_L = 50$ pF; see Figure 9 and Figure 10	6.0	-	-	ns
		$C_L = 50$ pF; see Figure 13 and Figure 14	5.5	-	-	ns

Table 9. Dynamic characteristics type 74AHCT594 ...continuedGND = 0 V; $t_r = t_f \leq 3.0$ ns; $V_{CC} = 4.5$ V to 5.5 V; see [Figure 15](#)

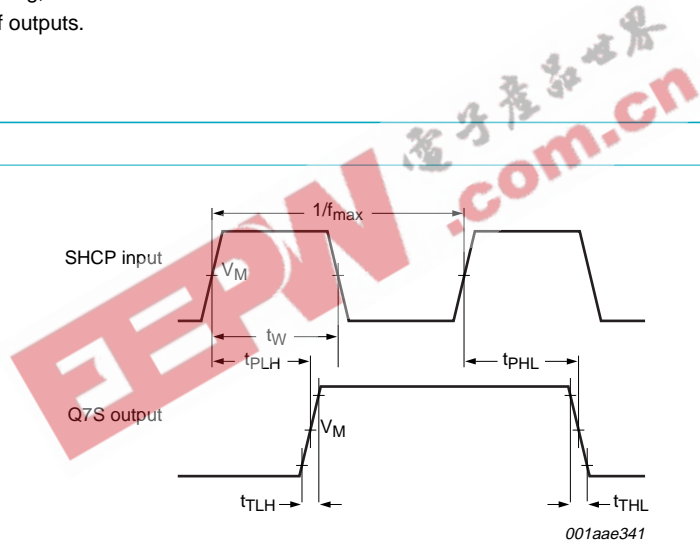
Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{su}	set-up time DS to SHCP	$C_L = 50$ pF; see Figure 11	3.0	-	-	ns
	set-up time SHR to STCP	$C_L = 50$ pF; see Figure 12	5.0	-	-	ns
	set-up time SHCP to STCP	$C_L = 50$ pF; see Figure 10	5.0	-	-	ns
t_h	hold time DS to SHCP	see Figure 11	2.0	-	-	ns
t_{rec}	recovery time SHR to SHCP	$C_L = 50$ pF; see Figure 13	3.3	-	-	ns
	recovery time STR to STCP	$C_L = 50$ pF; see Figure 14	3.8	-	-	ns
f_{max}	maximum frequency SHCP or STCP	$C_L = 50$ pF; see Figure 9 and Figure 10	80	-	-	MHz
$T_{amb} = -40$ °C to $+125$ °C						
t_{PLH}	LOW-to-HIGH propagation delay SHCP to Q7S	see Figure 9				
		$C_L = 15$ pF	1.7	-	7.8	ns
t_{PHL}	HIGH-to-LOW propagation delay SHCP to Q7S	$C_L = 50$ pF	2.2	-	9.9	ns
		see Figure 9				
t_{PLH}	LOW-to-HIGH propagation delay STCP to Qn	$C_L = 15$ pF	1.8	-	8.3	ns
		$C_L = 50$ pF	2.4	-	11.0	ns
t_{PHL}	HIGH-to-LOW propagation delay STCP to Qn	see Figure 10				
		$C_L = 15$ pF	1.9	-	7.2	ns
t_{PHL}	HIGH-to-LOW propagation delay SHR to Q7S	$C_L = 50$ pF	2.6	-	10.5	ns
		see Figure 10				
t_{PHL}	HIGH-to-LOW propagation delay STR to Qn	$C_L = 15$ pF	2.4	-	8.7	ns
		$C_L = 50$ pF	2.7	-	11.0	ns
t_{PHL}	HIGH-to-LOW propagation delay STR to Qn	see Figure 13				
		$C_L = 15$ pF	2.3	-	9.2	ns
t_{PHL}	HIGH-to-LOW propagation delay STR to Qn	$C_L = 50$ pF	3.1	-	11.7	ns
		see Figure 14				
t_w	pulse width HIGH or LOW SHCP and STCP	$C_L = 50$ pF; see Figure 9 and Figure 10	6.5	-	-	ns
		$C_L = 50$ pF; see Figure 13 and Figure 14	6.0	-	-	ns
t_{su}	set-up time DS to SHCP	$C_L = 50$ pF; see Figure 11	3.5	-	-	ns
	set-up time SHR to STCP	$C_L = 50$ pF; see Figure 12	5.5	-	-	ns
	set-up time SHCP to STCP	$C_L = 50$ pF; see Figure 10	5.5	-	-	ns
t_h	hold time DS to SHCP	see Figure 11	2.5	-	-	ns

Table 9. Dynamic characteristics type 74AHCT594 ...continued
GND = 0 V; $t_r = t_f \leq 3.0$ ns; $V_{CC} = 4.5$ V to 5.5 V; see Figure 15

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{rec}	recovery time SHR to SHCP	$C_L = 50$ pF; see Figure 13	3.8	-	-	ns
	recovery time STR to STCP	$C_L = 50$ pF; see Figure 14	4.3	-	-	ns
f_{max}	maximum frequency SHCP or STCP	$C_L = 50$ pF; see Figure 9 and Figure 10	70	-	-	MHz

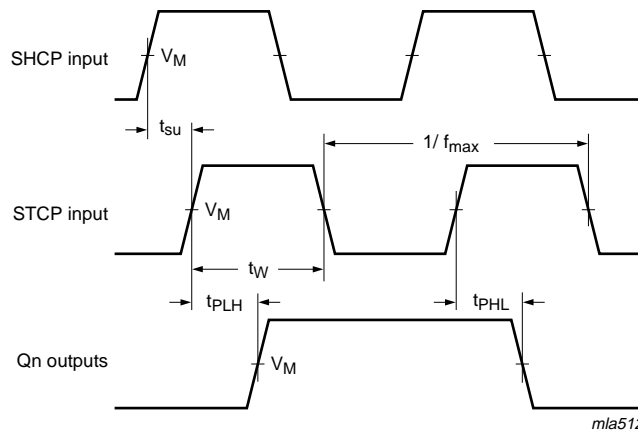
- [1] Typical values are measured at $V_{CC} = 5.0$ V.
- [2] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

12. Waveforms



Measurement points are given in Table 10.
 V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

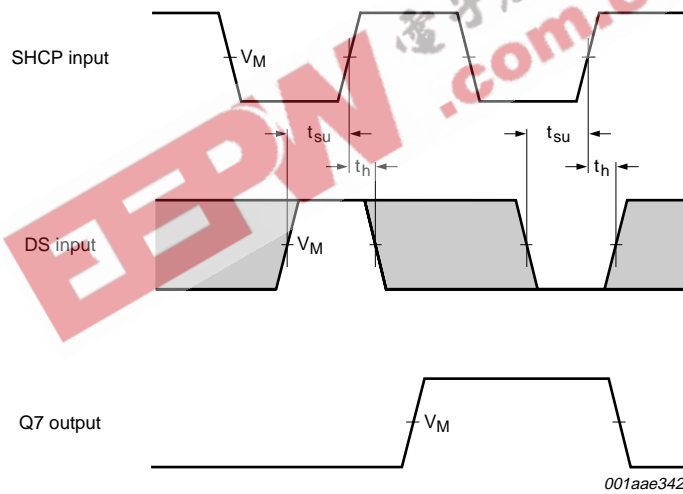
Fig 9. The shift clock (SHCP) to output (Q7S) propagation delays, the shift clock pulse width, and the maximum shift clock frequency



Measurement points are given in [Table 10](#).

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 10. The storage clock (STCP) to output (Qn), propagation delays, the storage clock pulse width, the maximum storage clock pulse frequency and the shift clock to storage clock set-up time

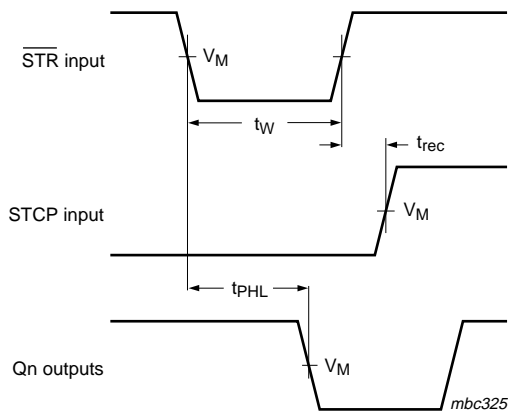


Measurement points are given in [Table 10](#).

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

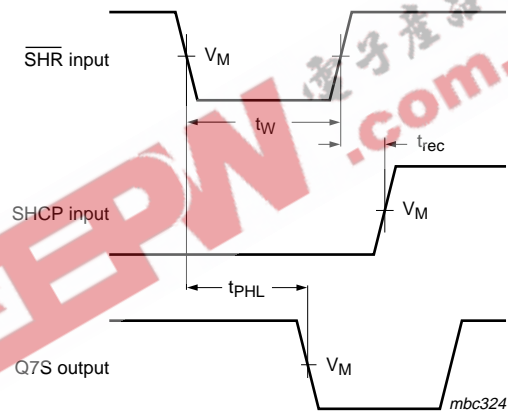
Fig 11. The data set-up time and hold times for DS input to SHCP



Measurement points are given in [Table 10](#).

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

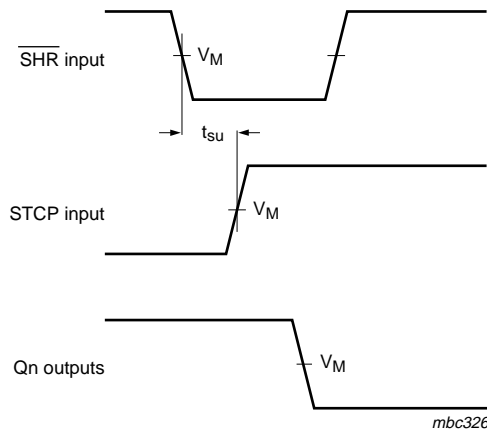
Fig 12. The set-up time shift reset ($\overline{\text{STR}}$) to storage clock (STCP)



Measurement points are given in [Table 10](#).

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 13. The shift reset ($\overline{\text{SHR}}$) pulse width, the shift reset to output (Q7S) propagation delay and the shift reset to shift clock (SHCP) recovery time



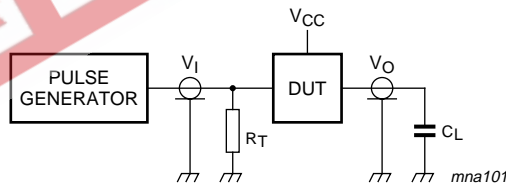
Measurement points are given in [Table 10](#).

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 14. The storage reset (\overline{STR}) pulse width, the storage reset to output (Q_n) propagation delay and the storage reset to storage clock (STCP) recovery time

Table 10. Measurement points

Type	Input		Output
	V_M		V_M
74AHC594	$0.5 \times V_{CC}$		$0.5 \times V_{CC}$
74AHCT594	1.5 V		$0.5 \times V_{CC}$



For test data see [Table 11](#).

Definitions for test circuit:

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig 15. Load circuitry for switching times

Table 11. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74AHC594	V_{CC}	≤ 3.0 ns	50 pF, 15 pF	t_{PLH}, t_{PHL}
74AHCT594	3.0 V	≤ 3.0 ns	50 pF, 15 pF	t_{PLH}, t_{PHL}

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

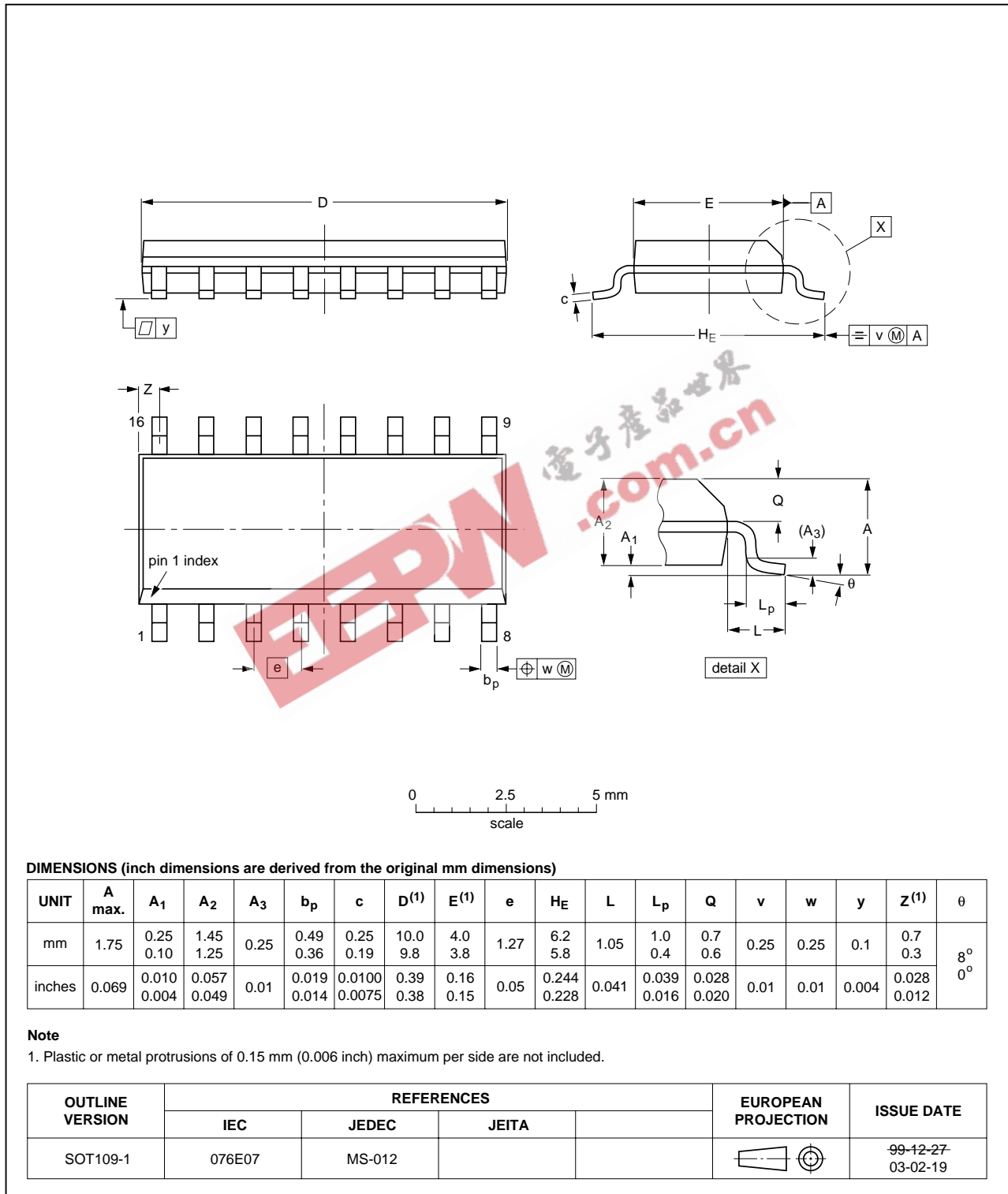


Fig 16. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

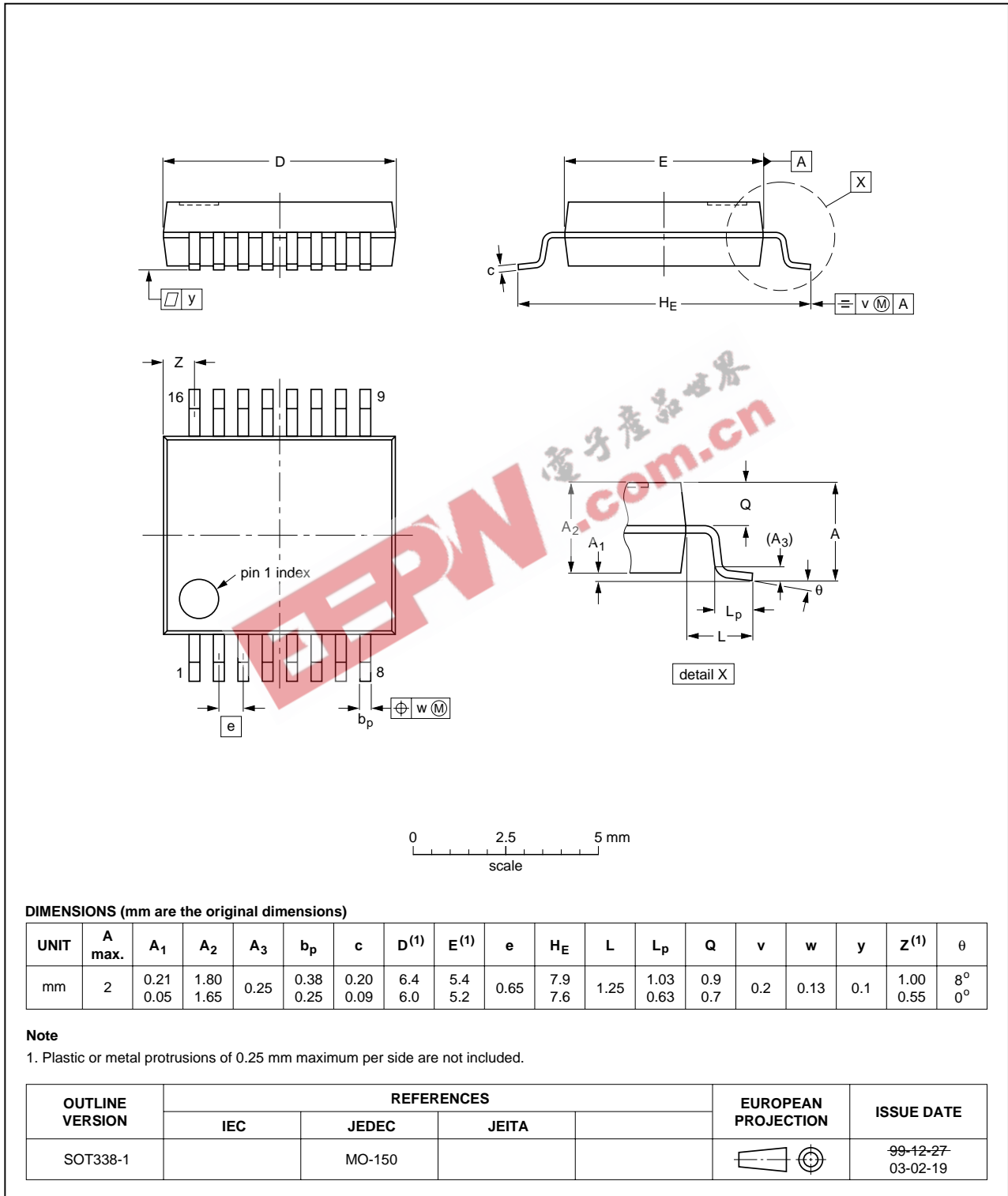


Fig 17. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

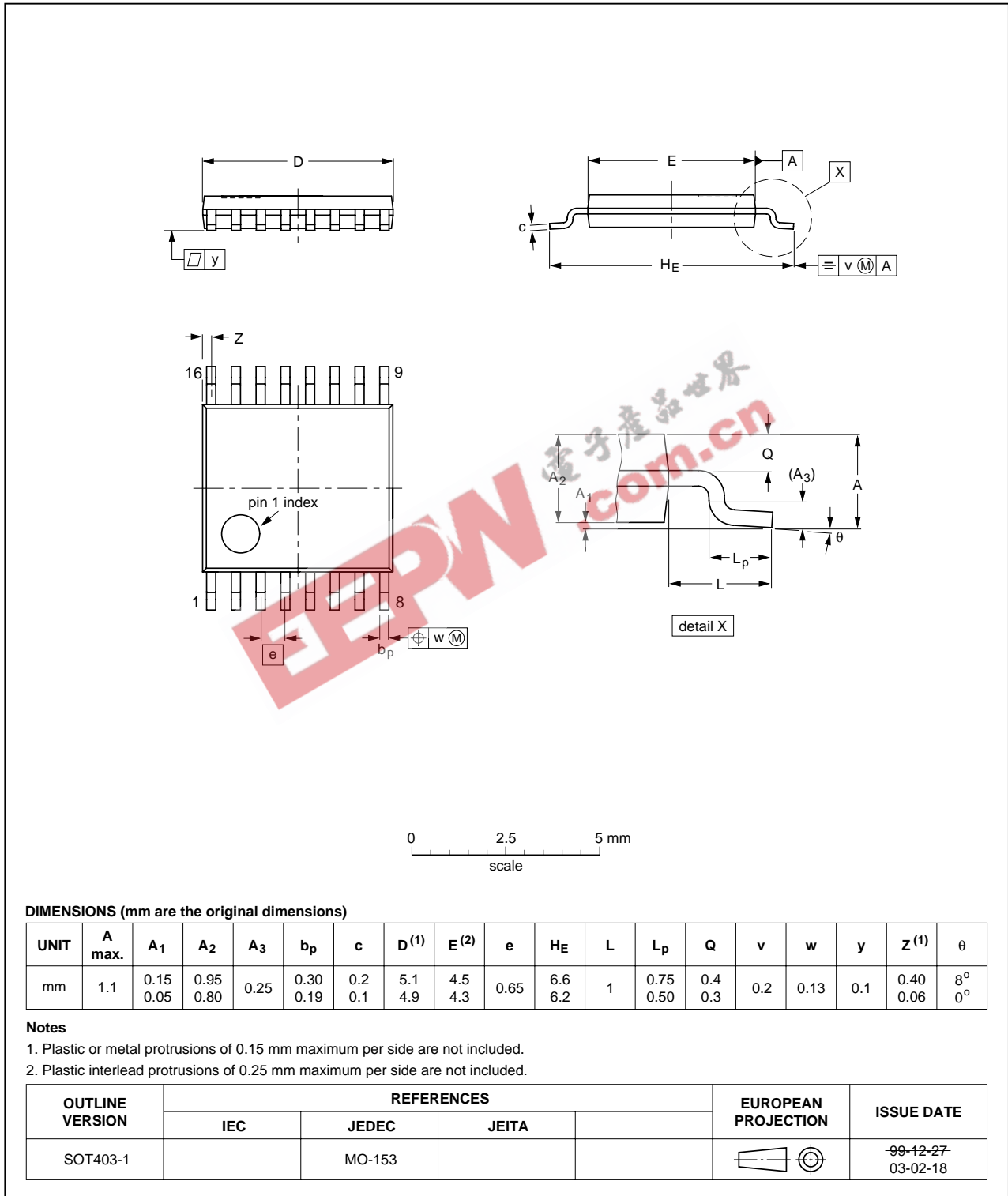


Fig 18. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

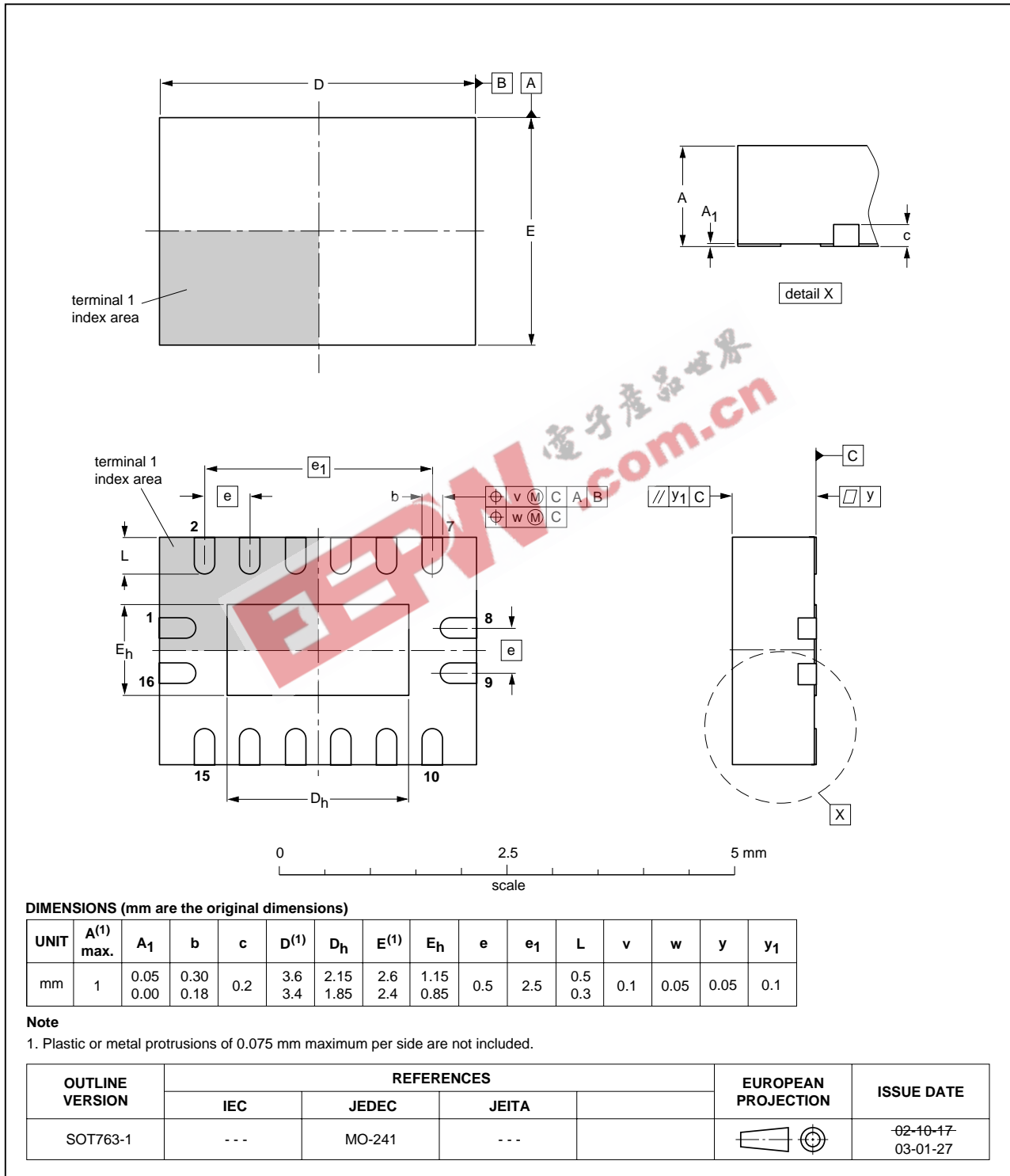


Fig 19. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
HBM	Human Body Model
ESD	ElectroStatic Discharge
MM	Machine Model
DUT	Device Under Test

15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT594_1	20060704	Product data sheet	-	-

EEPW 电子产品世界
.com.cn

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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