FAIRCHILD SEMICONDUCTOR™

March 1992
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74FR74 • 74FR1074
Dual D-Type Flip-Flop

General Description

The 74FR74 and 74FR1074 are dual D-type flip-flops with true and complement (Q/$\overline{Q}$) outputs. On the 74FR74, data at the D inputs is transferred to the outputs on the rising edge of the clock input (CP_n). The 74FR1074 is the negative edge triggered version of this device. Both parts feature asynchronous clear (C_{Dn}) and set (S_{Dn}) inputs which are low level enabled.

Features

- 74FR74 is pin-for-pin compatible with the 74F74
- True 150 MHz f_{MAX} capability on 74FR74
- Outputs sink 24 mA and source 24 mA
- Guaranteed pin-to-pin skew specifications

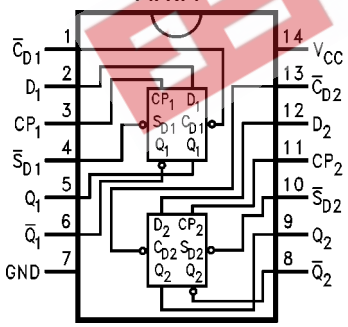
Ordering Code:

Order Number	Package Number	Package Description
74FR74SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74FR74PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74FR1074SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74FR1074PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

74FR74



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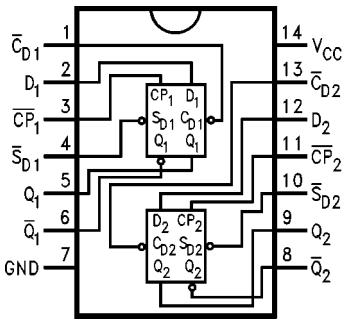
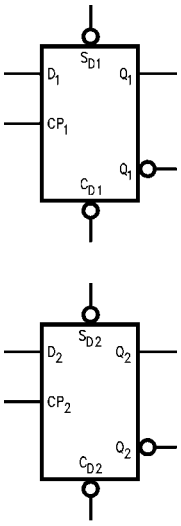


Logic Symbols

74FR74



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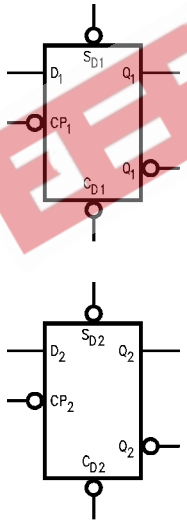


Pin Descriptions

Pin Names	Description
D_n	Data Inputs
CP_n	Clock Inputs
S_{Dn}	Asynchronous Set Inputs
C_{Dn}	Asynchronous Clear Inputs
Q_n	True Output
$\overline{Q}_n$	Complementary Output

Truth Tables

74FR74

Inputs				Outputs	
$\overline{SD}$	$\overline{CD}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	⌐	H	H	L
H	H	⌐	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
⌐ = Rising Edge
Q_0 = Previous Q($\overline{Q}$) before LOW-to-HIGH Clock Transition

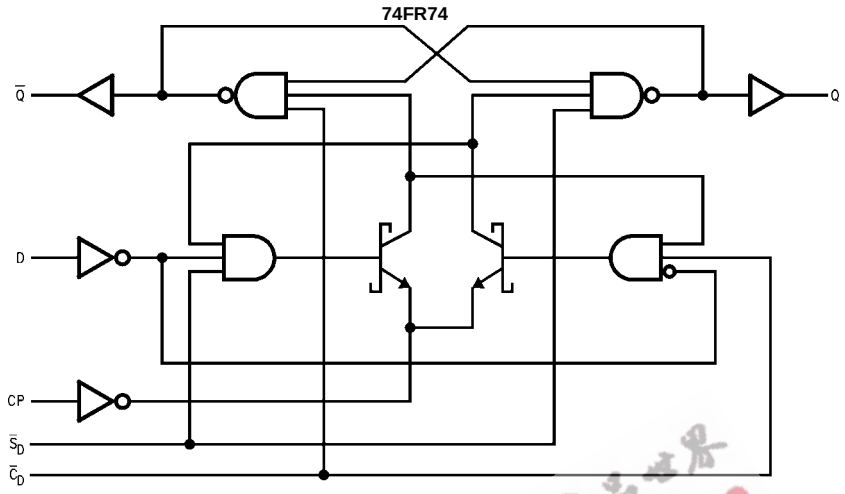
74FR1074

Inputs				Outputs	
$\overline{SD}$	$\overline{CD}$	$\overline{CP}$	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	⌙	H	H	L
H	H	⌙	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
⌙ = Falling Edge
Q_0 = Previous Q($\overline{Q}$) before HIGH-to-LOW Clock Transition

Logic Diagrams

74FR74



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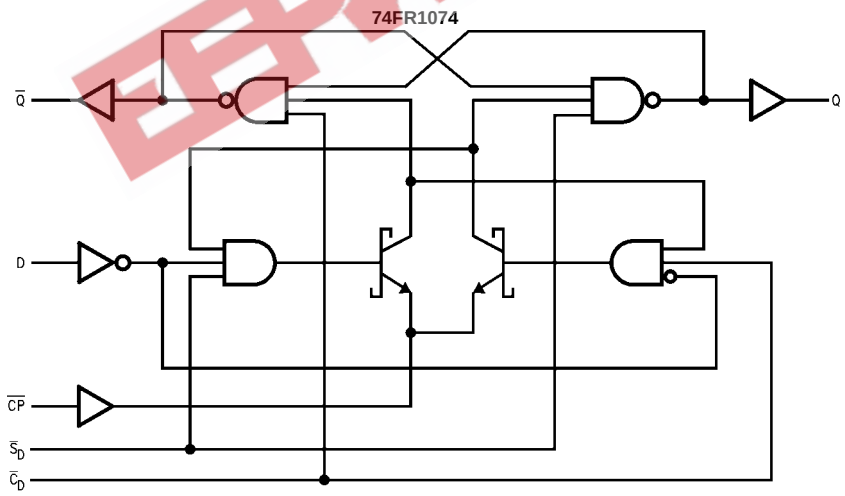


Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	2000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.5			V	Min	I_{OH} = −1 mA
		2.4			V	Min	I_{OH} = −3 mA
		2.0			V	Min	I_{OH} = −24 mA
V_{OL}	Output LOW Voltage			0.5	V	Min	I_{OL} = 24 mA
I_{IH}	Input HIGH Current			5	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7	µA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current			−150	µA	Max	V_{IN} = 0.5V (D_n, CP_n)
				−1.8	mA	Max	V_{IN} = 0.5V (C_{Dn}, S_{Dn})
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 µA, All Other Pins Grounded
I_{OD}	Output Circuit Leakage Test			3.75	V	0.0	V_{IOD} = 150 mV, All Other Pins Grounded
I_{OS}	Output Short-Circuit Current	−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output HIGH Leakage Current			50	µA	Max	V_{OUT} = V_{CC}
I_{CC}	Power Supply Current			24	mA	Max	

AC Electrical Characteristics 74FR74

Symbol	Parameter	$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	150	190		150		MHz
t_{PLH} t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	2.5 2.5	3.5 4.5	5.0 6.0	2.5 2.5	5.0 6.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	1.5 2.0	3.5 5.5	5.5 7.0	1.5 2.0	5.5 7.0	ns
t_{OSHL} (Note 3)	Pin to Pin Skew for HL Transitions					1.0	ns
t_{OSLH} (Note 3)	Pin to Pin Skew for LH Transitions					1.0	ns
t_{OST} (Note 3)	Pin to Pin Skew for HL/LH Transitions					3.0	ns
$t_{Q/\overline{Q}}$ (Note 3)	True/Complement Output Skew					1.8	ns
t_{PS} (Note 3)	Pin (Signal) Transition Variation					1.8	ns

Note 3: Pin-to-Pin Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). t_{OST} is guaranteed by design.

AC Operating Requirements 74FR74

Symbol	Parameter	$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		Units
		Min	Max	Min	Max	
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW D_n to CP_n	2.5 2.5		2.5 2.5		ns
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW D_n to CP_n	0 0		0 0		ns
$t_W(H)$ $t_W(L)$ (Note 4)	CP_n Pulse Width HIGH or LOW	3.3 3.3		3.3 3.3		ns
$t_W(L)$	$\overline{S}_{Dn}$ or $\overline{C}_{Dn}$ Pulse Width	4.0		4.0		ns
t_{REC}	Recovery Time $\overline{S}_{Dn}$ or $\overline{C}_{Dn}$ to CP_n	2.0		2.0		ns

Note 4: This specification is guaranteed by design.

AC Electrical Characteristics 74FR1074

Symbol	Parameter	$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	120	160		120		MHz
t_{PLH} t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	2.5 3.0	4.0 5.0	5.5 6.5	2.5 3.0	5.5 6.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	1.5 2.0	3.5 5.5	5.5 7.0	1.5 2.0	5.5 7.0	ns
t_{OSHL} (Note 5)	Pin to Pin Skew for HL Transitions					1.5	ns
t_{OSLH} (Note 5)	Pin to Pin Skew for LH Transitions					1.5	ns
t_{OST} (Note 5)	Pin to Pin Skew for HL/LH Transitions					3.5	ns
$t_{Q/\overline{Q}}$ (Note 5)	True/Complement Output Skew					2.0	ns
t_{PS} (Note 5)	Pin (Signal) Transition Variation					2.0	ns

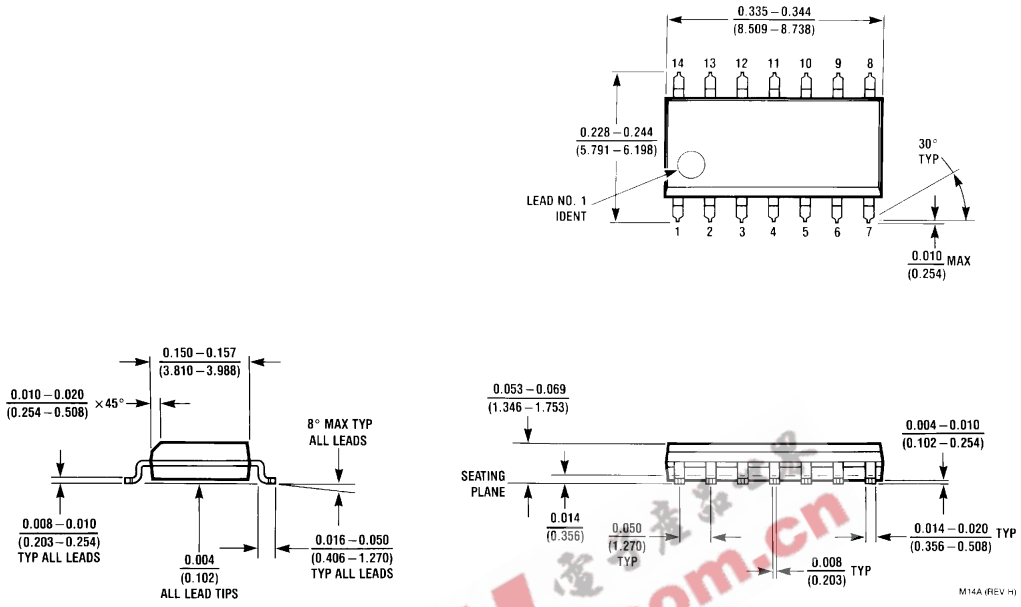
Note 5: Pin-to-Pin Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). t_{OST} is guaranteed by design.

AC Operating Requirements 74FR1074

Symbol	Parameter	$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		$T_A = 0°C = +70°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		Units
		Min	Max	Min	Max	
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW D_n to CP_n	2.0 2.0		2.0 2.0		ns
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW D_n to CP_n	0 0		0 0		ns
$t_W(H)$ $t_W(L)$ (Note 6)	$\overline{CP}_n$ Pulse Width HIGH or LOW	3.3 3.3		3.3 3.3		ns
$t_W(L)$	$\overline{S}_{Dn}$ or $\overline{C}_{Dn}$ Pulse Width	4.0		4.0		ns
t_{REC}	Recovery Time $\overline{S}_{Dn}$ or $\overline{C}_{Dn}$ to CP_n	2.0		2.0		ns

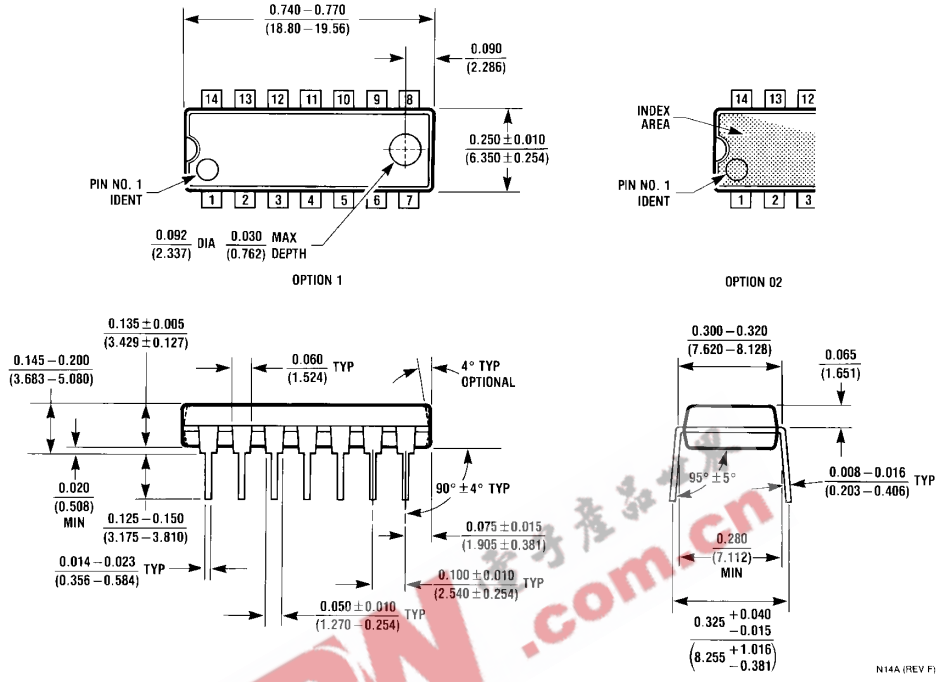
Note 6: This specification is guaranteed by design.

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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