FAIRCHILD

SEMICONDUCTOR TM

November 2001
Revised June 2002

74LCX32245

Low Voltage 32-Bit Bidirectional Transceiver with 5V Tolerant Inputs and Outputs

General Description

The LCX32245 contains thirty-two non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The device is byte controlled. Each byte has separate control inputs which could be shorted together for full 32-bit operation. The $T/\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

The LCX32245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

■ 5V tolerant inputs and outputs

■ 2.3V–3.6V V_{CC} specifications provided

■ 4.5 ns t_{PD} max (V_{CC} = 3.3V), 20 μA I_{CC} max

■ Power down high impedance inputs and outputs

■ Supports live insertion/withdrawal (Note 1)

■ ±24 mA output drive (V_{CC} = 3.0V)

■ Uses patented noise/EMI reduction circuitry

■ Latch-up performance exceeds 500 mA

■ ESD performance:
   Human body model > 2000V
   Machine model > 200V

■ Packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

Note 1: To ensure the high-impedance state during power up or down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.
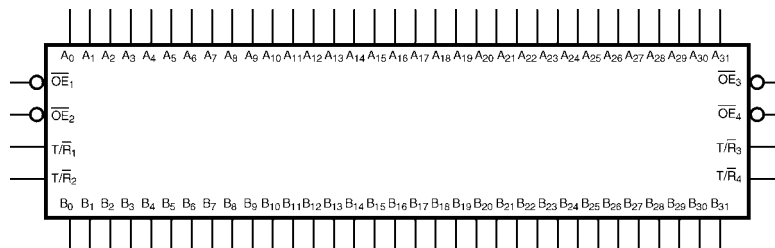
Ordering Code:

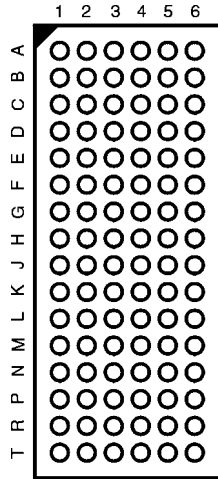| Order Number	Package Number	Package Description
74LCX32245G (Note 2)(Note 3)	BGA96A	96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide

Note 2: Ordering code "G" indicates Trays.

Note 3: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol

74LCX32245

Connection Diagram

(Top Thru View)

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$T/\overline{R}_n$	Transmit/Receive Input
A_0–A_{31}	Side A Inputs or 3-STATE Outputs
B_0–B_{31}	Side B Inputs or 3-STATE Outputs

FBGA Pin Assignments

	1	2	3	4	5	6
A	B_1	B_0	$T/\overline{R}_1$	$\overline{OE}_1$	A_0	A_1
B	B_3	B_2	GND	GND	A_2	A_3
C	B_5	B_4	V_{CC}	V_{CC}	A_4	A_5
D	B_7	B_6	GND	GND	A_6	A_7
E	B_9	B_8	GND	GND	A_8	A_9
F	B_{11}	B_{10}	V_{CC}	V_{CC}	A_{10}	A_{11}
G	B_{13}	B_{12}	GND	GND	A_{12}	A_{13}
H	B_{14}	B_{15}	$T/\overline{R}_2$	$\overline{OE}_2$	A_{15}	A_{14}
J	B_{17}	B_{16}	$T/\overline{R}_3$	$\overline{OE}_3$	A_{16}	A_{17}
K	B_{19}	B_{18}	GND	GND	A_{18}	A_{19}
L	B_{21}	B_{20}	V_{CC}	V_{CC}	A_{20}	A_{21}
M	B_{23}	B_{22}	GND	GND	A_{22}	A_{23}
N	B_{25}	B_{24}	GND	GND	A_{24}	A_{25}
P	B_{27}	B_{26}	V_{CC}	V_{CC}	A_{26}	A_{27}
R	B_{29}	B_{28}	GND	GND	A_{28}	A_{29}
T	B_{30}	B_{31}	$T/\overline{R}_4$	$\overline{OE}_4$	A_{31}	A_{30}

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH Z State on A_0–A_7, B_0–B_7

Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH Z State on A_8–A_{15}, B_8–B_{15}

Inputs		Outputs
$\overline{OE}_3$	$T/\overline{R}_3$	
L	L	Bus B_{16}–B_{23} Data to Bus A_{16}–A_{23}
L	H	Bus A_{16}–A_{23} Data to Bus B_{16}–B_{23}
H	X	HIGH Z State on A_{16}–A_{23}, B_{16}–B_{23}

Inputs		Outputs
$\overline{OE}_4$	$T/\overline{R}_4$	
L	L	Bus B_{24}–B_{31} Data to Bus A_{24}–A_{31}
L	H	Bus A_{24}–A_{31} Data to Bus B_{24}–B_{31}
H	X	HIGH Z State on A_{24}–A_{31}, B_{24}–B_{31}

H = HIGH Voltage Level
L = LOW Voltage Level

X = Immaterial (HIGH or LOW, inputs and I/O's may not float)
Z = High Impedance

Logic Diagrams

Absolute Maximum Ratings(Note 4)

Symbol	Parameter	Value	Conditions	Units
V$_{CC}$	Supply Voltage	−0.5 to +7.0		V
V$_I$	DC Input Voltage	−0.5 to +7.0		V
V$_O$	DC Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to V$_{CC}$ + 0.5	Output in HIGH or LOW State (Note 5)	
I$_{IK}$	DC Input Diode Current	−50	V$_I$ < GND	mA
I$_{OK}$	DC Output Diode Current	−50	V$_O$ < GND	mA
		+50	V$_O$ > V$_{CC}$	
I$_O$	DC Output Source/Sink Current	±50		mA
I$_{CC}$	DC Supply Current per Supply Pin	±100		mA
I$_{GND}$	DC Ground Current per Ground Pin	±100		mA
T$_{STG}$	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions (Note 6)

Symbol	Parameter		Min	Max	Units
V$_{CC}$	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V$_I$	Input Voltage		0	5.5	V
V$_O$	Output Voltage	HIGH or LOW State	0	V$_{CC}$	V
		3-STATE	0	5.5	
I$_{OH}$/I$_{OL}$	Output Current	V$_{CC}$ = 3.0V – 3.6V		±24	mA
		V$_{CC}$ = 2.7V – 3.0V		±12	
		V$_{CC}$ = 2.3V – 2.7V		±8	
T$_A$	Free-Air Operating Temperature		−40	85	°C
Δt/ΔV	Input Edge Rate, V$_{IN}$ = 0.8V–2.0V, V$_{CC}$ = 3.0V		0	10	ns/V

Note 4: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 5: I$_O$ Absolute Maximum Rating must be observed.

Note 6: Unused inputs or I/O's must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V$_{CC}$ (V)	T$_A$ = −40°C to +85°C		Units
				Min	Max	
V$_{IH}$	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		
V$_{IL}$	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	
V$_{OH}$	HIGH Level Output Voltage	I$_{OH}$ = −100 μA	2.3 – 3.6	V$_{CC}$ – 0.2		V
		I$_{OH}$ = −8 mA	2.3	1.8		
		I$_{OH}$ = −12 mA	2.7	2.2		
		I$_{OH}$ = −18 mA	3.0	2.4		
		I$_{OH}$ = −24 mA	3.0	2.2		
V$_{OL}$	LOW Level Output Voltage	I$_{OL}$ = 100 μA	2.3 – 3.6		0.2	V
		I$_{OL}$ = 8mA	2.3		0.6	
		I$_{OL}$ = 12 mA	2.7		0.4	
		I$_{OL}$ = 16 mA	3.0		0.4	
		I$_{OL}$ = 24 mA	3.0		0.55	
I$_I$	Input Leakage Current	0 ≤ V$_I$ ≤ 5.5V	2.3 – 3.6		±5.0	μA
I$_{OZ}$	3-STATE I/O Leakage	0 ≤ V$_O$ ≤ 5.5V	2.3 – 3.6		±5.0	μA
		V$_I$ = V$_{IH}$ or V$_{IL}$				
I$_{OFF}$	Power-Off Leakage Current	V$_I$ or V$_O$ = 5.5V	0		10	μA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_CC (V)	T_A = −40°C to +85°C		Units
				Min	Max	
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3–3.6		20	μA
		$3.6V \leq V_I$, $V_O \leq 5.5V$ (Note 7)	2.3–3.6		±20	
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.3–3.6		500	μA

Note 7: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	T_A = −40°C to +85°C, R_L = 500Ω						Units
		V_CC = 3.3V ± 0.3V		V_CC = 2.7V		V_CC = 2.5V ± 0.2V		
		C_L = 50 pF		C_L = 50 pF		C_L = 30 pF		
		Min	Max	Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.5	4.5	1.5	5.2	1.5	5.4	ns
t_{PLH}	A_n to B_n or B_n to A_n	1.5	4.5	1.5	5.2	1.5	5.4	
t_{PZL}	Output Enable Time	1.5	6.5	1.5	7.2	1.5	8.5	ns
t_{PZH}		1.5	6.5	1.5	7.2	1.5	8.5	
t_{PLZ}	Output Disable Time	1.5	6.4	1.5	6.9	1.5	7.7	ns
t_{PHZ}		1.5	6.4	1.5	6.9	1.5	7.7	

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_CC (V)	T_A = 25°C	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	−0.8	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	−0.6	

Capacitance

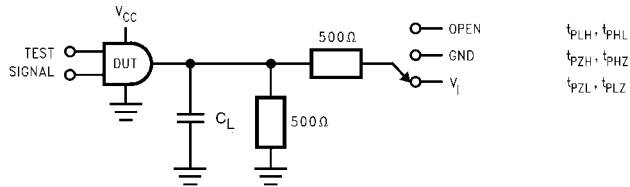| Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, f = 10 MHz	20	pF

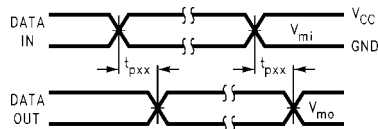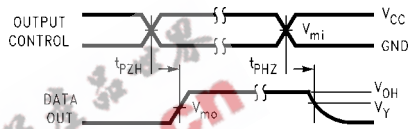# AC LOADING and WAVEFORMS Generic for LCX Family

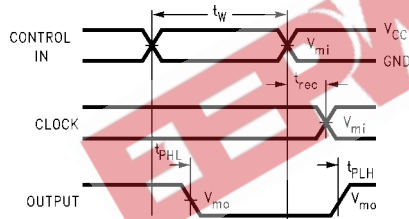FIGURE 1. AC Test Circuit (C$_L$ includes probe and jig capacitance)

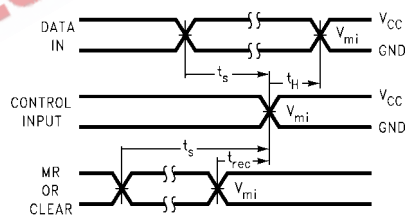| Test	Switch
t$_{PLH}$, t$_{PHL}$	Open
t$_{PZL}$, t$_{PLZ}$	6V at V$_{CC}$ = 3.3 ± 0.3V, and 2.7V V$_{CC}$ x 2 at V$_{CC}$ = 2.5 ± 0.2V
t$_{PZH}$, t$_{PHZ}$	GND

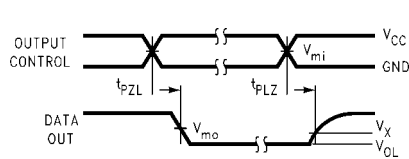Waveform for Inverting and Non-Inverting Functions

3-STATE Output High Enable and
Disable Times for Logic

Propagation Delay. Pulse Width and t$_{rec}$ Waveforms

Setup Time, Hold Time and Recovery Time for Logic

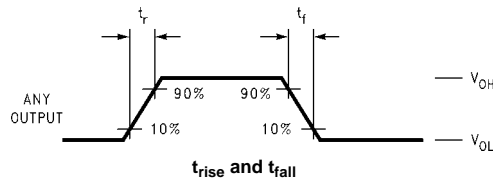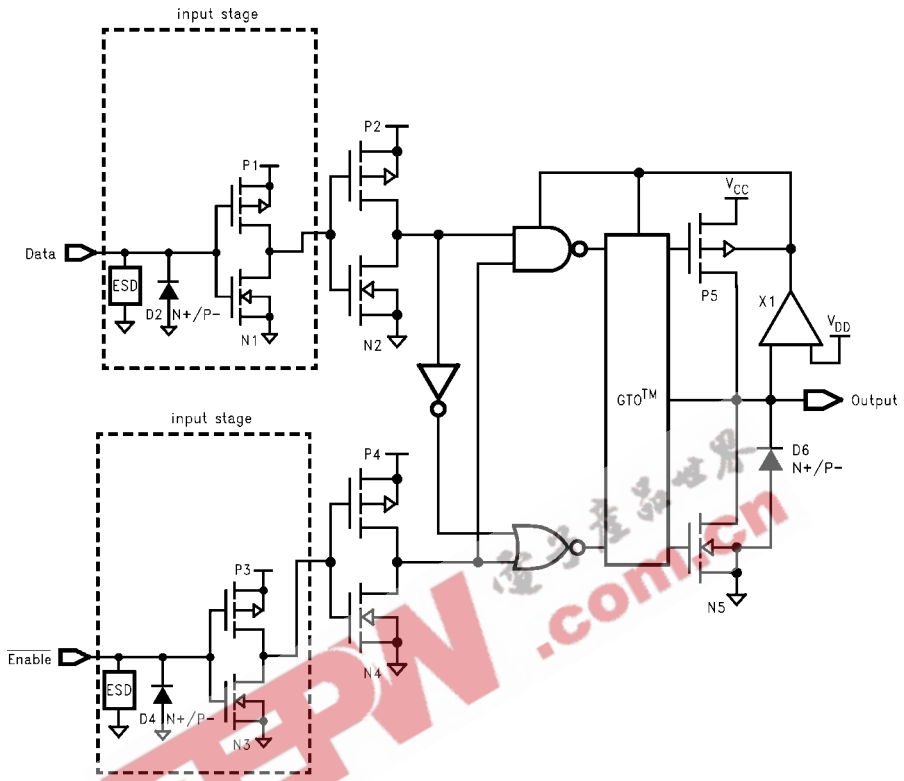3-STATE Output Low Enable and
Disable Times for Logic

t$_{rise}$ and t$_{fall}$

FIGURE 2. Waveforms
(Input Characteristics; f =1MHz, t$_r$ = t$_f$ = 3ns)

Symbol	V$_{CC}$		
	3.3V ± 0.3V	2.7V	2.5V ± 0.2V
V$_{mi}$	1.5V	1.5V	V$_{CC}$/2
V$_{mo}$	1.5V	1.5V	V$_{CC}$/2
V$_x$	V$_{OL}$ + 0.3V	V$_{OL}$ + 0.3V	V$_{OL}$ + 0.15V
V$_y$	V$_{OH}$ − 0.3V	V$_{OH}$ − 0.3V	V$_{OH}$ − 0.15V

Schematic Diagram Generic for LCX Family

Physical Dimensions inches (millimeters) unless otherwise noted

BGA96ArevE

**96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA96A**

NOTES:
A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined) .35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

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