MOTOROLA

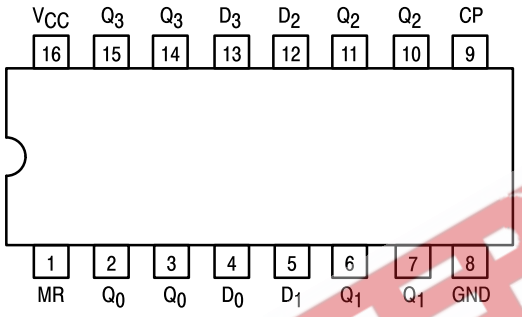
# QUAD D FLIP-FLOP

The LSTTL/MSI SN54/74LS175 is a high speed Quad D Flip-Flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW to HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

The LS175 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Edge-Triggered D-Type Inputs
- Buffered-Positive Edge-Triggered Clock
- Clock to Output Delays of 30 ns
- Asynchronous Common Reset
- True and Complement Output
- Input Clamp Diodes Limit High Speed Termination Effects

**CONNECTION DIAGRAM DIP** (TOP VIEW)



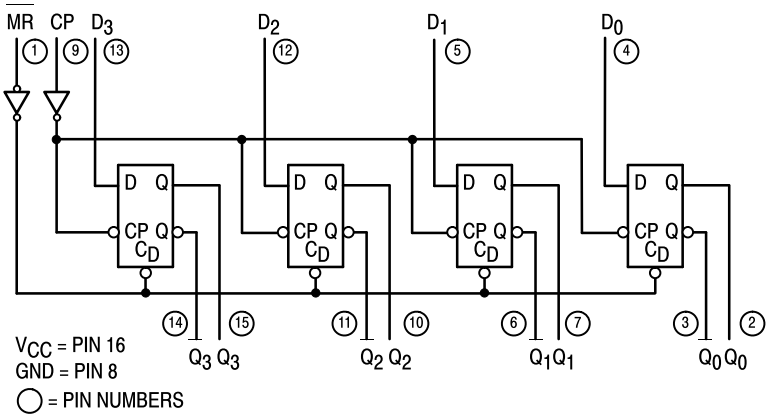

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

**PIN NAMES**

| | | LOADING (Note a) HIGH | LOW |
|---|---|---|---|
| $D_0-D_3$ | Data Inputs | 0.5 U.L. | 0.25 U.L. |
| $\overline{CP}$ | Clock (Active HIGH Going Edge) Input | 0.5 U.L. | 0.25 U.L. |
| MR | Master Reset (Active LOW) Input | 0.5 U.L. | 0.25 U.L. |
| $\overline{Q_0}-\overline{Q_3}$ | True Outputs (Note b) | 10 U.L. | 5 (2.5) U.L. |
| $Q_0-Q_3$ | Complemented Outputs (Note b) | 10 U.L. | 5 (2.5) U.L. |

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

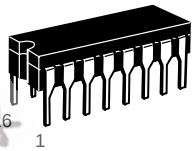
**LOGIC DIAGRAM**



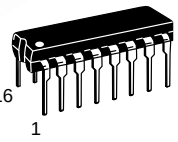

## SN54/74LS175

**QUAD D FLIP-FLOP**

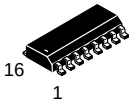
**LOW POWER SCHOTTKY**




**J SUFFIX**
CERAMIC
CASE 620-09




**N SUFFIX**
PLASTIC
CASE 648-08

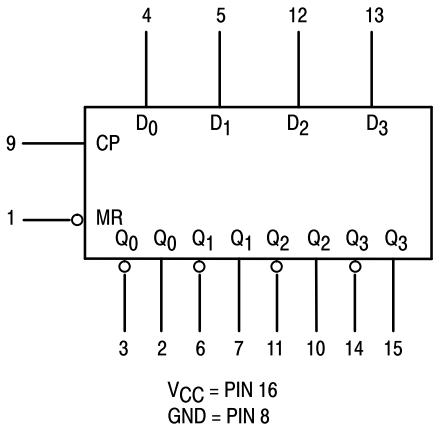



**D SUFFIX**
SOIC
CASE 751B-03

**ORDERING INFORMATION**

| | |
|---|---|
| SN54LSXXXJ | Ceramic |
| SN74LSXXXN | Plastic |
| SN74LSXXXD | SOIC |

**LOGIC SYMBOL**



## FUNCTIONAL DESCRIPTION

The LS175 consists of four edge-triggered D flip-flops with individual D inputs and Q and Q outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW to HIGH Clock (CP) transition, causing individual Q and Q outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and Q outputs HIGH independent of Clock or Data inputs.

The LS175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

### TRUTH TABLE

| Inputs (t = n, $\overline{MR}$ = H) | Outputs (t = n+1) Note 1 | |
|---|---|---|
| D | Q | $\overline{Q}$ |
| L | L | H |
| H | H | L |

Note 1: t = n + 1 indicates conditions after next clock.

### GUARANTEED OPERATING RANGES

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 54<br>74 | 4.5<br>4.75 | 5.0<br>5.0 | 5.5<br>5.25 | V |
| $T_A$ | Operating Ambient Temperature Range | 54<br>74 | −55<br>0 | 25<br>25 | 125<br>70 | °C |
| $I_{OH}$ | Output Current — High | 54, 74 | | | −0.4 | mA |
| $I_{OL}$ | Output Current — Low | 54<br>74 | | | 4.0<br>8.0 | mA |

### DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol | Parameter | | Limits Min | Limits Typ | Limits Max | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V | Guaranteed Input HIGH Voltage for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | 54 | | | 0.7 | V | Guaranteed Input LOW Voltage for All Inputs | |
| | | 74 | | | 0.8 | | | |
| $V_{IK}$ | Input Clamp Diode Voltage | | | −0.65 | −1.5 | V | $V_{CC}$ = MIN, $I_{IN}$ = −18 mA | |
| $V_{OH}$ | Output HIGH Voltage | 54 | 2.5 | 3.5 | | V | $V_{CC}$ = MIN, $I_{OH}$ = MAX, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ per Truth Table | |
| | | 74 | 2.7 | 3.5 | | V | | |
| $V_{OL}$ | Output LOW Voltage | 54, 74 | | 0.25 | 0.4 | V | $I_{OL}$ = 4.0 mA | $V_{CC}$ = $V_{CC}$ MIN, $V_{IN}$ = $V_{IL}$ or $V_{IH}$ per Truth Table |
| | | 74 | | 0.35 | 0.5 | V | $I_{OL}$ = 8.0 mA | |
| $I_{IH}$ | Input HIGH Current | | | | 20 | μA | $V_{CC}$ = MAX, $V_{IN}$ = 2.7 V | |
| | | | | | 0.1 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 7.0 V | |
| $I_{IL}$ | Input LOW Current | | | | −0.4 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 0.4 V | |
| $I_{OS}$ | Short Circuit Current (Note 1) | | −20 | | −100 | mA | $V_{CC}$ = MAX | |
| $I_{CC}$ | Power Supply Current | | | | 18 | mA | $V_{CC}$ = MAX | |

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

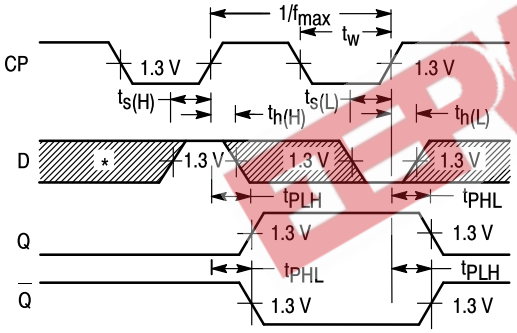
**AC CHARACTERISTICS** ($T_A$ = 25°C)

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| $f_{MAX}$ | Maximum Input Clock Frequency | 30 | 40 | | MHz | $V_{CC}$ = 5.0 V<br>$C_L$ = 15 pF |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay, $\overline{MR}$ to Output | | 20<br>20 | 30<br>30 | ns | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay, Clock to Output | | 13<br>16 | 25<br>25 | ns | |

**AC SETUP REQUIREMENTS** ($T_A$ = 25°C)

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| $t_W$ | Clock or $\overline{MR}$ Pulse Width | 20 | | | ns | $V_{CC}$ = 5.0 V |
| $t_s$ | Data Setup Time | 20 | | | ns | |
| $t_h$ | Data Hold Time | 5.0 | | | ns | |
| $t_{rec}$ | Recovery Time | 25 | | | ns | |

**AC WAVEFORMS**




*The shaded areas indicate when the input is permitted to change for predictable output performance.

**Figure 1. Clock to Output Delays, Clock Pulse Width, Frequency, Setup and Hold Times Data to Clock**

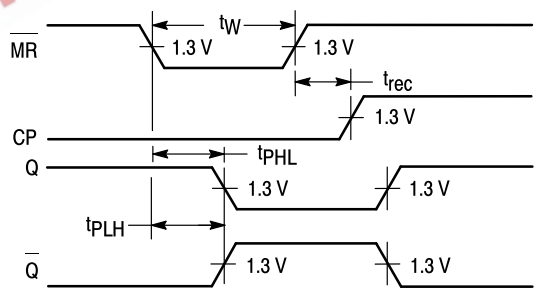



**Figure 2. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time**

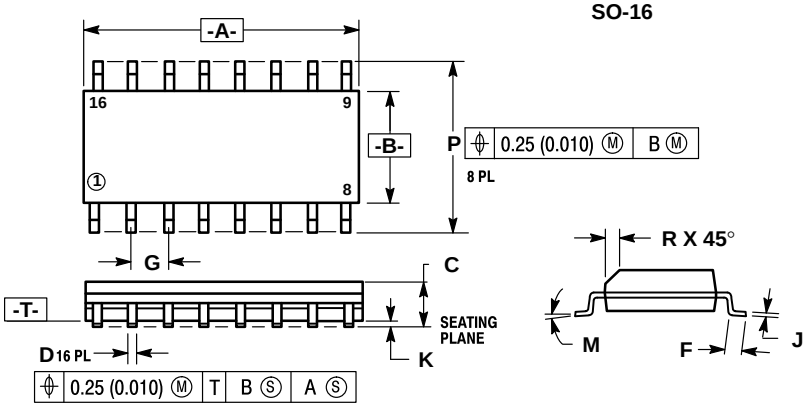
**DEFINITIONS OF TERMS**

SETUP TIME ($t_s$) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME ($t_h$) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME ($t_{rec}$) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

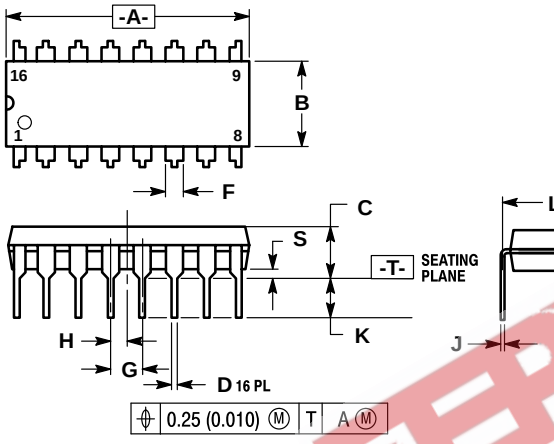
## Case 751B-03 D Suffix
## 16-Pin Plastic
## SO-16




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. 751B-01 IS OBSOLETE, NEW STANDARD 751B-03.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

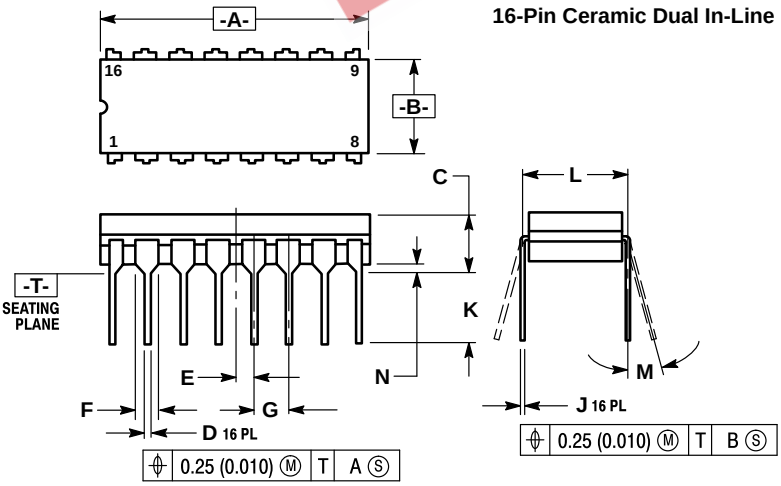
## Case 648-08 N Suffix
## 16-Pin Plastic




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.
6. 648-01 THRU -07 OBSOLETE, NEW STANDARD 648-08.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 18.80 | 19.55 | 0.740 | 0.770 |
| B | 6.35 | 6.85 | 0.250 | 0.270 |
| C | 3.69 | 4.44 | 0.145 | 0.175 |
| D | 0.39 | 0.53 | 0.015 | 0.021 |
| F | 1.02 | 1.77 | 0.040 | 0.070 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 1.27 BSC | | 0.050 BSC | |
| J | 0.21 | 0.38 | 0.008 | 0.015 |
| K | 2.80 | 3.30 | 0.110 | 0.130 |
| L | 7.50 | 7.74 | 0.295 | 0.305 |
| M | 0° | 10° | 0° | 10° |
| S | 0.51 | 1.01 | 0.020 | 0.040 |

## Case 620-09 J Suffix
## 16-Pin Ceramic Dual In-Line




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
5. 620-01 THRU -08 OBSOLETE, NEW STANDARD 620-09.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 19.05 | 19.55 | 0.750 | 0.770 |
| B | 6.10 | 7.36 | 0.240 | 0.290 |
| C | — | 4.19 | — | 0.165 |
| D | 0.39 | 0.53 | 0.015 | 0.021 |
| E | 1.27 BSC | | 0.050 BSC | |
| F | 1.40 | 1.77 | 0.055 | 0.070 |
| G | 2.54 BSC | | 0.100 BSC | |
| J | 0.23 | 0.27 | 0.009 | 0.011 |
| K | — | 5.08 | — | 0.200 |
| L | 7.62 BSC | | 0.300 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.39 | 0.88 | 0.015 | 0.035 |

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