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ACL Products	

# 74AC/ACT11898

## 10-bit serial-in parallel-out shift register

### FEATURES

- Gated serial data inputs
- Fully buffered clock and data inputs
- Fully synchronous data transfers
- Typical shift frequency of 100MHz
- Asynchronous master reset
- Output capability:  $\pm 24\text{mA}$
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50 $\Omega$  incident wave switching
- Center-pin  $V_{CC}$  and ground configuration to minimize high-speed switching noise
- $I_{CC}$  category: MSI

### DESCRIPTION

The 74AC/ACT11898 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11898 10-bit Serial-In Parallel-Out Shift Register is an edge-triggered shift register with serial data entry and an output from each of the 10 stages. Data is entered serially through one of two inputs (A • B); either input

(continued)

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V};$ $V_{CC} = 5.0\text{V}$	TYPICAL		UNIT
			AC	ACT	
$t_{PLH}/t_{PHL}$	Propagation delay CP to $Q_n$ ( $\overline{\text{MR}} = \text{High}$ )	$C_L = 50\text{pF}$	5.9	6.9	ns
$C_{PD}$	Power dissipation capacitance <sup>1</sup>	$f = 1\text{MHz}; C_L = 50\text{pF}$	122	117	pF
$C_{IN}$	Input capacitance	$V_I = 0\text{V or } V_{CC}$	4.0	4.0	pF
$I_{LATCH}$	Latch-up current	Per JEDEC JC40.2 Standard 17	500	500	mA
$f_{MAX}$	Maximum clock frequency	$C_L = 50\text{pF}$	100	100	MHz

#### Note:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$

$f_i$  = input frequency in MHz,  $C_L$  = output load capacitance in pF,

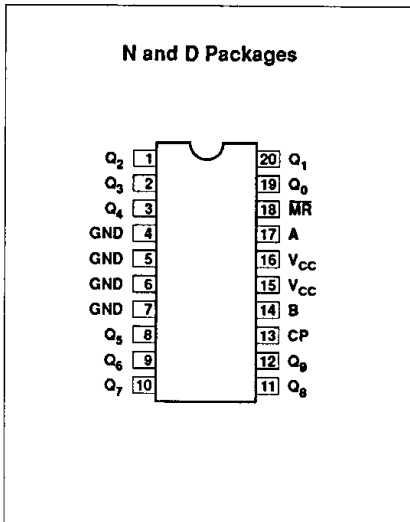
$f_o$  = output frequency in MHz,  $V_{CC}$  = supply voltage in V,

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

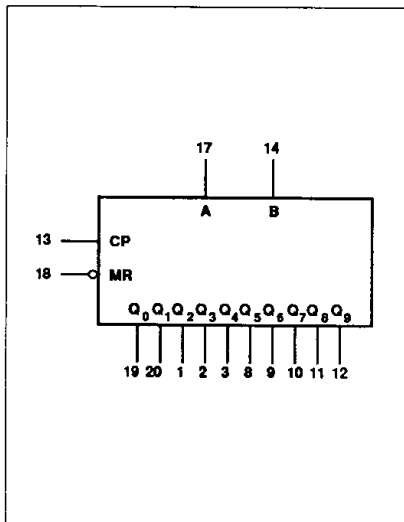
### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11898N 74ACT11898N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11898D 74ACT11898D

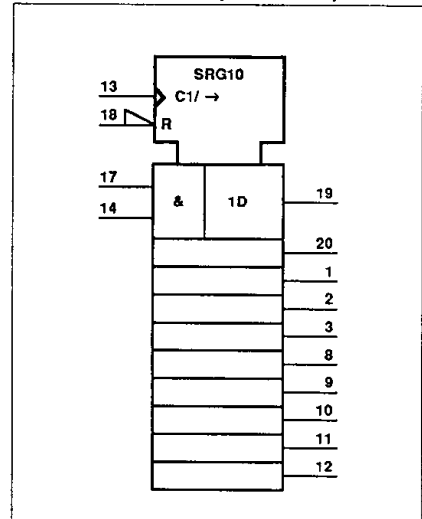
### PIN CONFIGURATION



### LOGIC SYMBOL



### LOGIC SYMBOL (IEEE/IEC)



# 10-bit serial-in parallel-out shift register

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can be used as an active-High enable for data entry through the other input. Otherwise both inputs must be connected to the input data or an unused input must be tied High.

Data shifts one place to the right on each Low-to-High transition of the Clock (CP) input and enters the logical AND of the two inputs (A • B) that existed one setup time before the rising clock edge

into Q<sub>0</sub>. A Low level on the Master Reset ( $\overline{MR}$ ) input overrides all other inputs and clears the register asynchronously, forcing all outputs Low.

### PIN DESCRIPTION

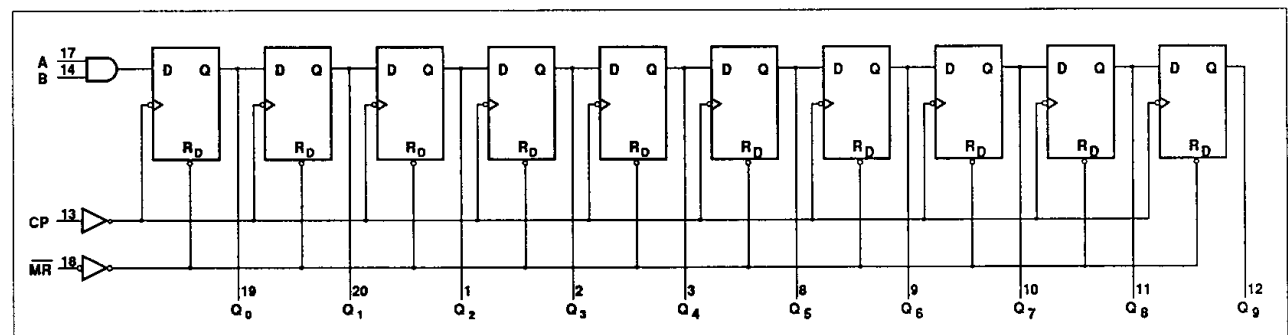
PIN NUMBER	SYMBOL	NAME AND FUNCTION
18	$\overline{MR}$	Asynchronous master reset (active Low)
13	CP	Clock input (Low-to-High, edge-triggered)
17, 14	A, B	Data inputs
19, 20, 1, 2, 3, 8, 9, 10, 11, 12	Q <sub>0</sub> - Q <sub>9</sub>	Parallel outputs outputs
4, 5, 6, 7	GND	Ground (0V)
15, 16	V <sub>CC</sub>	Positive supply voltage

### FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS			
	$\overline{MR}$	CP	A	B	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>9</sub>	
Reset (clear)	L	X	X	X	L	L	L	
Shift	H	↑	l	l	L	q <sub>0</sub>	q <sub>9</sub>	
	H	↑	l	h	L	q <sub>0</sub>	q <sub>9</sub>	
	H	↑	h	l	L	q <sub>0</sub>	q <sub>9</sub>	
	H	↑	h	h	H	q <sub>0</sub>	q <sub>9</sub>	

H = High voltage level  
 L = Low voltage level  
 h = High voltage level one setup time prior to the Low-to High clock transition  
 l = Low voltage level one setup time prior to the Low-to High clock transition  
 X = Don't care  
 q<sub>n</sub> = State of the referenced input (or output) one setup time prior to the Low-to-High clock transition  
 ↑ = Low-to-High clock transition

### LOGIC DIAGRAM



## 10-bit serial-in parallel-out shift register

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11898			74ACT11898			UNIT
		Min	Nom	Max	Min	Nom	Max	
$V_{CC}$	DC supply voltage	3.0 <sup>1</sup>	5.0	5.5	4.5	5.0	5.5	V
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$\Delta I/\Delta V$	Input transition rise or fall rate	0		10	0		10	ns/V
$T_{amb}$	Operating free-air temperature range	-40		+85	-40		+85	°C

## NOTE:

- No electrical or switching characteristics are specified at  $V_{CC} < 3V$ . Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 TO +7.0	V
$I_{IK}$ or $V_I$	DC input diode current <sup>2</sup>	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to $V_{CC} + 0.5$	V
$I_{OK}$ or $V_O$	DC output diode current <sup>2</sup>	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to $V_{CC} + 0.5$	V
$I_O$	DC output source or sink current per output pin	$V_O = 0$ to $V_{CC}$	$\pm 50$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ current		$\pm 250$	mA
	DC ground current		$\pm 250$	
$T_{STG}$	Storage temperature		-65 to 150	°C
$P_{TOT}$	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

## NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	74AC11898				74ACT11898				UNIT	
				T <sub>amb</sub> = +25°C		T <sub>amb</sub> = -40°C to +85°C		T <sub>amb</sub> = +25°C		T <sub>amb</sub> = -40°C to +85°C			
				Min	Max	Min	Max	Min	Max	Min	Max		
V <sub>IH</sub>	High-level input voltage		3.0	2.10		2.10						V	
			4.5	3.15		3.15		2.0		2.0			
			5.5	3.85		3.85		2.0		2.0			
V <sub>IL</sub>	Low-level input voltage		3.0		0.90		0.90					V	
			4.5		1.35		1.35		0.8		0.8		
			5.5		1.65		1.65		0.8		0.8		
V <sub>OH</sub>	High-level output voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OH</sub> = -50μA	3.0	2.9		2.9					V	
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I <sub>OH</sub> = -4mA	3.0	2.58		2.48						
				4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
				5.5			3.85				3.85		
V <sub>OL</sub>	Low-level output voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OL</sub> = 50μA	3.0		0.1		0.1				V	
				4.5		0.1		0.1		0.1			0.1
				5.5		0.1		0.1		0.1			0.1
			I <sub>OL</sub> = 12mA	3.0		0.36		0.44					
				4.5		0.36		0.44		0.36			0.44
				5.5		0.36		0.44		0.36			0.44
				5.5				1.65					1.65
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5		±0.1		±1.0		±0.1		±1.0	μA	
I <sub>CC</sub>	Quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0mA	5.5		8.0		80		8.0		80	μA	
ΔI <sub>CC</sub>	Supply current, TTL inputs High <sup>2</sup>	One input at 3.4V, other inputs at V <sub>CC</sub> or GND	5.5						0.9		1.0	mA	

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V<sub>CC</sub>.

## 10-bit serial-in parallel-out shift register

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AC ELECTRICAL CHARACTERISTICS AT 3.3V  $\pm 0.3V$ 

SYMBOL	PARAMETER	WAVEFORM	74AC11898					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum clock frequency	1	40	65		40		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Q <sub>n</sub>	1	3.3 3.9	8.1 8.8	9.8 10.5	3.3 3.9	10.8 11.5	ns
t <sub>PHL</sub>	Propagation delay $\overline{MR}$ to Q <sub>n</sub>	2	4.1	9.3	11.2	4.1	12.3	ns
t <sub>S</sub>	Setup time, High or Low A, B to CP	3	14.0			14.0		ns
t <sub>H</sub>	Hold time, High or Low A, B to CP	3	0.0			0.0		ns
t <sub>W</sub>	Clock pulse width (shift) High or Low	1	12.5			12.5		ns
t <sub>W</sub>	$\overline{MR}$ pulse width, Low	2	4.0			4.0		ns
t <sub>REC</sub>	Recovery time $\overline{MR}$ to CP	2	1.5			1.5		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V  $\pm 0.5V$ 

SYMBOL	PARAMETER	WAVEFORM	74AC11898					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum clock frequency	1	75	100		75		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Q <sub>n</sub>	1	2.7 3.1	5.5 6.3	7.4 8.3	2.7 3.1	8.1 9.0	ns
t <sub>PHL</sub>	Propagation delay $\overline{MR}$ to Q <sub>n</sub>	2	3.8	6.7	8.6	3.8	9.4	ns
t <sub>S</sub>	Setup time, High or Low A, B to CP	3	8.5			8.5		ns
t <sub>H</sub>	Hold time, High or Low A, B to CP	3	0.0			0.0		ns
t <sub>W</sub>	Clock pulse width (shift) High or Low	1	6.7			6.7		ns
t <sub>W</sub>	$\overline{MR}$ pulse width, Low	2	4.0			4.0		ns
t <sub>REC</sub>	Recovery time $\overline{MR}$ to CP	2	1.5			1.5		ns

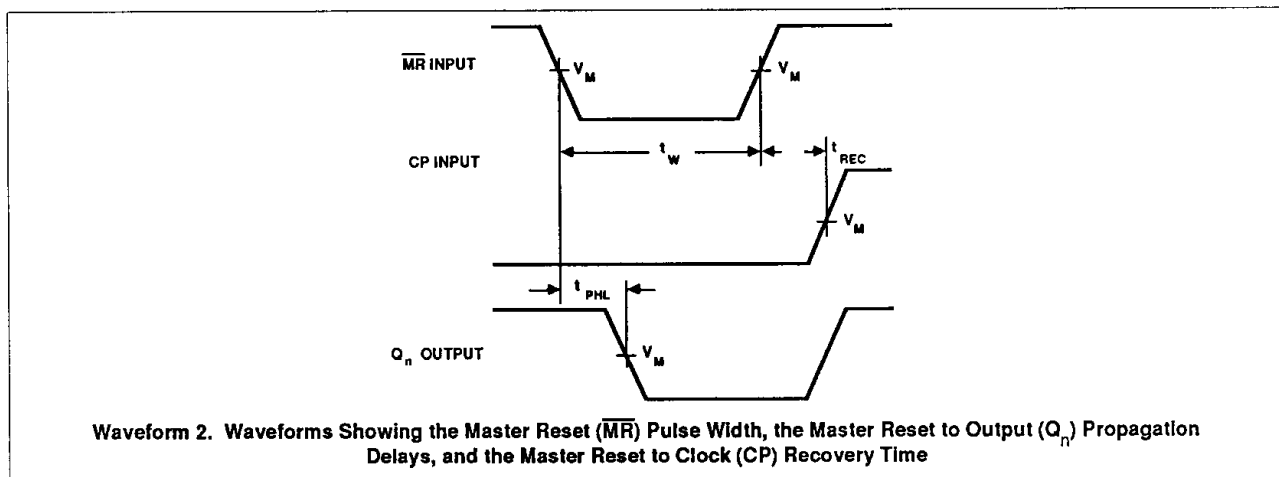
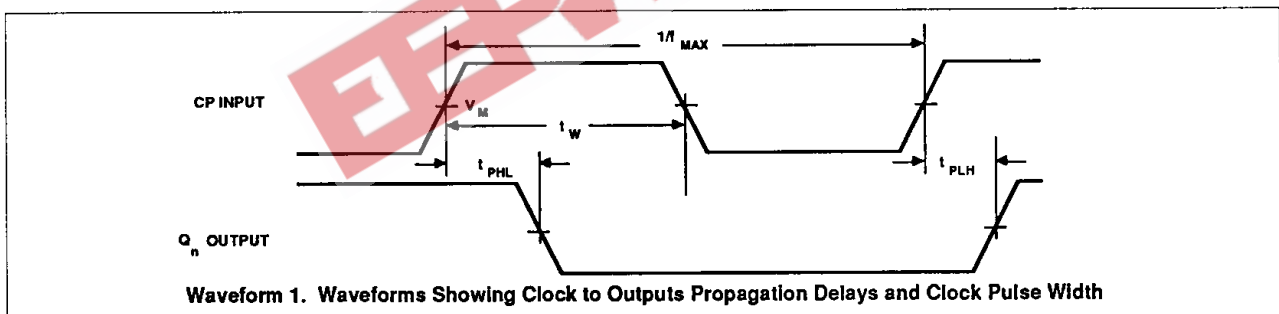
# 10-bit serial-in parallel-out shift register

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## AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11898					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum clock frequency	1	75	100		75		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Q <sub>n</sub>	1	4.1 4.4	6.5 7.2	8.0 8.8	4.1 4.4	8.8 9.6	ns
t <sub>PHL</sub>	Propagation delay $\overline{MR}$ to Q <sub>n</sub>	2	4.6	8.0	10.3	4.6	11.3	ns
t <sub>S</sub>	Setup time, High or Low A, B to CP	3	9.5			9.5		ns
t <sub>H</sub>	Hold time, High or Low A, B to CP	3	0.0			0.0		ns
t <sub>W</sub>	Clock pulse width (shift) High or Low	1	6.7			6.7		ns
t <sub>W</sub>	$\overline{MR}$ pulse width, Low	2	4.5			4.5		ns
t <sub>REC</sub>	Recovery time $\overline{MR}$ to CP	2	1.5			1.5		ns

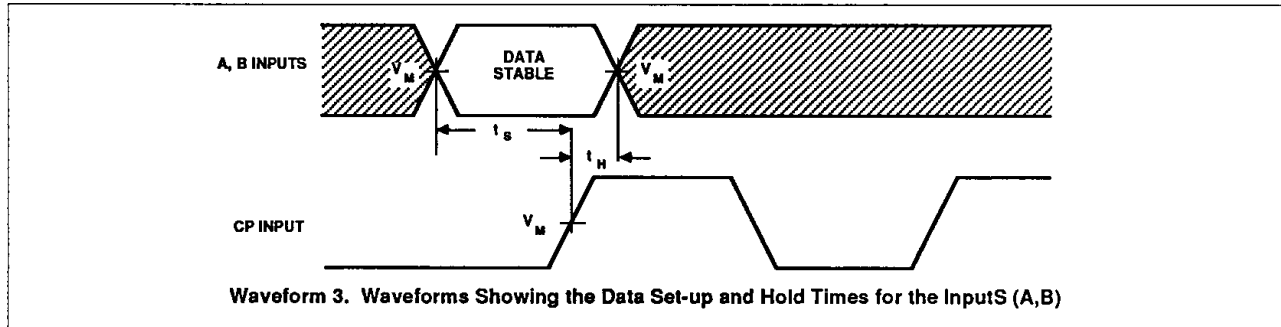
## AC WAVEFORMS



# 10-bit serial-in parallel-out shift register

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## AC WAVEFORMS (Continued)



## WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	$V_{IN} = \text{GND to } V_{CC}$ $V_M = 50\% V_{CC}$	$V_{OUT} = V_{OL} \text{ to } V_{OH}$
ACT	$V_{IN} = \text{GND to } 3.0V$ , $V_M = 1.5V$	$V_M = 50\% V_{CC}$

## TEST CIRCUIT

