



June 1990

# 54FCT/74FCT374A Octal D Flip-Flop with TRI-STATE® Outputs

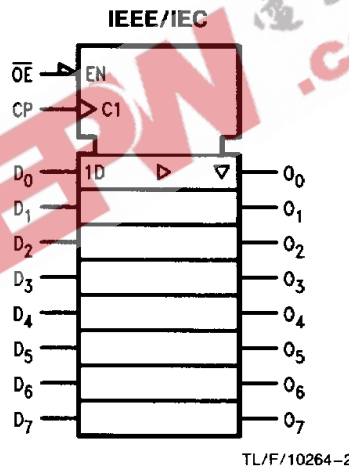
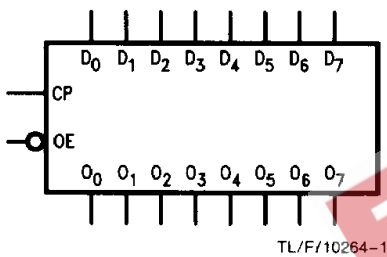
## General Description

The 'FCT374A is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ( $\overline{OE}$ ) are common to all flip-flops.

## Features

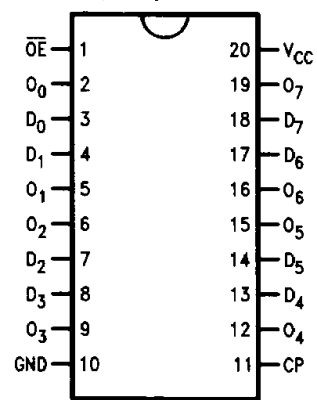
- NSC 54/74FCT374A is pin and functionally equivalent to IDT 54/74FCT374A
- Buffered positive edge triggered clock
- TRI-STATE outputs for bus-oriented applications
- TTL input and output level compatible
- TTL inputs accept CMOS levels
- High current latch up immunity
- $I_{OL} = 48$  mA (commercial) and 32 mA (military)
- Electrostatic discharge protection  $\geq 2$  kV
- Inherently radiation tolerant

## Logic Symbols



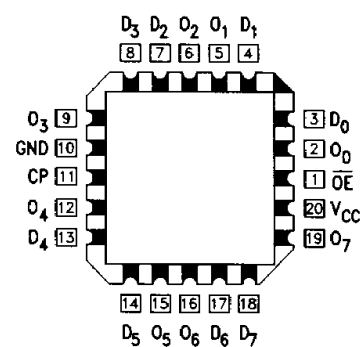
## Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O <sub>0</sub> -O <sub>7</sub>	TRI-STATE Outputs

Pin Assignment for LCC





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54FCT/74FCT374A Octal D Flip-Flop with TRI-STATE Outputs

## Functional Description

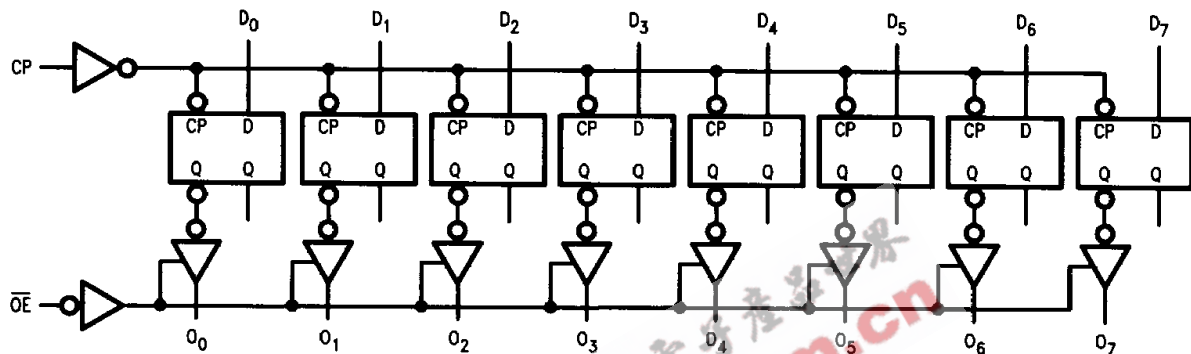
The 'FCT374A consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

## Truth Table

Inputs			Outputs
$D_n$	CP	$\overline{OE}$	$O_n$
H		L	H
L		L	L
X	X	H	Z

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 = LOW-to-HIGH Transition

## Logic Diagram



TL/F/10264-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND ( $V_{TERM}$ )		
54FCTA		-0.5V to 7.0V
74FCTA		-0.5V to 7.0V
Temperature under Bias ( $T_{BIAS}$ )		
74FCTA		-55°C to +125°C
54FCTA		-65°C to +135°C
Storage Temperature ( $T_{STG}$ )		
74FCTA		-55°C to +125°C
54FCTA		-65°C to +150°C
Power Dissipation ( $P_T$ )		0.5W
DC Output Current ( $I_{OUT}$ )		120 mA

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT FCT circuits outside databook specifications.

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )		
54FCTA		4.5V to 5.5V
74FCTA		4.75V to 5.25V
Input Voltage		0V to $V_{CC}$
Output Voltage		0V to $V_{CC}$
Operating Temperature ( $T_A$ )		
54FCTA		-55°C to +125°C
74FCTA		0°C to +70°C
Junction Temperature ( $T_J$ )		
CDIP		175°C
PDIP		140°C

## DC Characteristics for 'FCTA Family Devices

Typical values are at  $V_{CC} = 5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ ; Mil:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -55^\circ C$  to  $+125^\circ C$ ,  $V_{HC} = V_{CC} - 0.2V$ .

Symbol	Parameter	54FCTA/74FCTA			Units	Conditions	
		Min	Typ	Max			
$V_{IH}$	Minimum High Level Input Voltage	2.0			V		
$V_{IL}$	Maximum Low Level Input Voltage			0.8	V		
$I_{IH}$	Input High Current			5.0 5.0	$\mu A$	$V_{CC} = \text{Max}$	$V_I = V_{CC}$ $V_I = 2.7V$ (Note 2)
$I_{IL}$	Input Low Current			-5.0 -5.0	$\mu A$	$V_{CC} = \text{Max}$	$V_I = 0.5V$ (Note 2) $V_I = \text{GND}$
$I_{OZ}$	Maximum TRI-STATE Current			10.0 10.0 -10.0 -10.0	$\mu A$	$V_{CC} = \text{Max}$	$V_O = V_{CC}$ $V_O = 2.7V$ (Note 2) $V_O = 0.5V$ (Note 2) $V_O = \text{GND}$
$V_{IK}$	Clamp Diode Voltage		-0.7	-1.2	V	$V_{CC} = \text{Min}; I_N = -18 \text{ mA}$	
$I_{OS}$	Short Circuit Current	-60	-120		mA	$V_{CC} = \text{Max}$ (Note 1); $V_O = \text{GND}$	
$V_{OH}$	Minimum High Level Output Voltage	2.8 $V_{HC}$ 2.4 2.4	3.0 $V_{CC}$ 4.3 4.3		V	$V_{CC} = 3V; V_{IN} = 0.2V$ or $V_{HC}; I_{OH} = -32 \mu A$ $V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -300 \mu A$ $I_{OH} = -12 \text{ mA}$ (Mil) $I_{OH} = -15 \text{ mA}$ (Com)
$V_{OL}$	Maximum Low Level Output Voltage		GND GND 0.3 0.3	0.2 0.2 0.50 0.50	V	$V_{CC} = 3V; V_{IN} = 0.2V$ or $V_{HC}; I_{OL} = 300 \mu A$ $V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 300 \mu A$ $I_{OL} = 32 \text{ mA}$ (Mil) $I_{OL} = 48 \text{ mA}$ (Com)
$I_{CC}$	Maximum Quiescent Supply Current		0.001	1.5	mA	$V_{CC} = \text{Max}$ $V_{IN} \geq V_{HC}, V_{IN} \leq 0.2V$ $f_I = 0$	
$\Delta I_{CC}$	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	$V_{CC} = \text{Max}$ $V_{IN} = 3.4V$ (Note 3)	

## DC Characteristics for 'FCTA Family Devices (Continued)

Typical values are at  $V_{CC} = 5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ ; Mil:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -55^\circ C$  to  $+125^\circ C$ ,  $V_{HC} = V_{CC} - 0.2V$ .

Symbol	Parameter	54FCTA/74FCTA			Units	Conditions	
		Min	Typ	Max			
$I_{CCD}$	Dynamic Power Supply Current (Note 4)		0.15	0.25	mA/MHz	$V_{CC} = \text{Max}$ Outputs Open $\overline{OE} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
$I_C$	Total Power Supply Current (Note 6)		1.5	4.0			
			2.0	6.0	mA	$V_{CC} = \text{Max}$ Outputs Open $f_{CP} = 10 \text{ MHz}$ $\overline{OE} = \text{GND}$ $f_i = 5.0 \text{ MHz}$ One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			3.75	7.8			
			6.0	16.8		(Note 5) $V_{CC} = \text{Max}$ Outputs Open $f_{CP} = 10 \text{ MHz}$ $\overline{OE} = \text{GND}$ $f_i = 2.5 \text{ MHz}$ Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
							$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$
$V_H$	Input Hysteresis on Clock Only		200		mV		

**Note 1:** Maximum test duration not to exceed one second, not more than one output shorted at one time.

**Note 2:** This parameter guaranteed but not tested.

**Note 3:** Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.

**Note 4:** This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

**Note 5:** Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.

**Note 6:**  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$$

$I_{CC}$  = Quiescent Current

$\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )

$D_H$  = Duty Cycle for TTL Inputs High

$N_T$  = Number of Inputs at  $D_H$

$I_{CCD}$  = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

$f_{CP}$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)

$f_i$  = Input Frequency

$N_i$  = Number of Inputs at  $f_i$

All currents are in milliamps and all frequencies are in megahertz.

## AC Electrical Characteristics

Symbol	Parameter	54FCTA/74FCTA	74FCTA		54FCTA		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	$T_A, V_{CC} = \text{Com}$ $R_L = 500\Omega$ $C_L = 50\text{pF}$		$T_A, V_{CC} = \text{Mil}$ $R_L = 500\Omega$ $C_L = 50\text{pF}$		
		Typ	Min (Note 1)	Max	Min (Note 1)	Max	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $C_p$ to $O_n$	4.5	2.0	6.5			ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time	5.5	1.5	6.5			ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time	4.0	1.5	5.5			ns
$t_{SU}$	Set Up Time High or Low $D_n$ to $C_p$	1.0	2.0				ns
$t_H$	Hold Time High or Low $D_n$ to $C_p$	0.5	1.5				ns
$t_w$	$C_p$ Pulse Width High or Low	4.0	5.0				ns

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

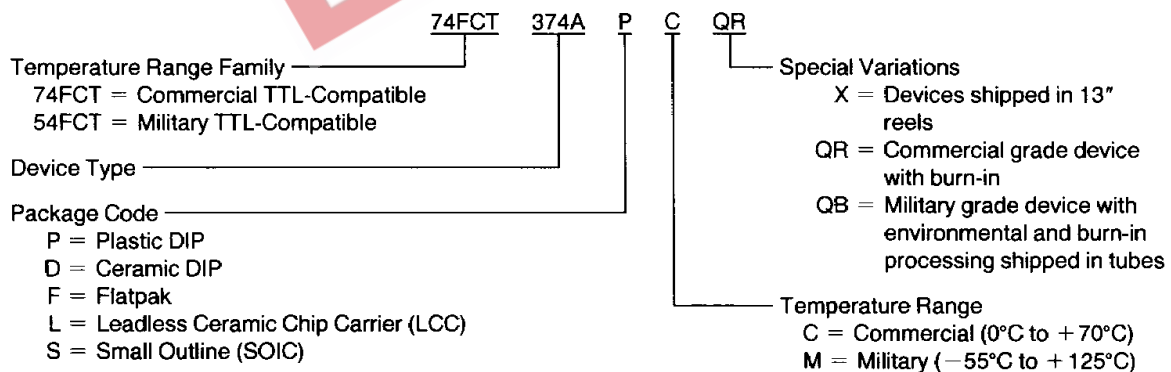
## Capacitance $T_A = +25^\circ\text{C}, f = 1.0\text{MHz}$

Symbol	Parameter (Note)	Typ	Max	Unit	Condition
$C_{IN}$	Input Capacitance	6	10	pF	$V_{IN} = 0\text{V}$
$C_{OUT}$	Output Capacitance	8	12	pF	$V_{OUT} = 0\text{V}$

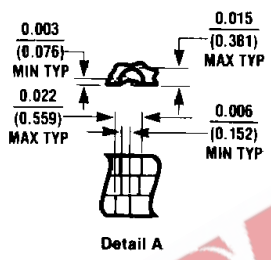
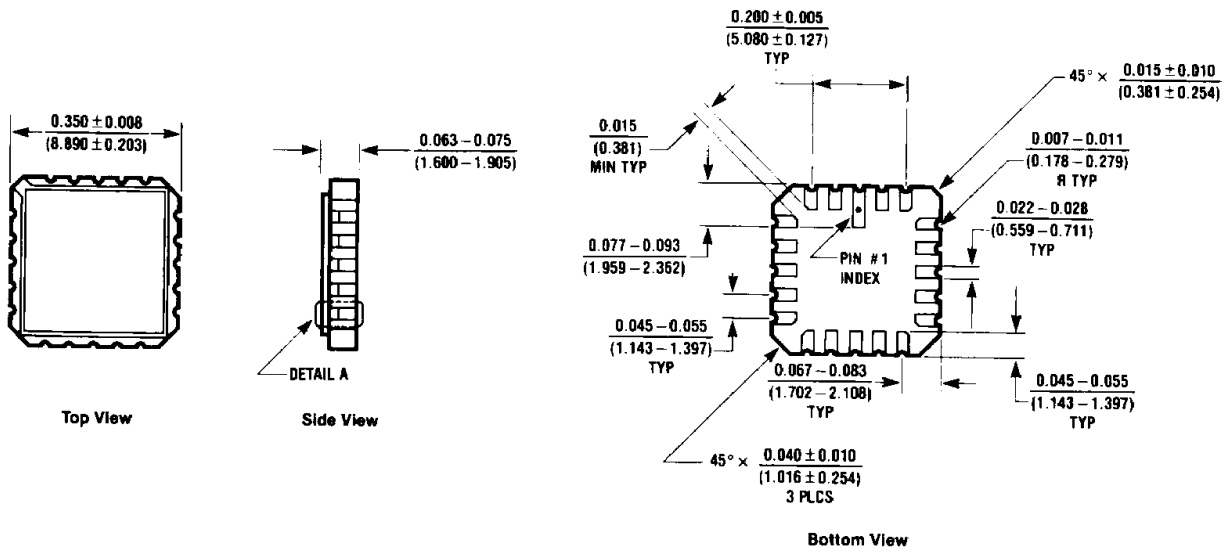
Note: This parameter is measured at characterization but not tested.

## Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

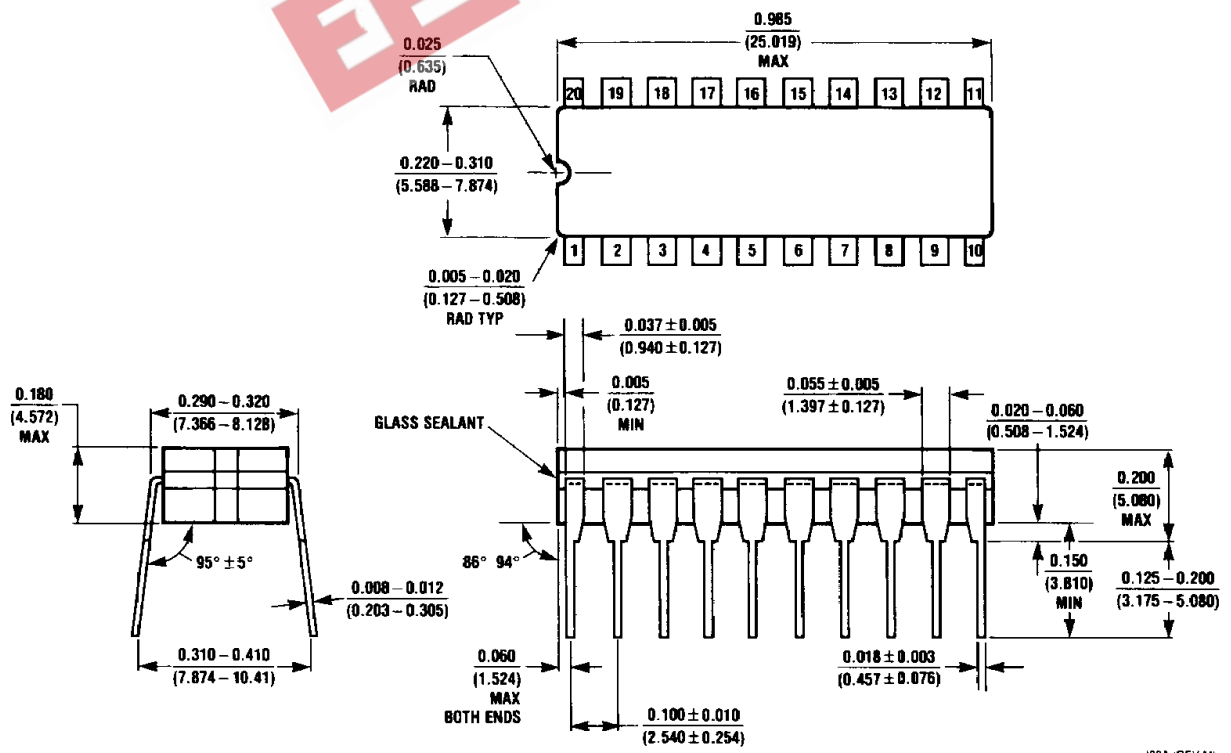


# Physical Dimensions inches (millimeters)



**20-Terminal Ceramic Leadless Chip Carrier (L)**  
 NS Package Number E20A

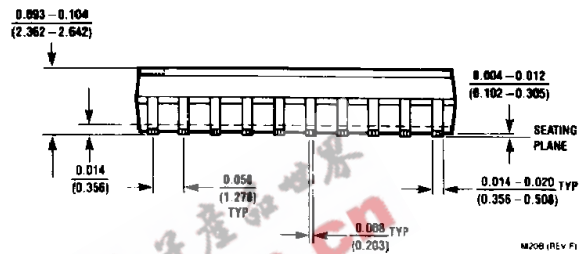
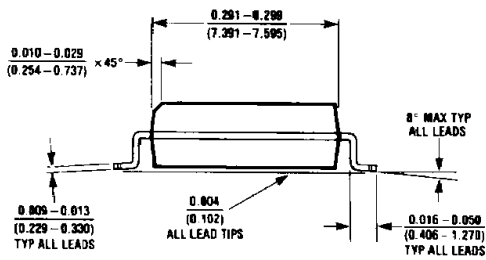
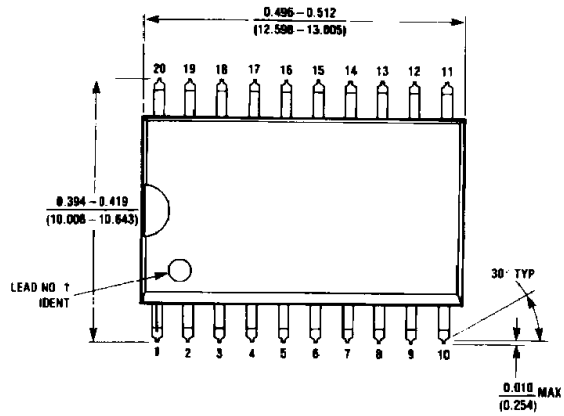
E20A (REV D)



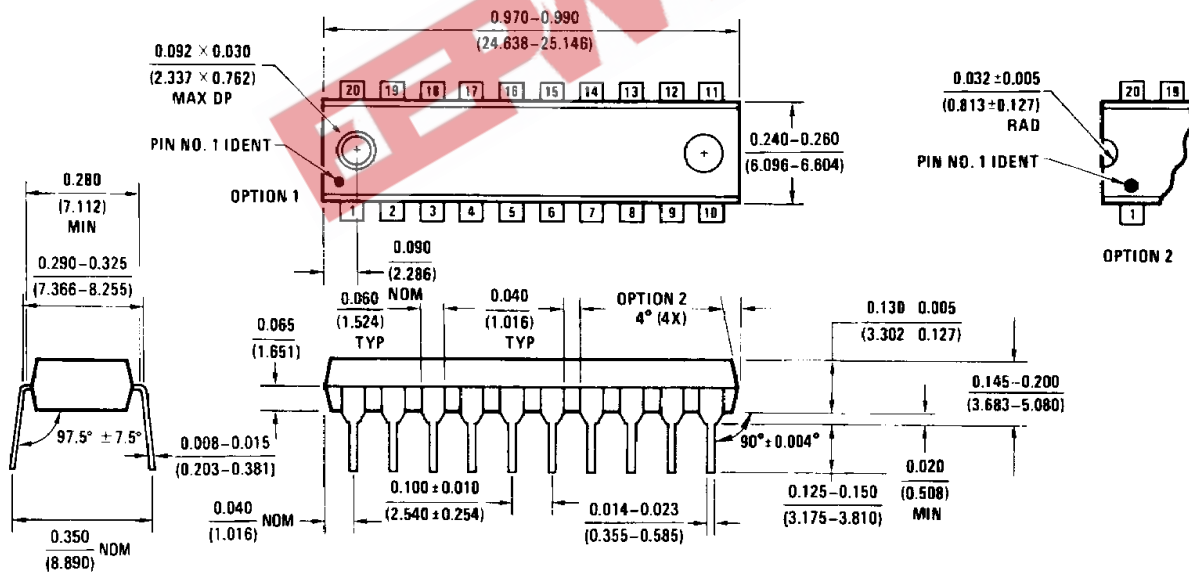
**20-Lead Ceramic Dual-In-Line Package (D)**  
 NS Package Number J20A

J20A (REV M)

**Physical Dimensions** inches (millimeters) (Continued)



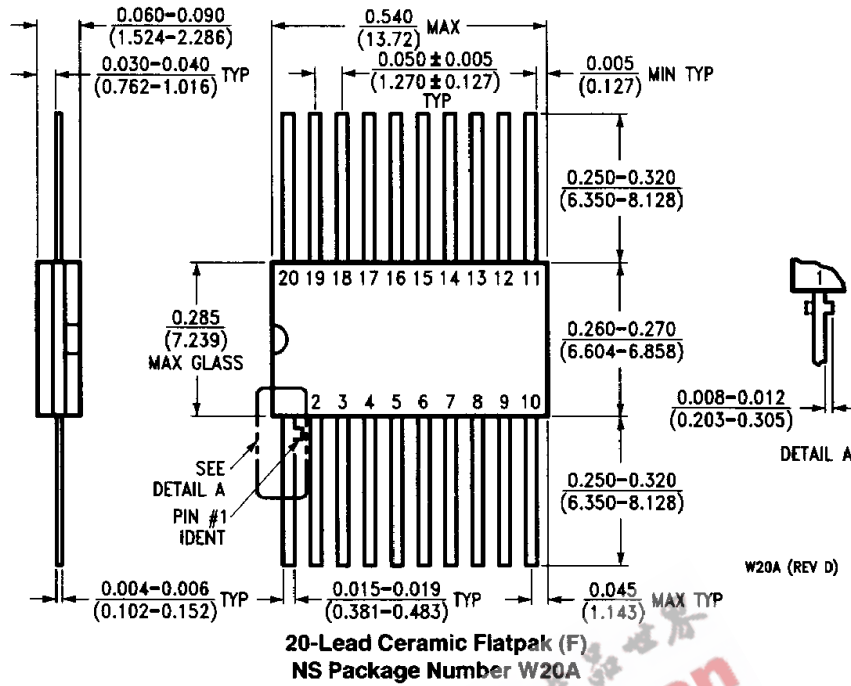
**20-Lead Small Outline Integrated Circuit (S)  
NS Package Number M20B**



**20-Lead Plastic Dual-In-Line Package (P)  
NS Package Number N20B**

**Physical Dimensions** inches (millimeters) (Continued)

Lit. # 114703



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