## SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SDAS143C - APRIL 1982 - REVISED AUGUST 1995

### Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

ТҮРЕ	TYPICAL MAXIMUM CLOCK FREQUENCY (CL = 50 pF) (MHz)	TYPICAL POWER DISSIPATION PER FLIP-FLOP (mW)
'ALS74A	50	6
′AS74A	134	26

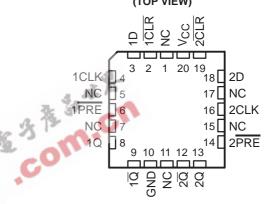
### description

devices These contain two independent positive-edge-triggered D-type flip-flops. A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The SN54ALS74A and SN54AS74A are characterized for operation over the full military temperature range of  $-55^{\circ}$ C to  $125^{\circ}$ C. The SN74ALS74A and SN74AS74A are characterized for operation from 0°C to 70°C.

SN74ALS74A, SN74	SN54ALS74A, SN54AS74A J PACKAGE SN74ALS74A, SN74AS74A D OR N PACKAGE (TOP VIEW)								
1CLR [ 1D [ 1CLK [ 1PRE [ 1Q [ GND [	1 2 3 4 5 6 7	14 13 12 11 10 9 8	] V <sub>CC</sub> ] 2CLR ] 2D ] 2CLK ] 2PRE ] 2Q ] 2Q						

#### SN54ALS74A, SN54AS74A...FK PACKAGE (TOP VIEW)



NC - No internal connection

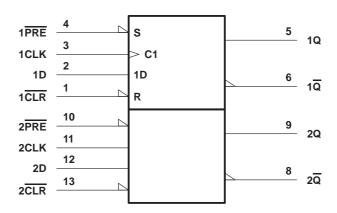
		0110110		_	
	INP	UTS		OUTI	PUTS
PRE	CLR	CLK	D	Q	Q
L	Н	Х	Х	Н	L
н	L	Х	Х	L	Н
L	L	Х	Х	н†	H‡
н	Н	$\uparrow$	Н	н	L
н	Н	$\uparrow$	L	L	Н
н	Н	L	Х	Q <sub>0</sub>	$\overline{Q}_0$

FUNCTION TABLE

<sup>†</sup> The output levels in this configuration are not specified to meet the minimum levels for V<sub>OH</sub> if the lows at PRE and CLR are near V<sub>IL</sub> maximum. Furthermore, this configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

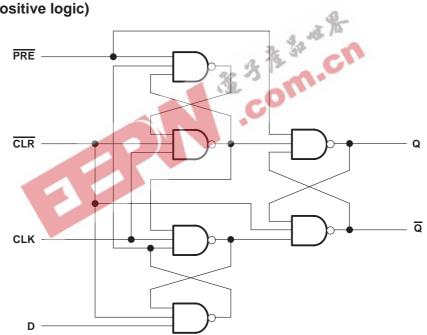
# SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A **DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS** WITH CLEAR AND PRESET SDAS143C - APRIL 1982 - REVISED AUGUST 1995

### logic symbol<sup>†</sup>



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, and N packages.

### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>‡</sup>

Supply voltage, V <sub>CC</sub>	
Operating free-air temperature range, T <sub>A</sub> : SN54ALS74A	-55°C to 125°C
SN74ALS74A	0°C to 70°C
Storage temperature range	-65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



# SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

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### recommended operating conditions

			SN	54ALS7	4A	SN74ALS74A		UNIT	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	V
IOH	High-level output current				-0.4			-0.4	mA
IOL	Low-level output current				4			8	mA
fclock	Clock frequency		0		25	0		34	MHz
		PRE or CLR low	15			15			
tw	Pulse duration	CLK high	17.5			14.5			ns
		CLK low	17.5			14.5			
		Data	16			15			
t <sub>su</sub>	Setup time before CLK <sup>↑</sup>	PRE or CLR inactive	10			10			ns
t <sub>h</sub>	Hold time after CLK↑	Data	2			0			ns
TA	Operating free-air temperature		-55	.0	125	0		70	°C
. A					.20			10	

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) 23 G

PARAMETER		TEAT OON		SN	54ALS7	4A	SN	74ALS74	1A	
		TEST CON	TEST CONDITIONS		TYP <sup>†</sup>	MAX	MIN	TYP†	MAX	UNIT
VIK		V <sub>CC</sub> = 4.5 V,	lj = -18 mA			-1.5			-1.5	V
VOH		$V_{CC} = 4.5 V \text{ to } 5.5 V,$	I <sub>OH</sub> = -2 mA	V <sub>CC</sub> -2			V <sub>CC</sub> -2			V
Vai		V <sub>CC</sub> = 4.5 V	$I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
VOL		$V_{CC} = 4.5 V$	$I_{OL} = 8 \text{ mA}$					0.35	0.5	v
1.	CLK or D		VCC = 4.5 V, VI = 7 V			0.1			0.1	mA
1	PRE or CLR	$V_{CC} = 4.5 V,$				0.2			0.2	IIIA
I	CLK or D					20			20	A
lΗ	PRE or CLR	$V_{\rm CC} = 4.5  \rm V,$	V <sub>I</sub> = 2.7 V			40			40	μA
lu.	CLK or D		V <sub>I</sub> = 0.4 V			-0.2			-0.2	m۸
ΊL	PRE or CLR	$V_{CC} = 4.5 V,$	$v_{\rm CC} = 4.3 v,$ $v_{\rm I} = 0.4 v$			-0.4			-0.4	mA
10‡		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	-20		-112	-30		-112	mA
ICC		V <sub>CC</sub> = 5.5 V,	See Note 1		2.4	4		2.4	4	mA

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

<sup>‡</sup> The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>. NOTE 1: I<sub>CC</sub> is measured with D, CLK, and PRE grounded, then with D, CLK, and CLR grounded.



# SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A **DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS** WITH CLEAR AND PRESET SDAS143C - APRIL 1982 - REVISED AUGUST 1995

### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CL RL T <sub>A</sub>	= 50 pl = 500 = MIN t	<sup>2,</sup> o MAX†		UNIT
			SN54A		SN74A		
			MIN	MAX	MIN	MAX	
fmax			25		34		MHz
<sup>t</sup> PLH	PRE or CLR	Q or Q	3	18	3	13	ns
<sup>t</sup> PHL	PRE OF CLR	Q OF Q	5	17	5	15	115
<sup>t</sup> PLH	CLK	Q or Q	5	23	5	16	ns
<sup>t</sup> PHL	ULK		5	20	5	18	115

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>‡</sup>

Supply voltage, V <sub>CC</sub>			7 V
Input voltage, V <sub>1</sub>			7 V
Operating free-air temperature range, T <sub>A</sub> :			
	SN74AS74A	· · ·	0°C to 70°C
Storage temperature range		A. 19	–65°C to 150°C
5 1 5	30 .		

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

			SN	154AS74	A	SN	174AS74	A	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.8			0.8	V
ЮН	High-level output current				-2			-2	mA
IOL	Low-level output current				20			20	mA
fclock*	Clock frequency		0		90	0		105	MHz
		PRE or CLR low	4			4			
tw*	Pulse duration	CLK high	4			4			ns
		CLK low	5.5			5.5			
+ *		Data	4.5			4.5			ns
t <sub>su</sub> *	Setup time before CLK <sup>↑</sup>	PRE or CLR inactive	2			2			115
t <sub>h</sub> *	Hold time after $CLK^\uparrow$	Data	0			0			ns
ТА	Operating free-air temperature		-55		125	0		70	°C

\* On products compliant to MIL-STD-833, Class B, this parameter is based on characterization data but is not production tested.



### SN54ALS74A, SN54AS74A, SN74ALS74A, SN74AS74A **DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS** WITH CLEAR AND PRESET SDAS143C - APRIL 1982 - REVISED AUGUST 1995

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CO	NDITIONS	SN	54AS74	A	SN	74AS74	A	UNIT
	PARAMETER	TEST COL	NDITIONS	MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT
VIK		V <sub>CC</sub> = 4.5 V,	lj = -18 mA			-1.2			-1.2	V
VOH		$V_{CC} = 4.5 V$ to 5.5 V,	$I_{OH} = -2 \text{ mA}$	V <sub>CC</sub> -2			V <sub>CC</sub> -2			V
VOL		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 20 mA		0.25	0.5		0.25	0.5	V
Ц		V <sub>CC</sub> = 5.5 V,	$V_{I} = 7 V$			0.1			0.1	mA
	CLK or D		V <sub>I</sub> = 2.7 V			20			20	μA
ЧΗ	PRE or CLR	$V_{\rm CC} = 5.5 \text{ V}, \qquad V_{\rm I} = 2.7 \text{ V}$	$v_{1} = 2.7 v_{1}$			40			40	μΑ
1	CLK or D					-0.5			-0.5	A
ΊL	PRE or CLR	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V			-1.8			-1.8	mA
10‡		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	-30		-112	-30		-112	mA
ICC		V <sub>CC</sub> = 5.5 V,	See Note 1		10.5	16		10.5	16	mA

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

<sup>‡</sup> The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>. NOTE 1: I<sub>CC</sub> is measured with D, CLK, and PRE grounded, then with D, CLK, and CLR grounded.

### switching characteristics (see Figure 1)

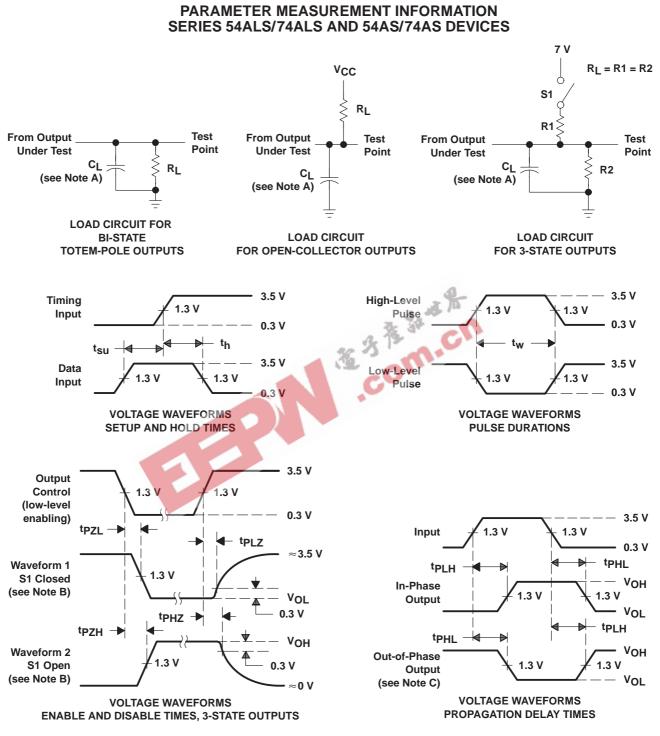
NOTE 1: ICC is measured with D, CLK, and PRE grounded, then with D, CLK, and CLR grounded.									
switching characteris	stics (see Figure 1)	34 - 45 M	0						
PARAMETER	FROM (INPUT)	VCC = 4.5 V to 5.5 V,       CL = 50 pF,       RL = 500 Ω,       TA = MIN to MAX§					UNIT		
			SN54A	S74A	SN74AS74A				
			MIN	MAX	MIN	MAX			
f <sub>max</sub> *			90		105		MHz		
tPLH 🖌			2	9	2	7.5			
<sup>t</sup> PHL	PRE or CLR	Q or $\overline{Q}$	2.5	11.5	2.5	10.5	ns		
<sup>t</sup> PLH	CLK	Q or Q	2.5	10	3	8			
<sup>t</sup> PHL	ULK		3.5	10.5	3	9	ns		

\* On products compliant to MIL-STD-833, Class B, this parameter is based on characterization data but is not production tested. § For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



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NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: PRR  $\leq$  1 MHz, t<sub>r</sub> = t<sub>f</sub> = 2 ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

### Figure 1. Load Circuits and Voltage Waveforms



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