FAIRCHILD SEMICONDUCTOR™

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74F524
8-Bit Registered Comparator

General Description

The 74F524 is an 8-bit bidirectional register with parallel input and output plus serial input and output progressing from LSB to MSB. All data inputs, serial and parallel, are loaded by the rising edge of the input clock. The device functions are controlled by two control lines (S_0, S_1) to execute shift, load, hold and read out.

An 8-bit comparator examines the data stored in the registers and on the data bus. Three true-HIGH, open-collector outputs representing "register equal to bus", "register greater than bus" and "register less than bus" are provided. These outputs can be disabled to the OFF state by the use of Status Enable ($\overline{SE}$). A mode control has also been provided to allow twos complement as well as magnitude compare. Linking inputs are provided for expansion to longer words.

Features

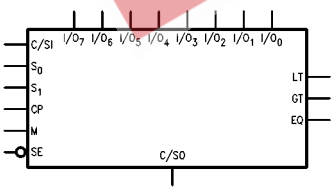
- 8-Bit bidirectional register with bus-oriented input-output
- Independent serial input-output to register
- Register bus comparator with "equal to", "greater than" and "less than" outputs
- Cascadable in groups of eight bits
- Open-collector comparator outputs for AND-wired expansion
- Twos complement or magnitude compare

Ordering Code:

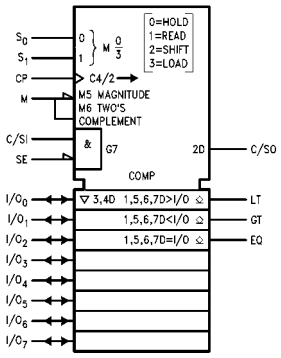
Order Number	Package Number	Package Description
74F524SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F524PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

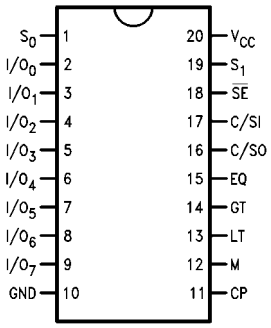
Logic Symbols



IEEE/IEC



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
S_0, S_1	Mode Select Inputs	1.0/1.0	20 µA/–0.6 mA
C/SI	Status Priority or Serial Data Input	1.0/1.0	20 µA/–0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 µA/–0.6 mA
$\overline{SE}$	Status Enable Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
M	Compare Mode Select Input	1.0/1.0	20 µA/–0.6 mA
I/O_0–I/O_7	Parallel Data Inputs or	3.5/1.083	70 µA/–0.65 mA
	3-STATE Parallel Data Outputs	150/40 (33.3)	–3 mA/24 mA (20 mA)
C/SO	Status Priority or Serial Data Output	50/33.3	–1 mA/20 mA
LT	Register Less Than Bus Output	OC (Note 1) /33.3	(Note 1) /20 mA
EQ	Register Equal Bus Output	OC(Note 1) /33.3	(Note 1) /20 mA
GT	Register Greater Than Bus Output	OC(Note 1) /33.3	(Note 1) /20 mA

Note 1: OC = Open Collector

Number Representation Select Table

M	Operation
L	Magnitude Compare
H	Twos Complement Compare

Select Truth Table

S_0	S_1	Operation
L	L	Hold—Retains Data in Shift Register
L	H	Read—Read Contents in Register onto Data Bus, Data Remains in Register Unaffected by Clock
H	L	Shift—Allows Serial Shifting on Next Rising Clock Edge
H	H	Load—Load Data on Bus into Register

Status Truth Table

(Hold Mode)

Inputs			Outputs			
$\overline{SE}$	C/SI	Data Comparison	EQ	GT	LT	C/SO
H	H	X	H	H	H	1
L	L	O_A–O_H > I/O_0–I/O_7	L	H	H	L
X	L	O_A–O_H = I/O_0–I/O_7	H	H	H	L
H	L	O_A–O_H < I/O_0–I/O_7	L	H	H	L
H	H	O_A–O_H > I/O_0–I/O_7	L	H	L	L
H	H	O_A–O_H = I/O_0–I/O_7	H	L	L	H
L	H	O_A–O_H < I/O_0–I/O_7	L	L	H	L

1 = HIGH if data are equal, otherwise LOW
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Functional Description

The 74F524 contains eight D-type flip-flops connected as a shift register with provision for either parallel or serial loading. Parallel data may be read from or loaded into the registers via the data bus I/O_0–I/O_7. Serial data is entered from the C/SI input and may be shifted into the register and out through the C/SO output. Both parallel and serial data entry occur on the rising edge of the input clock (CP). The operation of the shift register is controlled by two signals S_0 and S_1 according to the Select Truth Table. The 3-STATE parallel output buffers are enabled only in the Read mode.

One port of an 8-bit comparator is attached to the data bus while the other port is tied to the outputs of the internal register. Three active-OFF, open-collector outputs indicate whether the contents held in the shift register are “greater than”, (GT), “less than” (LT), or “equal to” (EQ) the data on the input bus. A HIGH signal on the Status Enable ($\overline{SE}$) input disables these outputs to the OFF state. A mode control input (M) allows selection between a straightforward magnitude compare or a comparison between twos complement numbers.

For “greater than” or “less than” detection, the C/SI input must be held HIGH, as indicated in the Status Truth Table. The internal logic is arranged such that a LOW signal on the C/SI input disables the “greater than” and “less than” outputs. The C/SO output will be forced HIGH if the “equal to” status condition exists, otherwise C/SO will be held LOW. These facilities enable the 74F524 to be cascaded for word length greater than eight bits.

Word length expansion (in groups of eight bits) can be achieved by connecting the C/SO output of the more significant byte to the C/$\overline{SI}$ input of the next less significant byte and also to its own $\overline{SE}$ input (see Figure 1). The C/SI input of the most significant device is held HIGH while the $\overline{SE}$ input of the least significant device is held LOW. The corresponding status outputs are AND-wired together. In the case of twos complement number compare, only the Mode input to the most significant device should be HIGH. The Mode inputs to all other cascaded devices are held LOW.

Suppose that an inequality condition is detected in the most significant device. Assuming that the byte stored in the register is greater than the byte on the data bus, the EQ and LT outputs will be pulled LOW and the GT output will float HIGH. Also the C/SO output of the most significant device will be forced LOW, disabling the subsequent devices but enabling its own status outputs. The correct status condition is thus indicated. The same applies if the registered byte is less than the data byte, only in this case the EQ and GT outputs go LOW and LT output floats HIGH.

If an equality condition is detected in the most significant device, its C/SO output is forced HIGH. This enables the next less significant device and also disables its own status outputs. In this way, the status output priority is handed down to the next less significant device which now effectively becomes the most significant byte. The worst case propagation delay for a compare operation involving “n” cascaded 74F524s will be when an equality condition is detected in all but the least significant byte. In this case, the status priority has to ripple all the way down the chain before the correct status output is established. Typically, this will take 35 + 6(n–2) ns.

Function Diagram

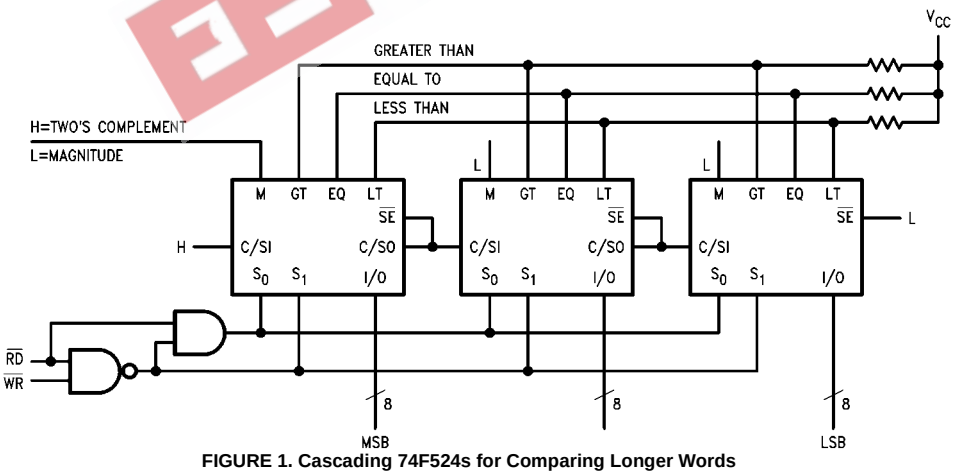
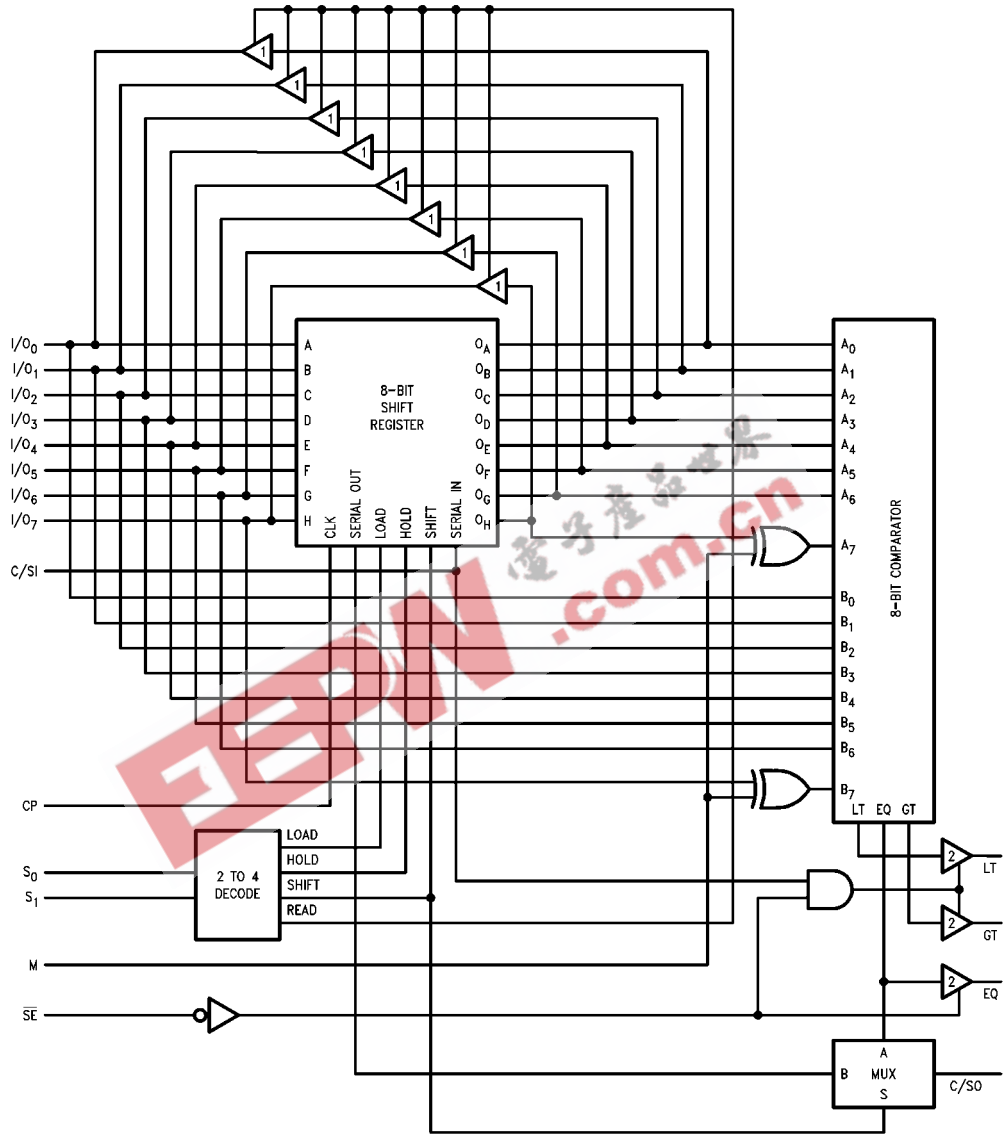


FIGURE 1. Cascading 74F524s for Comparing Longer Words

Block Diagram



Notes:

1. 3-STATE Output
2. Open-Collector Output

Absolute Maximum Ratings(Note 2)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 3)	−0.5V to +7.0V
Input Current (Note 3)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		10% V_{CC}	2.4					I_{OH} = −3 mA
		5% V_{CC}	2.7					I_{OH} = −1 mA
		5% V_{CC}	2.7					I_{OH} = −3 mA
V_{OL}	Output LOW Voltage	10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA (I/O_n)
		10% V_{CC}			0.5			I_{OL} = 24 mA (LT, GT, EQ, C/SO)
I_{IH}	Input HIGH Current				5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				7.0	µA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC} (I/O_n, C/SO)
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{IH} + I_{OZH}	Output Leakage Current				70	µA	Max	$V_{I/O}$ = 2.7V
I_{IL} + I_{OZL}	Output Leakage Current				−650	µA	Max	$V_{I/O}$ = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{OHC}	Open Collector, Output OFF Leakage Test				250	µA	Min	V_{OUT} = V_{CC}
I_{CCH}	Power Supply Current			128	180	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			128	180	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			128	180	mA	Max	V_O = HIGH Z

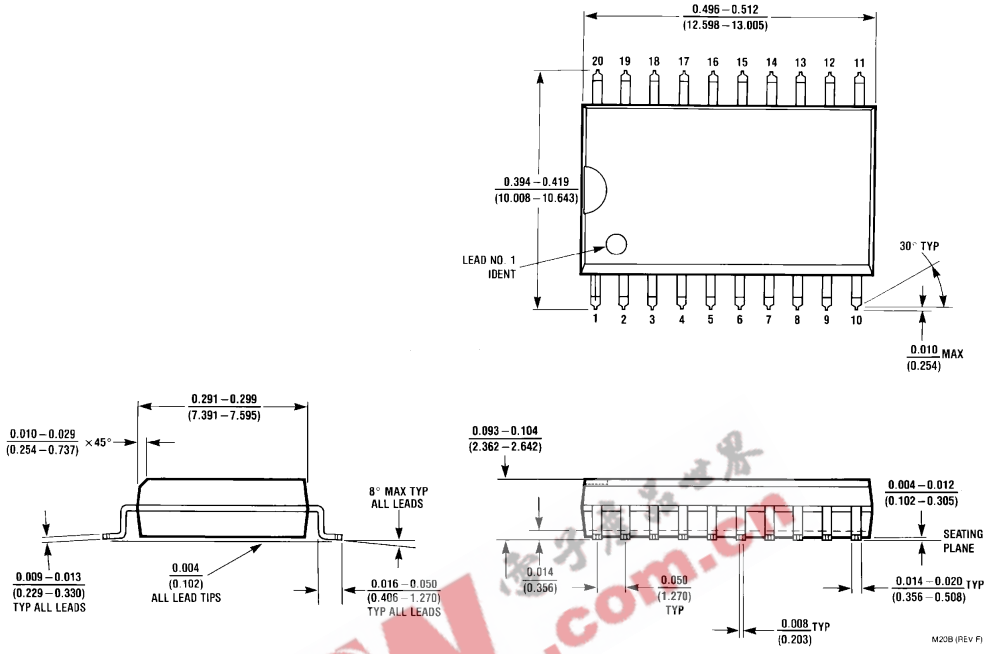
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Shift Frequency	50	75		50		MHz
t_{PLH}	Propagation Delay	9.0	16.5	20.0	9.0	21.0	ns
t_{PHL}	I/O_n to EQ	5.0	9.5	12.0	5.0	13.0	
t_{PLH}	Propagation Delay	8.5	14.1	19.0	8.5	20.0	ns
t_{PHL}	I/O_n to GT	6.5	13.0	16.5	6.5	17.5	
t_{PLH}	Propagation Delay	7.0	15.5	20.0	7.0	21.0	ns
t_{PHL}	I/O_n to LT	4.5	10.0	14.0	4.5	15.0	
t_{PLH}	Propagation Delay	8.0	15.2	19.5	8.0	20.5	ns
t_{PHL}	I/O_n to C/SO	6.0	12.5	16.0	6.0	17.0	
t_{PLH}	Propagation Delay	10.0	20.0	25.0	10.0	26.0	ns
t_{PHL}	CP to EQ	4.0	8.5	16.5	4.0	17.5	
t_{PLH}	Propagation Delay	10.0	16.5	21.0	10.0	22.0	ns
t_{PHL}	CP to GT	8.5	17.0	22.0	8.5	23.0	
t_{PLH}	Propagation Delay	9.0	20.0	25.0	9.0	26.0	ns
t_{PHL}	CP to LT	5.5	13.5	17.0	5.5	18.0	
t_{PLH}	Propagation Delay CP to C/SO (Load)	8.5	16.5	21.0	8.5	22.0	ns
t_{PLH}	Propagation Delay	5.0	10.0	13.0	5.0	14.0	ns
t_{PHL}	CP to C/SO (Serial Shift)	4.5	9.0	11.5	4.5	12.5	
t_{PLH}	Propagation Delay	9.0	15.0	19.0	9.0	20.0	ns
t_{PHL}	C/SI to GT	3.0	6.5	8.5	3.0	9.5	
t_{PLH}	Propagation Delay	8.0	15.5	20.0	8.0	21.0	ns
t_{PHL}	C/SI to LT	3.5	6.5	8.5	3.5	9.5	
t_{PLH}	Propagation Delay	6.5	11.5	14.5	6.5	15.5	ns
t_{PHL}	S_0, S_1 to C/SO	5.5	14.0	18.0	5.5	19.0	
t_{PLH}	Propagation Delay	3.5	8.0	10.5	3.5	11.5	ns
t_{PHL}	$\overline{SE}$ to EQ	2.5	6.0	8.0	2.5	9.0	
t_{PLH}	Propagation Delay	6.5	12.5	16.0	6.5	17.0	ns
t_{PHL}	$\overline{SE}$ to GT	3.5	6.0	8.0	3.5	9.0	
t_{PLH}	Propagation Delay	5.0	10.5	13.5	5.0	14.5	ns
t_{PHL}	$\overline{SE}$ to LT	3.5	6.0	8.0	3.5	9.0	
t_{PLH}	Propagation Delay	4.0	8.5	11.0	4.0	12.0	ns
t_{PHL}	C/SI to C/SO	4.0	8.5	11.0	4.0	12.0	
t_{PLH}	Propagation Delay	8.0	15.0	19.5	8.0	20.5	ns
t_{PHL}	M to GT	6.0	12.0	17.5	6.0	18.5	
t_{PLH}	Propagation Delay	8.0	17.0	22.0	8.0	23.0	ns
t_{PHL}	M to LT	4.5	9.5	12.0	4.5	13.0	
t_{PLH}	Propagation Delay	15.0	25.0	33.0	15.0	35.0	ns
t_{PHL}	S_0, S_1 to EQ	9.0	15.0	19.0	9.0	20.0	
t_{PLH}	Propagation Delay	10.5	18.0	23.0	10.5	24.0	ns
t_{PHL}	S_0, S_1 to GT	10.5	18.0	23.0	10.5	24.0	
t_{PLH}	Propagation Delay	13.0	22.0	28.0	13.0	30.0	ns
t_{PHL}	S_0, S_1 to LT	12.0	19.0	24.0	12.0	25.0	
t_{PZH}	Output Enable Time	4.5	10.0	13.0	4.5	14.0	ns
t_{PZL}	S_0, S_1 to I/O_n	5.5	11.0	15.0	5.5	16.0	
t_{PHZ}	Output Disable Time	3.5	8.0	12.0	3.5	13.0	ns
t_{PLZ}	S_0, S_1 to I/O_n	4.5	9.6	12.5	4.5	13.5	

AC Operating Requirements

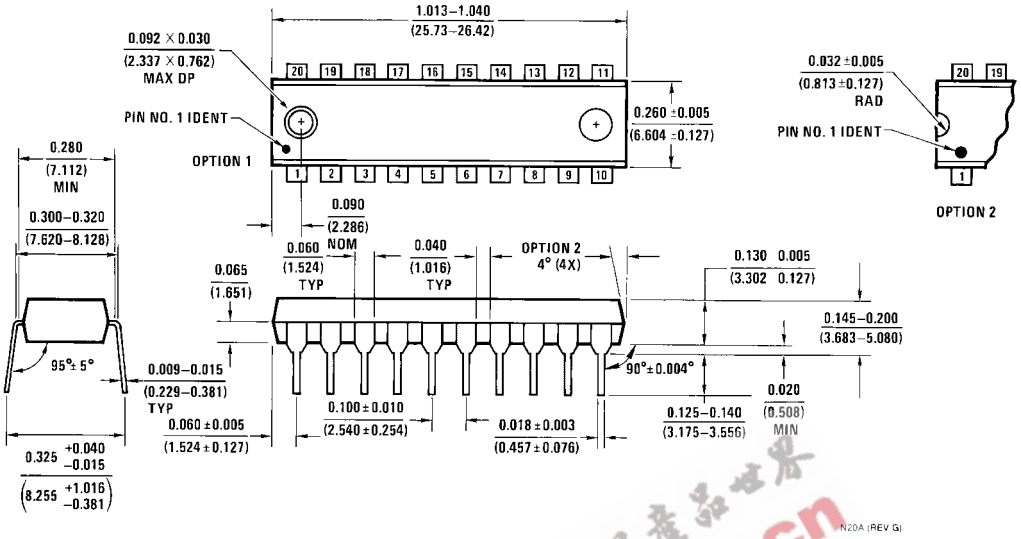
Symbol	Parameter	$T_A = +25°C$ $V_{CC} = +5.0V$		$T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V$		Units
		Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW	6.0		6.0		ns
$t_S(L)$	I/O_n to CP	6.0		6.0		
$t_H(H)$	Hold Time, HIGH or LOW	0		0		
$t_H(L)$	I/O_n to CP	0		0		
$t_S(H)$	Setup Time, HIGH or LOW	10.0		10.0		ns
$t_S(L)$	S_0 or S_1 to CP	10.0		10.0		
$t_H(H)$	Hold Time, HIGH or LOW	0		0		
$t_H(L)$	S_0 or S_1 to CP	0		0		
$t_S(H)$	Setup Time, HIGH or LOW	7.0		7.0		ns
$t_S(L)$	C/SI to CP	7.0		7.0		
$t_H(H)$	Hold Time, HIGH or LOW	0		0		
$t_H(L)$	C/SI to CP	0		0		
$t_W(H)$	Clock Pulse Width, HIGH	5.0		5.0		ns

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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